SmartFusion2 MSS

Fabric Interface Controller Configuration

Microsemi

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Introduction

The fabric interface controller (FIC) is part of the microcontroller subsystem (MSS). There are up to two FIC instances per MSS depending on the selected die:

- FIC_0 (available on every device)
- FIC_1 (may not be present in the smaller devices)

The clocks associated with each FIC sub-system inside the MSS are FIC_0_CLK and FIC_1_CLK. Each FIC sub-system can operate on a different clock frequency based on your system requirements. Each FIC can be configured to perform an AHB to AHB or AHB to APB bridging function between the AHB bus matrix and an AHB or APB bus in the FPGA fabric.

The FIC consumes no FPGA resources. Each FIC instance provides two bus interfaces between the MSS and the fabric. The first is mastered by the MSS and has slaves in the fabric and the second has a master in the fabric and slaves in the MSS.

Each FIC can be configured as an APB3 or AHBLite compliant interface. When configured as an AHBLite interface and mastered by fabric, FIC_0 and FIC_1 can each support up to four AHBLite fabric masters.

In addition to the choice of AHBLite or APB3 interfaces between the MSS and the fabric, a number of options related to relative clock frequencies and pipelining of transactions are available. In pipelined mode (default mode), the ratio between the MSS M3_CLK frequency and the frequency of each FIC AHBLite/APB3 sub-system can be configured as 1:1, 2:1, 4:1, 8:1, 16:1 or 32:1.

The FIC configurator helps you to define how the MSS is connected to the FPGA fabric.

Use the MSS Clock Conditioning Circuit Configurator (MSS CCC) to configure the M3_CLK to FIC_0_CLK and FIC_1_CLK clock ratios.

For complete details about the Fabric Interface Controller (FIC), please refer to the Microsemi SmartFusion2 User's Guide.

FIC_0/1 Configurator Overview

As shown in Figure 1, the FIC configurator (applies to both FIC_0 and FIC_1) is organized as follows. In the left panel, you can configure:

- The MSS to FPGA fabric interface
- Advanced AHBLite options
- The FPGA Fabric Address Regions (MSS Master View)

In the right panel, a dynamic picture displays the high level block diagram of the architecture you have chosen. The picture changes when you configure any option in the MSS To FPGA Fabric Interface group.

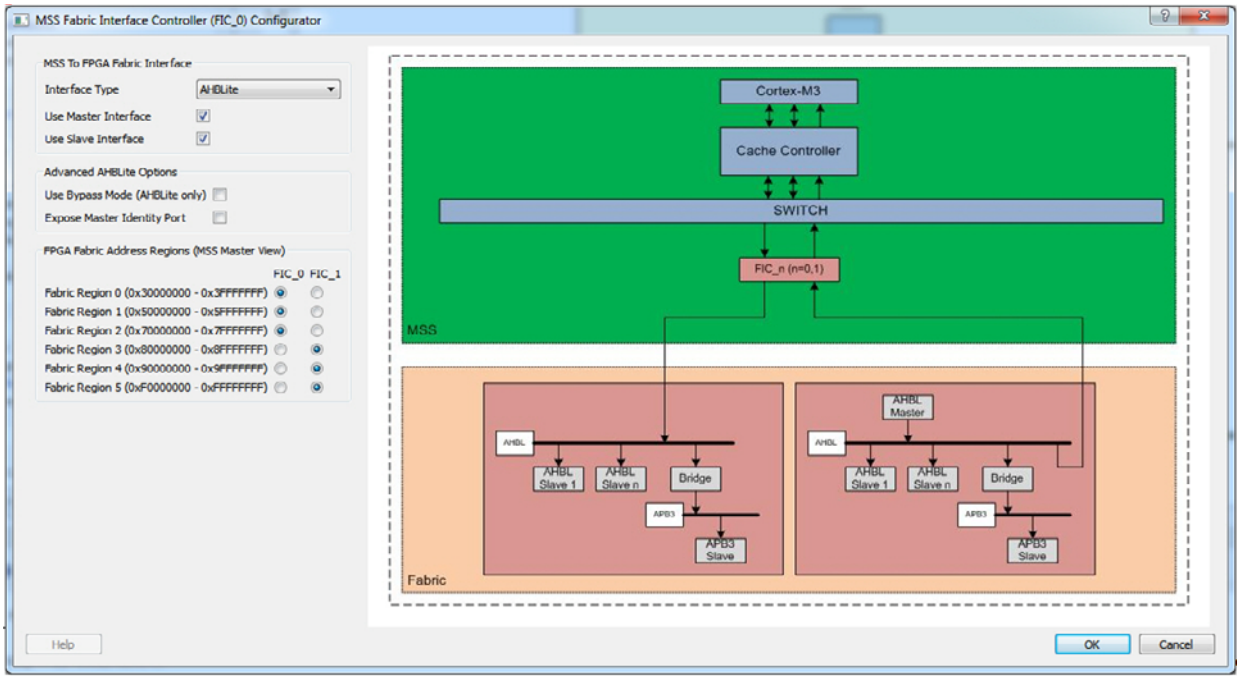

Figure 1 **• FIC Configurator Overview**

1 – Configuration Options

MSS To FPGA Fabric Interface

Interface Type - Use this option to select between the AMBA APB3 (AHB to APB bridge) and AHBLite (AHB to AHB bridge) FIC modes (as shown in Figure 1-1).

Use Master Interface - Use this option to expose the master Bus Interface (BIF) port. When selected, the port is automatically available on the MSS core.

Use Slave Interface - Use this option to expose the slave Bus Interface (BIF) port. When selected, the port is automatically available on the MSS core.

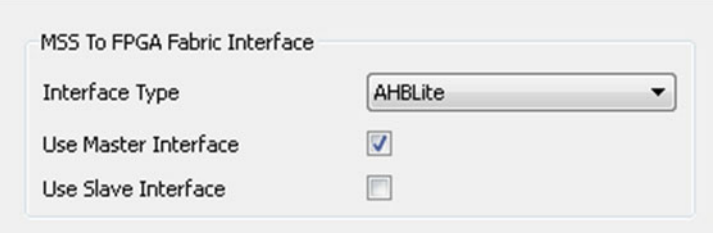

***Figure 1-1* • MSS to FPGA Fabric Interface Core**

Advanced AHBLite Options

Use Bypass Mode - In bypass mode, signals to and from the fabric are not registered, thus fewer clock cycles are required to complete each transaction but the overall system frequency may be lower than what could be achieved in pipelined mode (non-bypass mode).

Use this option to enable the FIC bypass mode. This option is only active when the interface type is AHBLite (as shown in Figure 1-2). The clock ratio between M3_CLK and the FIC_0_CLK and FIC_1_CLK must be set to 1:1 when the bypass mode is selected. This requirement is enforced in the MSS CCC Configurator when bypass is selected.

Expose Master Identity Port - The AHB Bus Matrix provides a 2-bit side band signal to the FPGA Fabric (one 2-bit signal per FIC instance). The side band signal indicates to the slave implemented in the FPGA fabric the identification of the master performing the current transaction. These signals have the same timing as other AHB master signals such as: HTRANS, HMASTLOCK etc. Table 1-1 provides the decoding of the master accessing the FPGA fabric Slave through the MSS AHB Bus Matrix.

***Table 1-1* • Master Identity Port Decoding**

MASTER_IDENTITY[1:0]	Accessing Master
00	IC-Bus, D-Bus and S-Bus Master
01	FIC_0, FIC_1 Master
10	HPDMA, Ethernet Master, PDMA, USB
11	SII Master/G Bus

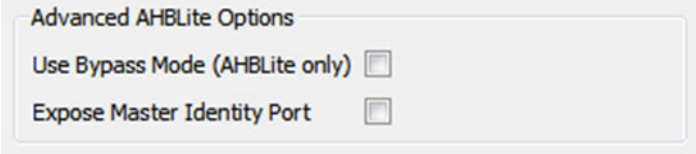

***Figure 1-2* • Advanced Options Configuration**

FPGA Fabric Address Regions (MSS Master View)

There are six 256 MB regions defined as FIC Regions 0 to 5 in the MSS memory map. Each of these regions can be allocated to the FIC_0 or FIC_1 slave interfaces in a mutually exclusive fashion. You can select to which FIC (0 or 1) slave interface you assign those regions by using the radio button next to each region in the FPGA Fabric Address Regions (MSS Master View) group box (as shown in Figure 1-3). This fabric region assignment is available only in the FIC_0 Configurator, but the fabric region assignment applies to FIC_1 also. Always configure FIC_0 first before configuring FIC_1.

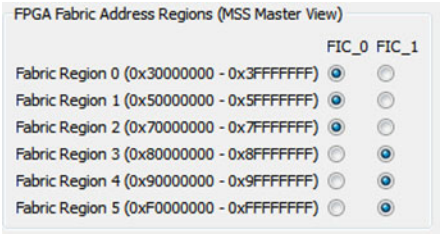

***Figure 1-3* • FPGA Fabric Address Regions (MSS Master View)**

2 – Port Description

***Table 2-1* • FIC Hard Master AHBLite Bus Interface - AHB_MASTER**

Port Name	Direction	Description
AHB_M_ADDR[19:0]	Out	Address bus - byte address on the bus interface
AHB_M_WDATA[31:0]	Out	Write data from the hard master to the fabric slave.
AHB_M_RDATA[31:0]	In	Read data from the fabric slave to the hard master.
AHB_M_LOCK	Out	Lock. When asserted, the current transfer is part of a locked transaction.
AHB_M_SIZE[1:0]	Out	Indicates the size of the current transfer (8/16/32 byte transactions) 00: byte (8-bit) 01: halfword (16-bit) 10: word (32-bit)
AHB_M_TRANS[1:0]	Out	Indicates the transfer type of the current transaction. 00 - Idle 01 - Busy 10 - Non-Sequential 11 - Sequential
AHB_M_WRITE	Out	When high, indicates that the current transaction is a write. When low, indicates that the current transaction is a read.
AHB_M_READY	In	When high, indicates that the bus is ready to accept a new transaction.
AHB_M_RESP	In	Response status - When driven high at the end of a transaction, indicates that the transaction has completed with errors. When driven low at the end of a transaction, indicates that the transaction has completed successfully.

***Table 2-2* • FIC Hard Master APB Bus Interface - APB_MASTER**

Port Name	Direction	Description
APB_M_ADDR[19:0]	Out	Address bus - byte address on the bus interface.
APB_M_WDATA[31:0]	Out	Write data from the hard master to the fabric slave.
APB_M_RDATA[31:0]	In	Read data from the fabric slave to the hard master.
APB_M_SEL	Out	Select. The AHB bus matrix to APB bridge unit generates a single select to the fabric.
APB_M_ENABLE	Out	Enable. This signal indicates the second and subsequent cycles of an APB transfer.

***Table 2-2* • FIC Hard Master APB Bus Interface - APB_MASTER (continued)**

Port Name	Direction	Description
APB_M_WRITE	Out	Direction. This signal indicates an APB write access when HIGH and an APB read access when LOW.
APB_M_READY	In	Ready. The slave uses this signal to extend an APB transfer.
APB_M_SLVERR	In	This signal indicates a transfer failure.

***Table 2-3* • FIC Hard Slave AHBLite Bus Interface - AHB_SLAVE**

Port Name	Direction	Description
AHB_S_ADDR[31:0]	In	Address bus from fabric master.
AHB_S_WDATA[31:0]	In	Write data from a fabric master to a slave.
AHB_S_RDATA[31:0]	Out	Read data from the selected slave to the fabric master.
AHB_S_M_MASTLOCK	In	Lock. When asserted, the current transfer is part of a locked transaction.
AHB_S_SIZE[1:0]	In	Indicates the size of the current transfer (8/16/32 byte transactions). 00: byte (8-bit) 01: halfword (16-bit) 10: word (32-bit)
AHB_S_TRANS[1:0]	In	Indicates the transfer type of the current transaction. 00 - Idle 01 - Busy 10 - Non-Sequential 11 - Sequential
AHB_S_SEL	In	Slave select. When asserted, it is being accessed by the fabric master.
AHB_S_WRITE	In	When high, indicates that the current transaction is a write. When low indicates that the current transaction is a read.
AHB_S_READY	In	When high, indicates that the bus is ready to accept a new transaction.
AHB_S_READYOUT	Out	Slave ready. When high for a write, indicates the selected subsystem slave is ready to accept data and when high for a read, indicates that data is valid.
AHB_S_RESP	Out	Response status. When driven high at the end of a transaction, indicates that the transaction has completed with errors. When driven low at the end of a transaction, indicates that the transaction has completed successfully.

***Table 2-4* • Hard Slave APB Bus Interface - APB_SLAVE**

Port Name	Direction	Description
APB_S_ADDR[31:0]	In	Address bus from fabric master.
APB_S_WDATA[31:0]	In	Write data from a fabric master to a slave.

Table 2-4 • **Hard Slave APB Bus Interface - APB_SLAVE (continued)**

Port Name	Direction	Description
APB_S_RDATA[31:0]	Out	Read data from the selected slave to the fabric master.
APB_S_SEL	In	Select. The AHB bus matrix to APB bridge unit generates a single select to the fabric.
APB_S_ENABLE	In	Enable. This signal indicates the second and subsequent cycles of an APB transfer.
APB_S_WRITE	In	Direction. This signal indicates an APB write access when HIGH and an APB read access when LOW.
APB_S_READY	Out	Ready. The slave uses this signal to extend an APB transfer.
APB_S_SLVERR	Out	This signal indicates a transfer failure.

A – Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call 800.262.1060
From the rest of the world, call 650.318.4460
Fax, from anywhere in the world, 650.318.8044

Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

Visit the Customer Support website (www.microsemi.com/soc/support/search/default.aspx) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the website.

Website

You can browse a variety of technical and non-technical information on the SoC home page, at www.microsemi.com/soc.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

My Cases

Microsemi SoC Products Group customers may submit and track technical cases online by going to My Cases.

Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office. Sales office listings can be found at www.microsemi.com/soc/company/contact/default.aspx.

ITAR Technical Support

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech_itar@microsemi.com. Alternatively, within My Cases, select **Yes** in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the ITAR web page.

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