SmartFusion2 MSS

AHB Bus Matrix Configuration

Microsemi

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Introduction

The SmartFusion2 Microcontroller Subsystem (MSS) AHB Bus Matrix is highly configurable. You can use the MSS AHB Bus Matrix configurator to configure the matrix remapping and arbitration schemes. To configure the AHB Bus Matrix access options, use the MSS Security configurator.

The values entered in the configurator are exported into the programming files for programming of the flash bits that control this functionality. The flash bits are loaded in the system registers at power up (or when the DEVRST_N external pad is asserted/de-asserted).

This document provides a brief description of these options. For more details, refer to the Microsemi SmartFusion2 Microcontroller Subsystem User Guide.

AHB Bus Matrix Configurator

1. Right-click Configure MSS in the Design Flow window and choose **Run**. The MSS Configurator appears (Figure 1).
2. Right-click AHB Bus Matrix in the MSS Configurator and choose **Configure**.

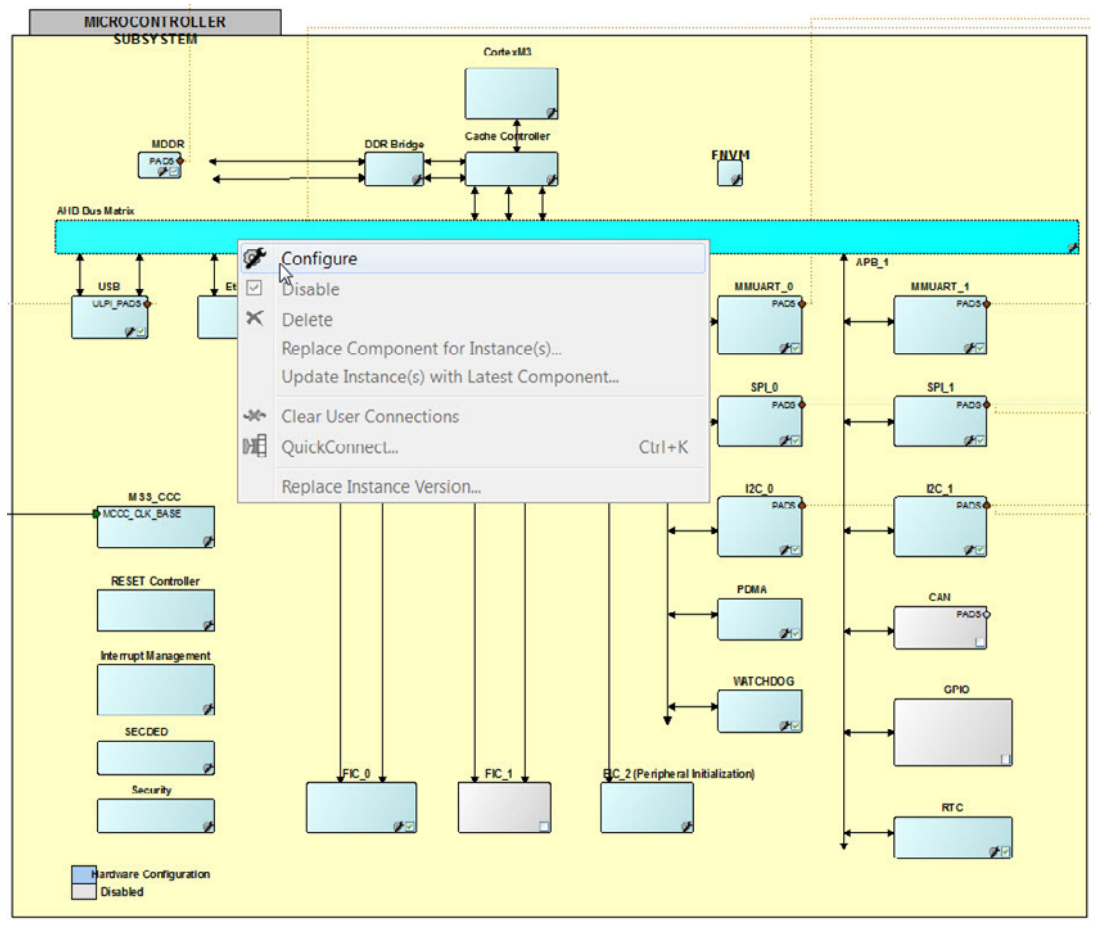

***Figure 1* • MSS Configurator**

1 – Configuration Options

Remapping

The AHB bus matrix provides support to remap eNVM, eSRAM and MDDR memory regions to location 0x00000000 of the ARM® Cortex™-M3 ID code space (Figure 1-1). Select one of the three memories to remap.

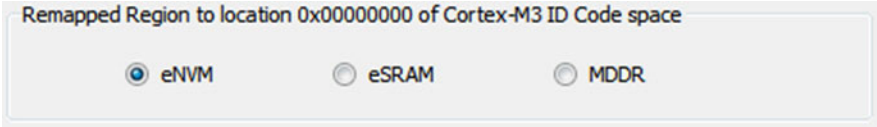

***Figure 1-1* • ARM® Cortex™-M3 Remapping Options**

eNVM is selected because memory locations 0x00000000 through 0x0007FFFF are mapped to the eNVM by default. You may select eSRAM or MDDR to change the mapping from the default.

The Configurator also provides an option to remap the eNVM for a Fabric-based Soft Processor (Figure 1-2). In this case, the eNVM will be mapped to address 0x0 of the Soft Processor which is connected to the Fabric Master Interface of the MSS. Click the checkbox to enable this option.

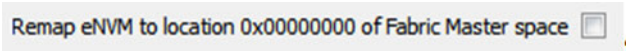

***Figure 1-2* • eNVM Remap for Soft Processor**

eNVM Remap - An eNVM can have multiple firmware images located at any of the possible locations of the eNVM array. But any image can be accessed from the zero or base address location in the virtual view by remapping the eNVM. The AHB bus matrix, under the control of the SYSREG block, handles the eNVM remap, whereby a virtual eNVM view is presented to the AHB bus for accesses in the range from 0x00000000 to 0x1FFFFFFF (Figure 1-3).

***Figure 1-3* • eNVM Remap Configuration**

eSRAM Remap - The AHB bus matrix supports remapping the eSRAM address space into code space (both eSRAM blocks are remapped) for error-correcting code (ECC) ON or OFF. When ECC is ON, the two eSRAM blocks are re-mapped to appear at the bottom of ARM® Cortex™-M3 code space, and the ECC eSRAM is not remapped, but can be used as scratchpad memory, addressable at its locations.

When ECC is OFF, the two eSRAM blocks are re-mapped to appear at the bottom of ARM® Cortex™-M3 code space and the ECC eSRAM is not available as the scratchpad memory.

MDDR Remap - In default mode, the ARM® Cortex™-M3 firmware boots from eNVM. However, it is also possible to get the firmware to boot from MDDR by re-mapping MDDR to location zero. Code shadowing is supported to facilitate this. User boot firmware, located in eNVM, must copy an executable image from external flash memory (serial or parallel) to external DDR memory, and then jump to the application entry point in external DDR memory.

eNVM Remap for Soft Processor - Any soft processor implemented within the FPGA fabric usually tries to fetch instructions from location 0x00000000. However, this refers to different code than the Cortex-M3 boot code, which resides at location 0x00000000 as far as the ARM® Cortex™-M3 microcontroller is concerned. The AHB bus matrix supports remapping of an eNVM segment to location 0x00000000 in the memory map seen by masters in the FPGA fabric with the ENVM_REMAP_FAB_CR control register, which configures where ENVM is mapped in fabric space. There is no eSRAM remap for fabric masters.

Arbitration

Each of the slave devices on the AHB bus matrix contains an arbiter. Arbitration is done at two levels to prevent bus contention. At the first level, the fixed higher priority masters are evaluated for any access request to the slave. At the second level, the remaining busses are evaluated in round robin fashion for any access request to the slave It should be noted that the user can override the arbitration scheme dynamically in their run-time code on the fly.

Note: Fixed Priority Masters have priority over Round Robin Masters.

The priority levels of masters with fixed priority are listed in Table 1.

Table 1 • **Fixed Priority Masters**

Masters		Priority	Arbitration Rate
M3 DCode bus	MM0	1	Fixed Priority
M3 ICode bus	MM1	2	Fixed Priority
M3 System bus	MM2	3	Fixed Priority
System controller	MM9	4	Fixed Priority

The Masters with Round Robin priority are listed in Table 2.

Table 2 • **Weighted Round Robin Masters**

Masters		Priority	Arbitration Rate
FIC_0	MM4	4	Round Robin
FIC_1	MM5	4	Round Robin
PDMA	MM7	4	Round Robin
HPDMA	MM3	4	Round Robin
USB	MM8	4	Round Robin
Ethernet Master (MAC)	MM6	4	Round Robin

The following slave arbitration configuration parameters are user programmable registers in the SYSREG block.

- **Programmable weight** - MASTER_WEIGHT0_CR and MASTER_WEIGHT1_CR are 5-bit programmable registers located in the SYSREG block that define the number of consecutive transfers (up to 32) the weighted master can perform without being interrupted by a fixed priority master, or before moving onto the next master in the WRR cycle. You can configure those programmable weights using this configurator (Figure 1-4).

Enter any value between 1 and 32 for the weight.

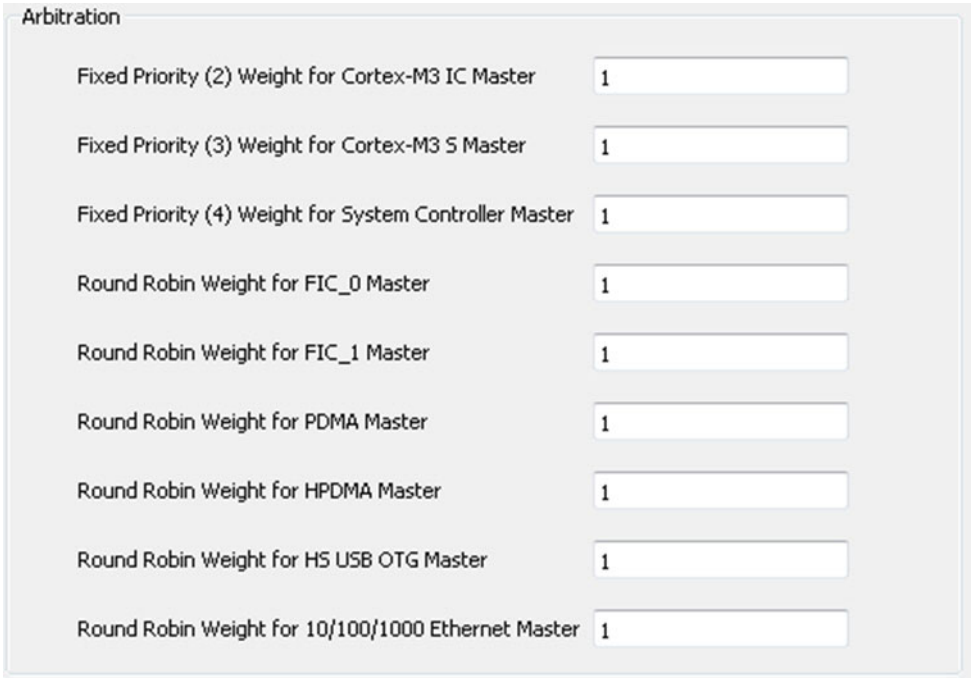

***Figure 1-4* • Programmable Weight Configuration**

- **Programmable slave maximum latency** - Slave maximum latency, ESRAM_MAX_LAT are 3-bit programmable registers located in the SYSREG block that decides the peak wait time for a fixed priority master arbitrating for eSRAM access while the WRR master is accessing the slave. After the defined latency period, the WRR master must re-arbitrate for slave access. Slave maximum latency is configurable from 1 to 8 clock cycles (8 by default). ESRAM_MAX_LAT is only supported for fixed priority masters addressing eSRAM slaves; it has no effect on WRR masters. The system designer can use this feature to ensure the processor latency for accesses to eSRAM is limited to a defined number of clock cycles. This is to facilitate limiting the ISR latency for real-time-critical functions (Figure 1-5).

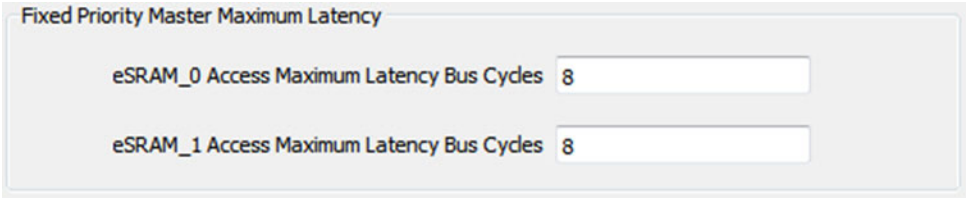

***Figure 1-5* • Programmable Slave Maximum Latency Configuration**

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From the rest of the world, call 650.318.4460
Fax, from anywhere in the world, 408.643.6913

Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

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Visit the Customer Support website (www.microsemi.com/soc/support/search/default.aspx) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the website.

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You can browse a variety of technical and non-technical information on the SoC home page, at www.microsemi.com/soc.

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The technical support email address is soc_tech@microsemi.com.

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