SmartFusion

Dedicated Fabric Clock Conditioning Circuit with PLL Integration

Actel
POWER MATTERS

Actel Corporation, Mountain View, CA 94043

Printed in the United States of America

Part Number: 5-02-00274-0

Release: June 2010

Trademarks

Table of Contents

1 Configuration Options

The Fabric Clock Conditioning Circuit (FAB_CCC) Configurator enables you to configure the second CCC/PLL block available only in the A2F500 device. This CCC/PLL is dedicated to the FPGA fabric.

The Fabric CCC can condition up to three input clocks and generate up to three global clocks. The configuration of the CCC can be broken down in the following four major blocks:

- Input reference clocks (CLKx) configuration
- Output Clocks (GLx) configuration
    - Clock source selection
    - Clock frequency and phase configurations
    - Clock delay configurations
- PLL feedback clock selection
- Glitch less clock multiplexing configuration

The Fabric Clock Conditioning Circuitry (FAB_CCC) is configured using flash cells based on the selection made in this configurator. You can also override the static configuration by using the configuration shift register available on the FAB_CCC block.

The Dedicated Fabric Clock Conditioning Circuit is shown in Figure 1-1.

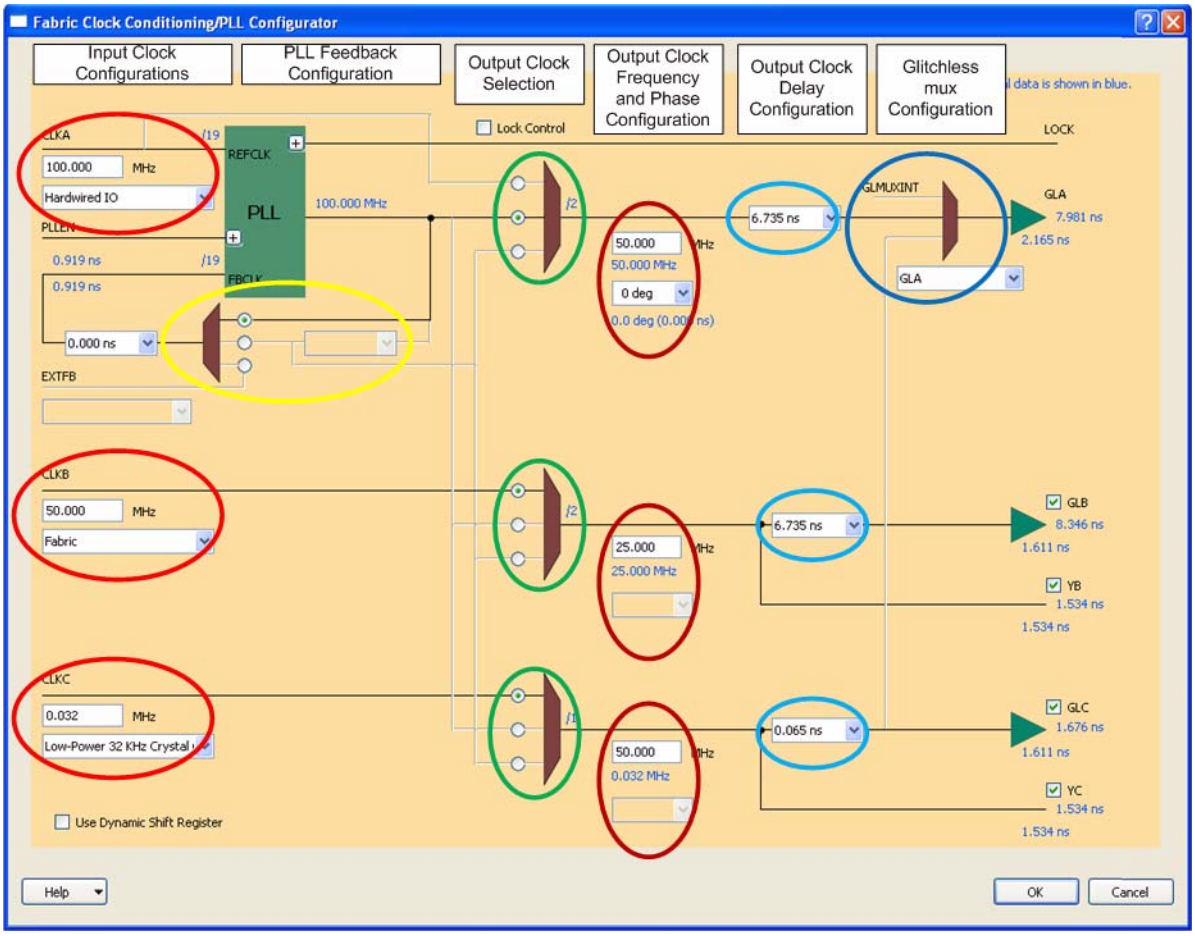

Figure 1-1 · FAB_CCC Configuration Options

CLK<x> (x= A/B/C) Input Clocks

To configure the CLK<x> reference clock, first select the clock source, then define the clock source.

Clock Source Selection

The following sources are available from the reference clock pull-down menu:

- **External I/O** - The clock source can be any fabric I/O. The regular FPGA I/O is routed to the reference clock fabric interface pin.
- **Hardwired I/O** - The clock source is one of three regular FPGA I/Os that has a dedicated path to drive the reference clock.
- **Hardwired I/O (LVPECL)** - The clock source is one of two regular FPGA I/Os (P side of the LVPECL pair) that has a dedicated path to drive the reference clock.
- **Hardwired I/O (LVDS)** - The clock source is one of two regular FPGA I/Os (P side of the LVDS pair) that has a dedicated path to drive the reference clock.

- **Internal logic** - The clock source can be any FPGA fabric logic.
- **On-chip RC Oscillator** - The clock source is a dedicated 100 MHz On-chip RC Oscillator available on the SmartFusion device. The on-chip RC oscillator is actually generated as part of the MSS clock configurator. Refer to the MSS_CCC Configurator for details of how to export the on-chip RC oscillator output port.
- **Main Crystal Oscillator** - The source is an external Crystal or an external RC circuit connected to the main crystal oscillator external pins. See the Actel SmartFusion Microcontroller Subsystem User's Guide for details about how the external crystal must be connected on the board to the SmartFusion device. This option is only available for CLKA and CLKB. The main crystal oscillator is actually generated as part of the MSS clock configurator. Refer to the MSS_CCC Configurator for details on how to export the main crystal oscillator output port.

Clock Frequency

You must specify the clock source frequency. Note the following frequency requirements:

- The On-chip Oscillator clock frequency is fixed to 100 MHz and cannot be changed.
- The Main Crystal Oscillator clock frequency must be between 1.5 MHz and 20 MHz when the PLL is used or between 32 KHz and 20 MHz when the PLL is bypassed. Use the same frequency as the one specified in the MSS_CCC configurator for the main crystal oscillator.
- The Main Crystal Oscillator (RC network configuration) clock frequency must be between 1.5 MHz and 4 MHz when the PLL is used or between 32 KHz and 4 MHz when the PLL is bypassed. Use the same frequency as the one specified in the MSS_CCC configurator for the main crystal oscillator.
- For all other sources, the source clock frequency must be between 1.5 MHz and 176 MHz when the PLL is used or between 32 KHz and 350 MHz when the PLL is bypassed.

GLx Output Clocks

GLA is always enabled. You may optionally enable the GLB (YB) and GLC (YC) clocks. The GLA, GLB and GLC clock drive a global network in the FPGA fabric; the YB and YC drive local routing resources in the FPGA. If you enable only the YB or YC output, the GLB or GLC global network cannot be used any more.

- **Clock Source Selection** - The source of the GLx clocks can either be:
  - Derived from the corresponding input clock CLKx (bypass mode). It can be a division of the input clock.
  - Derived from the CLKA reference clock using one of the PLL 4 output VCO phases.
  - Derived from the CLKA reference clock using the PLL output VCO (phase 0) with a programmable delay.
- **Clock Frequency** - You must specify the output clock frequencies. This frequency is used by the FAB_CCC configuration engine to automatically compute the CCC dividers to meet your frequency requirements. The dividers are highlighted in blue (for instance /2) in the configurator UI.
- **Phase Configuration** - The PLL block offers 4 phases that you can access through the phase selection pull-down menu. The actual phases and resulting delays are highlighted in blue on the configurator UI. The actual phase is not the same as the selected phase if the output divider is not 1 (actual_phase = selected_phase / output_divider). The actual delay is a function of the actual phase of the PLL output (VCO).
- **Delay Configuration** - For GLx only, you may configure the programmable delay to further tune the overall CLKA to GLx delays (when the PLL is used) or CLKx to GLx delays (when the bypass mode is used) based on your system requirements. The programmable delays are typical delays. The total delays are highlighted in blue in the configurator UI. The delays provided by the configurator are typical delays and match those computed by SmartTime typical conditions.

PLL Feedback Clock

- **PLL Feedback Source** - If the you use the PLL, you can choose to use an internal or an external feedback loop depending on your system level requirements:
  - **Internal feedback from VCO (phase 0) without programmable delay** - This is the default choice.

- **Internal feedback from VCO (phase 0) with programmable delay** - Use a fine grain programmable delay to tune your overall CCC delays based on your system requirements. The programmable delays are typical delays
- **External I/O** - The clock source can be any regular FPGA I/O. The regular FPGA I/O is routed to the feedback clock fabric interface pin.
- **Hardwired I/O** - The clock source is one of three regular FPGA I/Os that has a dedicated path to drive the feedback clock.
- **Hardwired I/O (LVPECL)** - The clock source is one of two regular FPGA I/Os (P side of the LVPECL pair) that has a dedicated path to drive the feedback clock.
- **Hardwired IO (LVDS)** - The clock source is one of two regular FPGA I/Os (P side of the LVDS pair) that has a dedicated path to drive the feedback clock.
- **Fabric** - The clock source can be any FPGA fabric logic.

- **Programmable Fix Delay** - You can also add a fix delay (~2 ns typical) to your feedback loop. This delay has been defined to be about the same delay as the clock network within the FPGA (GLx to the input of a flip-flop).

Note: When the PLL is used with an external feedback, all engine computations are based on the assumptions that the external feedback is driven from the GLA fabric CCC output whether through the fabric or externally to the chip. The engine also assumes a delay of 0 ns for the path from GLA to the fabric CCC external feedback input. To have the correct delays at the system level you must adjust the delay computation based on the actual typical external delay.

Glitchless Clock Multiplexing

You can configure the glitch less clock multiplexor as follows:

- **GLA** - No dynamic multiplexing is available and the GLA output comes from the CCC internal GLA signal.
- **GLA_GLC** - You can make a glitchless switch between the CCC internal GLA signal and the CCC internal GLC signal. The output of the glitchless clock multiplexor comes out on the GLA global network.
- **GLA_GLMUXINT** - You can make a glitchless switch between the CCC internal GLA signal and the FPGA fabric signal GLMUXINT. The output of the glitchless clock multiplexor comes out on the GLA global network.

Dynamic Shift Register

You can dynamically configure or re-configure the Fabric CCC in your design by using the CCC configuration dynamic shift register. Click the **Use Dynamic Shift Register** check box to enable this option. The ports used to configure this register are SDIN, SCLK, SSHIFT, SUPDATE, SDOUT and MODE and are described in "Port Description" on page 11.

Table 1-1 describes the CCC configuration shift register from SDIN to SDOUT. This table can be generated from the Designer Software Tools > Report > Global > CCC_Configuration menu after layout is complete. You must complete layout because as some configuration bits can only be computed based on the placement of the design. The columns are defined as follows:

- **NAME** - The configuration signal as defined on the FAB_CCC_DYN CAE macro.
- **SDIN** - The register bit numbers.
- **VALUE** - The configuration value as defined in the configurator and assigned to the configuration signal.
- **TYPE** - The type of the configuration with respect to what you are allowed to change when using the CCC configuration shift register. Configuration bits marked EDIT can be safely changed by you. Those marked MASKED

should not be changed as they are defined by the placement of the design. Finally, configurations marked READONLY should not be changed.

Table 1-1 · CCC Configuration Shift Register from SDIN to SDOUT

NAME	SDIN	VALUE	TYPE
FINDIV	[6: 0]	0010010	EDIT
FBDIV	[13: 7]	0010010	EDIT
OADIV	[18:14]	00001	EDIT
OBDIV	[23:19]	00000	EDIT
OCDIV	[28:24]	00000	EDIT
OAMUX	[31:29]	100	EDIT
OBMUX	[34:32]	000	EDIT
OCMUX	[37:35]	000	EDIT
FBSEL	[39:38]	01	EDIT
FBDLY	[44:40]	00000	EDIT
XDLYSEL	[45]	1	EDIT
DLYGLA	[50:46]	00011	EDIT
DLYGLB	[55:51]	11111	EDIT
DLYGLC	[60:56]	00000	EDIT
DLYA0	[65:61]	00000	EDIT
DLYA1	[70:66]	00000	EDIT
STATASEL	[71]	0	MASKED
STATBSEL	[72]	1	MASKED
STATCSEL	[73]	1	MASKED
VCOSEL	[76:74]	000	EDIT
RESETEN	[80]	1	READONLY
RXASEL	[81]	0	MASKED
RXBSEL	[82]	0	MASKED
RXCSEL	[83]	0	MASKED
OADIVHALF	[84]	0	EDIT
OBDIVHALF	[85]	0	EDIT
OCDIVHALF	[86]	0	EDIT
GLMUXCFG	[88:87]	00	MASKED

For more details about the architecture of the SmartFusion fabric CCC and the definition of the configuration bits, please refer to the Actel SmartFusion FPGA Fabric User's Guide.

2 Port Description

In Table 2-1, 'x' indicates A, B or C.

Table 2-1 · FAB_CCC Port Description

Port Name	Direction	PAD?	Description
CLKx	IN	No	Reference clock when driven from Internal Logic or External I/O
CLKx_PAD	IN	Yes	Reference clock when driven from Hardwired I/O
CLKx_PADP	IN	Yes	Reference clock P side when driven from Hardwired I/O (LVDS) or Hardwired I/O (LVPECL)
CLKx_PADN	IN	Yes	Reference clock N side when driven from Hardwired I/O (LVDS) or Hardwired I/O (LVPECL)
RCOSC	IN	No	Reference clock when driven from On-chip RC Oscillator
MAINXIN	IN	No	Reference clock when driven from Main Crystal Oscillator
EXTFB	IN	No	PLL feedback clock when driven from Internal Logic or External I/O
EXTFB_PAD	IN	Yes	PLL feedback clock when driven from Hardwired I/O
EXTFB_PADP	IN	Yes	PLL feedback clock P side when driven from Hardwired I/O (LVDS) or Hardwired I/O (LVPECL)
EXTFB_PADN	IN	Yes	PLL feedback clock N side when driven from Hardwired I/O (LVDS) or Hardwired I/O (LVPECL)
GLx	OUT	No	Generated clock driving clock FPGA fabric global network 'x'
Yx	OUT	No	Generated clock driving clock FPGA fabric local routing resource
OxDIVRST	IN	No	OxDIVRST is available when the GLx or Yx output is not derived from the PLL VCO output; it is in bypass mode with an output divider greater than 1. The purpose of the OADIVRST signal is to reset the output of the final clock divider to synchronize it with the input to that divider when the PLL is bypassed. The signal is active on a low to high transition. The signal must be low for at least one divider input.
PLLEN	IN	No	PLL Enable signal; this signal is active high or low based on the polarity chosen in the configurator.
LOCK	OUT	No	PLL Lock indicator signal; this signal is asserted (lock) high or low based on the polarity chosen in the configurator
GLMUXINT	IN	No	FPGA fabric input to the CCC glitchless MUX
GLMUXSEL	IN	No	FPGA fabric input used to make a glitchless switch between GLA and GLMUXINT or GLA and GLC.
SDIN	IN	No	Dynamic shift register serial data in
SCLK	IN	No	Dynamic shift register serial clock

Table 2-1 · FAB_CCC Port Description

Port Name	Direction	PAD?	Description
SSHIFT	IN	No	Dynamic shift register serial shift data command; the data present on SDIN is shifted into the CCC configuration shift register on the rising edge of SCLK.
SUPDATE	IN	No	Dynamic shift register serial data update; the data present in the shift register is applied to the CCC as a new configuration
SDOUT	OUT	No	Dynamic shift register serial data out; the last bit of the CCC configuration shift register
MODE	IN	No	If MODE is 0, the CCC configuration data is coming from the CCC configuration register else it is coming from the programmed flash cells

A

Product Support

Actel backs its products with various support services including Customer Service, a Customer Technical Support Center, a web site, an FTP site, electronic mail, and worldwide sales offices. This appendix contains information about contacting Actel and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From Northeast and North Central U.S.A., call **650.318.4480**
From Southeast and Southwest U.S.A., call **650. 318.4480**
From South Central U.S.A., call **650.318.4434**
From Northwest U.S.A., call **650.318.4434**
From Canada, call **650.318.4480**
From Europe, call **650.318.4252** or **+44 (0) 1276 401 500**
From Japan, call **650.318.4743**
From the rest of the world, call **650.318.4743**
Fax, from anywhere in the world **650.318.8044**

Actel Customer Technical Support Center

Actel staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions. The Customer Technical Support Center spends a great deal of time creating application notes and answers to FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Actel Technical Support

Visit the Actel Customer Support website (www.actel.com/support/search/default.aspx) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the Actel web site.

Website

You can browse a variety of technical and non-technical information on Actel's home page, at www.actel.com.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. Several ways of contacting the Center follow:

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is tech@actel.com.

Phone

Our Technical Support Center answers all calls. The center retrieves information, such as your name, company name, phone number and your question, and then issues a case number. The Center then forwards the information to a queue where the first available application engineer receives the data and returns your call. The phone hours are from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. The Technical Support numbers are:

650.318.4460
800.262.1060

Customers needing assistance outside the US time zones can either contact technical support via email (tech@actel.com) or contact a local sales office. Sales office listings can be found at www.actel.com/company/contact/default.aspx.

Actel is the leader in low-power and mixed-signal FPGAs and offers the most comprehensive portfolio of system and power management solutions. Power Matters. Learn more at www.actel.com.

Actel Corporation *• 2061 Stierlin Court • Mountain View, CA 94043 • USA*
Phone 650.318.4200 • Fax 650.318.4600 • Customer Service: 650.318.1010 • Customer Applications Center: 800.262.1060

Actel Europe Ltd*. • River Court, Meadows Business Park • Station Approach, Blackwater • Camberley Surrey GU17 9AB • United Kingdom*
Phone +44 (0) 1276 609 300 • Fax +44 (0) 1276 607 540

Actel Japan *• EXOS Ebisu Building 4F • 1-24-14 Ebisu Shibuya-ku • Tokyo 150 • Japan*
Phone +81.03.3445.7671 • Fax +81.03.3445.7668 • http://jp.actel.com

Actel Hong Kong *• Room 2107, China Resources Building • 26 Harbour Road • Wanchai • Hong Kong*
Phone +852 2185 6460 • Fax +852 2185 6488 • www.actel.com.cn

5-02-00274-0/06.10