SmartDesign MSS

How to Create a MSS and Fabric AMBA AHBLite Design (MSS Master Mode)

Actel
POWER MATTERS

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1 Configuration and Connectivity

The SmartFusion Microcontroller Subsystem enables you to naturally extend the AMBA Bus into the FPGA fabric. You can configure the AMBA fabric interface as either APB3 or AHBLite depending on your design needs. A master and a slave bus interface is available in each mode.

This document provides the essential steps to creating mixed MSS-FPGA fabric AMBA AHBLite/APB3 system using the MSS configurator available in the Libero® IDE software.

AHBLite peripherals are connected to the MSS using **CoreAHBLite version 3.0.112** or greater.

The following steps connect AHBLite peripherals implemented in the FPGA fabric to the MSS.

MSS Configuration

Step 1. Select the MSS FCLK (GLA0) to fabric clock clock ratio.

Select the FAB_CLK divisor in the MSS Clock Management Configurator as shown Figure 1-1. You must perform post-layout static timing analysis to ensure that the design meets the timing requirements defined in the Clock Management Configurator. You may have to adjust the clock ratio between the MSS and the fabric to get a functional design.

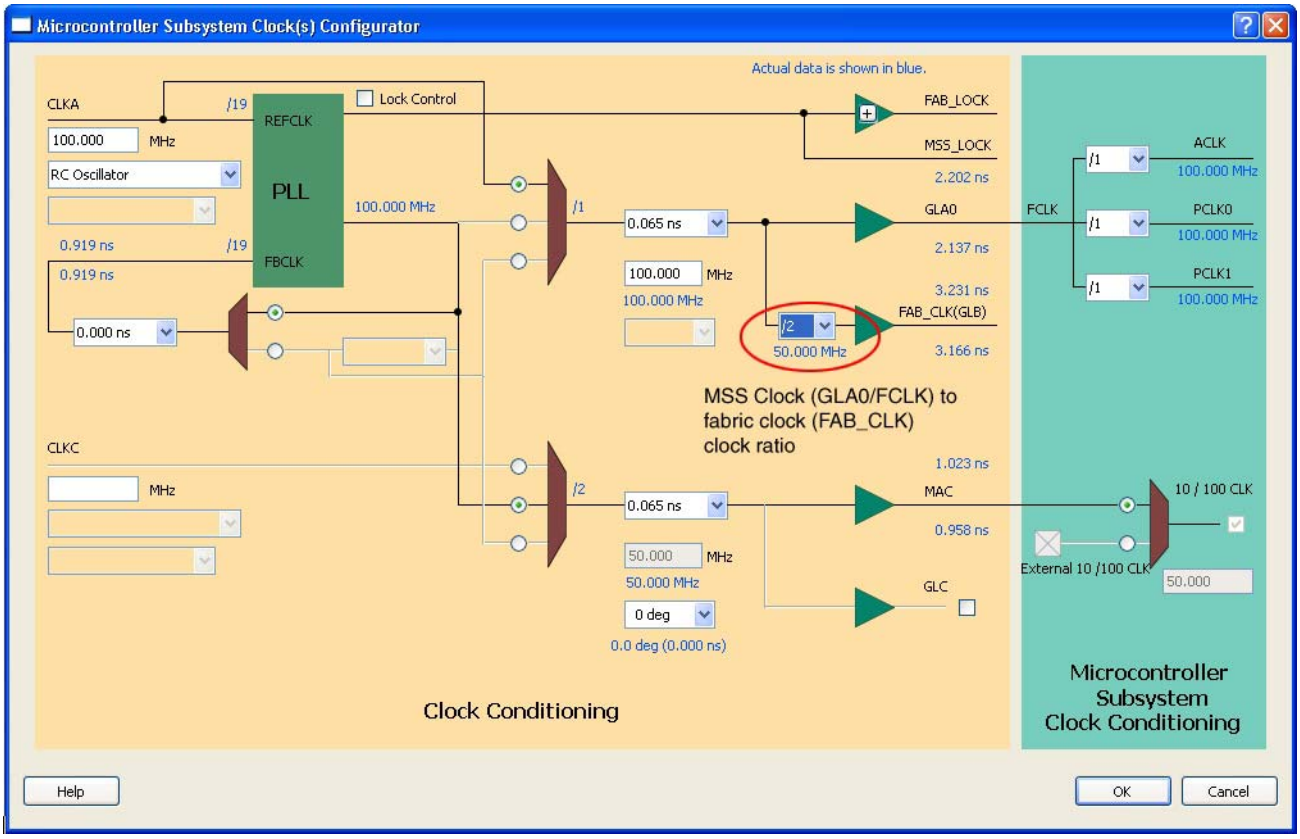


Figure 1-1 · Fabric Clock Clock Ratio

Step 2. Select the MSS AMBA mode.

Select the AHBLite Interface. Type in the MSS Fabric Interface Configurator as shown in Figure 1-2.

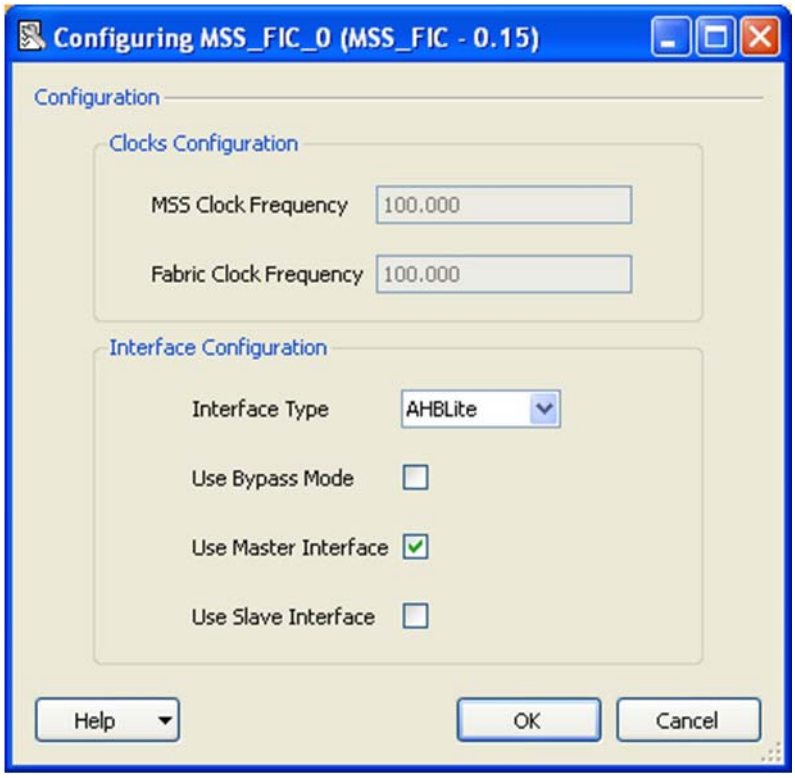


Figure 1-2 · AHBLite Interface Selected

Step 3. Promote the Fabric Interface AHBLite Bus Interface (BIF) master port (as shown in Figure 1-3).

- Enable the AHBLite Master Bus Interface (BIF) as shown in Figure 1-2.
- In the MSS configurator, right-click the **Bus Interface master port** (MSS Fabric Interface core) and choose **Promote-to-top**. The BIF master port will then be available to the next level of hierarchy (where the fabric extension needs to be implemented).

Step 4. Promote FAB_CLK to make it a port (as shown in Figure 1-3).

- In the MSS configurator, right-click **FAB_CLK** (MSS Clock Management core) and choose **Clear attribute**, then right-click it again and choose **Promote-to-top**. The FAB_CLK port will then be available to the next level of hierarchy (where the fabric extension needs to be implemented).

Note: Actel recommends that you not change the FAB_CLK top-level port name. The SmartDesign auto-connect feature only works if the FAB_CLK port name has not been changed.

Step 5. Promote M2F_RESET_N to make it a port.

- In the MSS configurator, right-click **M2F_RESET_N** (MSS Reset Management core) and choose **Clear attribute**. The M2F_RESET_N port will then be available to the next level of hierarchy (where the fabric extension needs to be implemented).

Note: Actel recommends that you not change the M2F_RESET_N top level port name. The SmartDesign auto-connect feature only works if the M2F_RESET_N port name has not been changed.

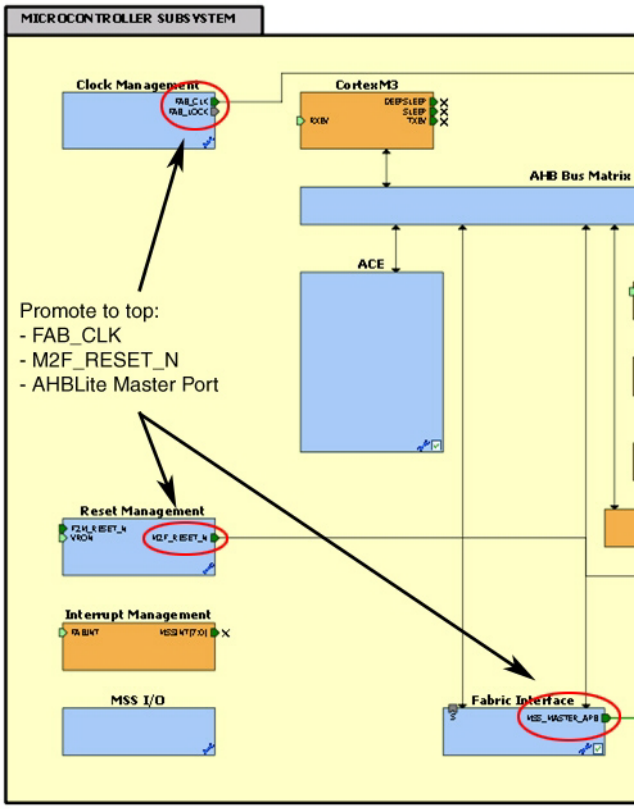


Figure 1-3 · Promote FAB_CLK, M2F_RESET_N and AHBLite Master Port

Create the FPGA Fabric and AMBA Subsystem

The fabric AMBA subsystem is created into a regular SmartDesign component, and then the MSS component is instantiated into that component (as shown in Figure 1-4).

Step 1. Instantiate and configure CoreAHBLite.

- Select the Memory Mode 1 as shown in Figure 1-4. This mode provides 15 64KB slots that can be used to connect 15 AHBLite slaves. You may ignore the 16 4KB clients slots (mapped into Slot 4) and the huge slot as they are irrelevant in this particular MSS master configuration.

- Enable the slots that you are planning on using for your application. Enable the slots from the **ENABLE Master1 AHBLite Slave Slots** group as shown in the figure below. Only slots 5 to 15 can be used when CoreAHBLite is connected to the MSS component. See the "Memory Map Computation" on page 13.

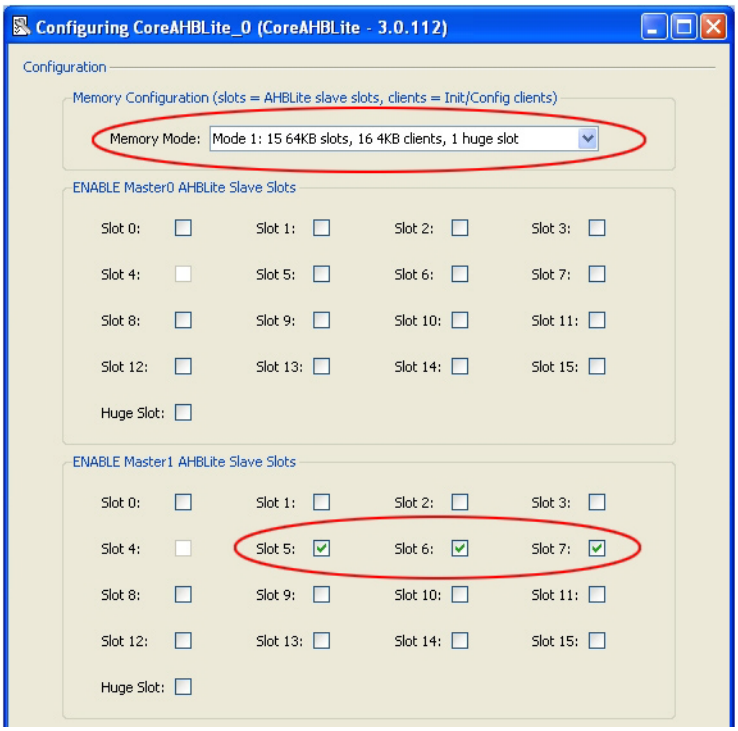


Figure 1-4 · Configuring AHBLite: Memory Mode and Slave Slots

Step 2. Instantiate and configure AMBA AHBLite peripherals in your design.

Step 3. Connect the subsystem together.

- Select the direct addressing mode.
- Select the 32-bit APB bus master data bus width. It is the width of the MSS AMBA data bus width.
- Disable the slots that you do not plan on using for your application. All slots are available. See the "Memory Map Computation" on page 13 for more details about slot sizes and slave/slot connection.

- Select the APB slot size as 4KB or below as shown in Figure 1-5. Assuming that you have selected 64KB slot sizes for CoreAHBLite, then the maximum size of the slots on CoreAPB3 (16 slots) is 64KB/16 = 4KB when going through CoreAHBtoAPB3.

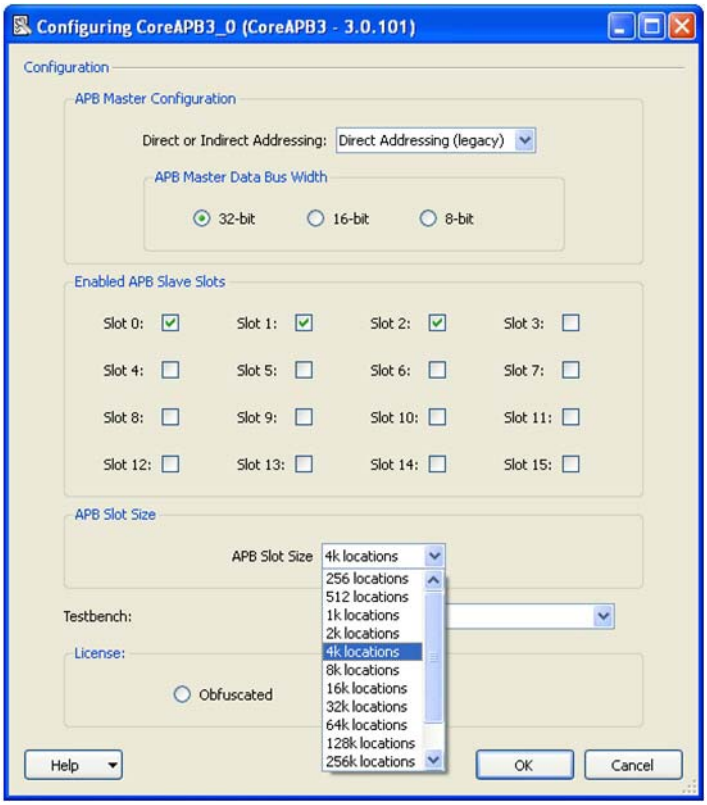


Figure 1-5 · Select the APB Slot Size

Step 4. Instantiate and configure AMBA AHBLite and APB peripherals in your design.

Step 5. Connect the subsystem together. This can be done automatically or manually.

Automatic Connection - The SmartDesign auto-connect feature (available from the SmartDesign Menu, toolbar or by right-clicking the Canvas) automatically connects the subsystem clocks and resets and present you with a memory map editor where you can assign the AHBLite slaves to the proper addresses (Figure 1-6). Note that the auto-connect feature

performs the clock and reset connections only if the FAB_CLK and M2F_RESET_N port names have not been changed on the MSS component.

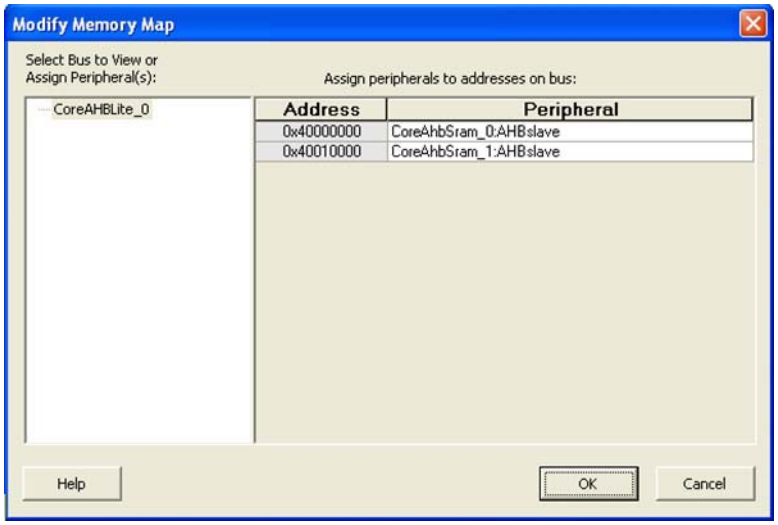


Figure 1-6 · AHBLite Memory Map

Manual Connection- Connect the subsystem as follows:

- Connect the CoreAHBLite mirrored-master BIF M0 or M1 to the MSS Master BIF (as shown in Figure 1-7). Use M1 if you plan to create a multi-master subsystem where you have a master in the fabric that requires the remap feature and thus needs to be connected to M0.
- Connect the AHBLite slaves to the proper slots as per your memory map specification.
- Connect FAB_CLK to HCLK of all AHBLite peripherals in your design.
- Connect M2F_RESET_N to HRESET of all AHBLite peripherals in your design.

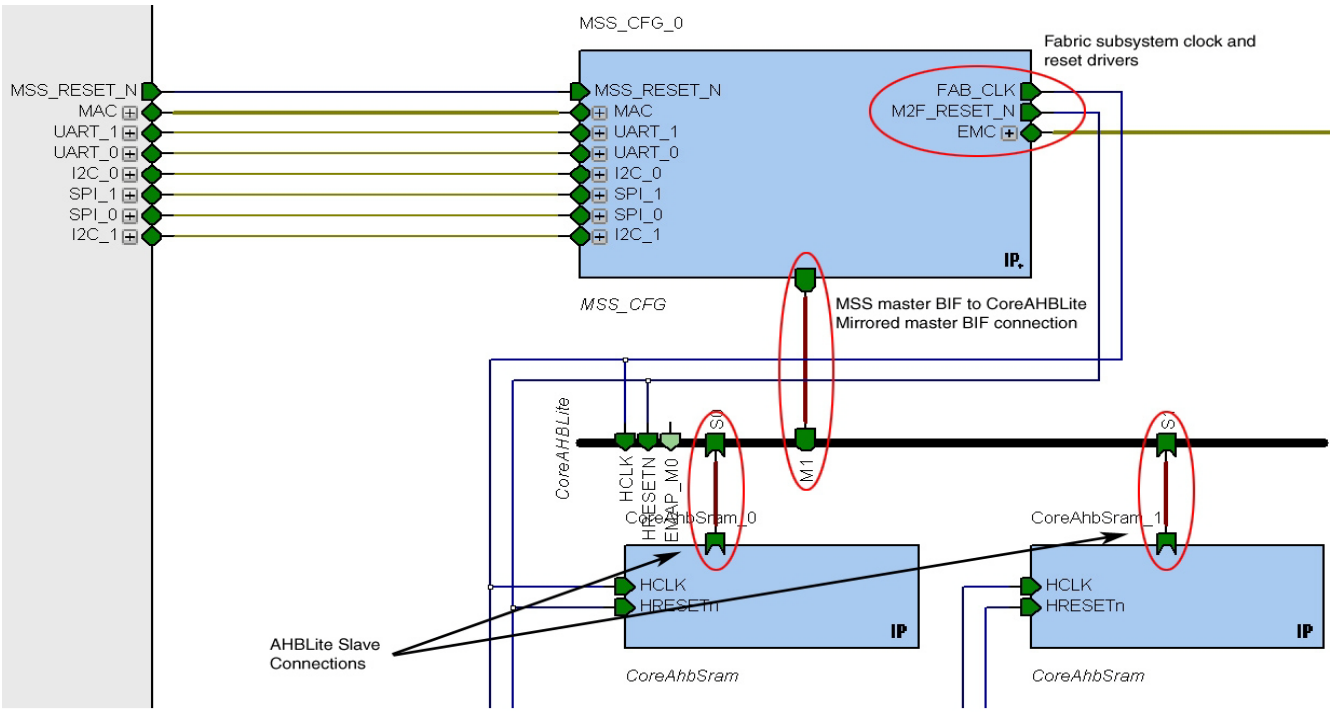


Figure 1-7 · Manual Connections in Subsystem

2 Memory Map Computation

General Formula

For AHBLite, the slot size is always 64KB slots = 65536 slots (0x10000).

For each slot 5 to 15 (slots 0 to 4 are prohibited as per the CortexM3 memory map), the address of client peripheral is: 0x40000000 + (slot number * 0x10000).

Note: The base address for the fabric is fixed at 0x4005000, but to simplify the memory map equation we are showing the base address as 0x40000000.

Example 1:

If the peripheral is at slot number 7, then, its address is:

0x40000000 + (0x7 * 0x10000) = 0x40070000

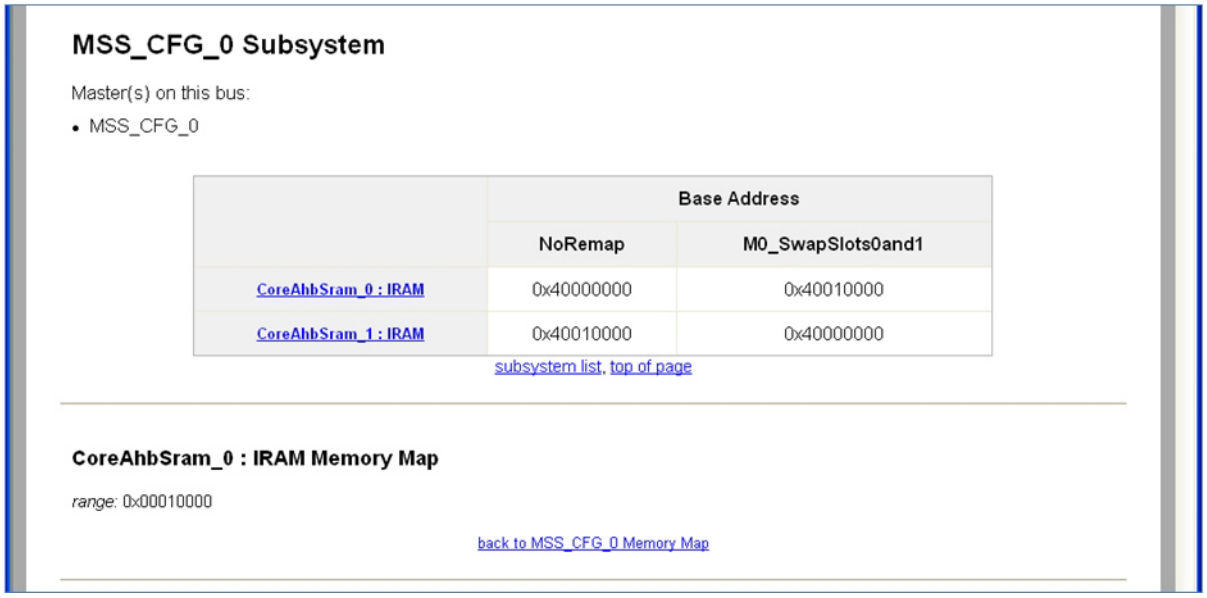
Example 2:

If the peripheral is at slot number 15, then, its address is:

0x40000000 + (0xF * 0x10000) = 0x400F0000

Memory Map View

You can see the system memory map by using the SmartDesign Memory Map / Data Sheet feature (from the SmartDesign menu in the Libero IDE Project Manager). For example, here is the memory map generated for the subsystem shown in Figure 1-7 on page 11.



MSS_CFG_0 Subsystem

Master(s) on this bus:

- MSS_CFG_0

	Base Address	
	NoRemap	M0_SwapSlots0and1
CoreAhbSram_0 : IRAM	0x40000000	0x40010000
CoreAhbSram_1 : IRAM	0x40010000	0x40000000

subsystem list, top of page

CoreAhbSram_0 : IRAM Memory Map

range: 0x00010000

back to MSS_CFG_0 Memory Map

Figure 2-1 · Memory Map

A

Product Support

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Actel Technical Support

Visit the Actel Customer Support website (www.actel.com/support/search/default.aspx) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the Actel web site.

Website

You can browse a variety of technical and non-technical information on Actel's home page, at www.actel.com.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. Several ways of contacting the Center follow:

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is tech@actel.com.

Phone

Our Technical Support Center answers all calls. The center retrieves information, such as your name, company name, phone number and your question, and then issues a case number. The Center then forwards the information to a queue where the first available application engineer receives the data and returns your call. The phone hours are from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. The Technical Support numbers are:

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Customers needing assistance outside the US time zones can either contact technical support via email (tech@actel.com) or contact a local sales office. Sales office listings can be found at www.actel.com/company/contact/default.aspx.

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