

# SmartDesign MSS

**GPIO** Configuration



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# **Configuration Options**

The SmartFusion Microcontroller Subsystem (MSS) provides a GPIO hard peripheral (APB\_1 sub bus) with 32 configurable GPIOs. The actual behavior of each GPIO (input, output and output enable register controls, interrupt modes, etc.) can be defined at the application level using the SmartFusion MSS GPIO Driver provided by Actel. However, you must define whether a GPIO is directly connected to an external pad (MSS I/O) or to the FPGA fabric. This portion of the device configuration is done using the MSS GPIO configurator and is described in this document.

For more details about the MSS GPIO hard peripheral, please refer to the Actel SmartFusion Microcontroller Subsystem User's Guide.

### **Connectivity Options**

MSS I/O Pad - Select this option to indicate that the selected GPIO will be connected to an external dedicated pad (MSS I/O). You must select the type of I/O buffer - INBUF, OUTBUF, TRIBUFF and BIBUF - that will define how the MSS I/O pad is being configured. Note that this option may not be available if the MSS I/O is already used by another peripheral or the fabric (see the MSS I/O Sharing section for more details)

Fabric - Select this option to indicate that the selected GPIO will be connected to the FPGA fabric. You must select whether you want the GPI (Input), GPO (Output) or both GPI and GPO (Input/Output) connection(s) to be brought out to connect to the fabric. Note that the GPIO output enable register cannot be brought out to the fabric when this option is selected. Also, GPI's connected to the fabric can trigger interrupts from user logic if the appropriate interrupt enable bits are set properly by your application (MSS GPIO driver initialization functions).

## MSS I/O Sharing

In the SmartFusion architecture MSS I/Os are shared between two MSS peripherals or between a MSS peripheral and the FPGA fabric. MSS GPIOs may not be able to connect to a particular MSS I/O if this I/Os is already connected to a MSS peripheral or to the FPGA fabric. The GPIO configurator provides direct feedback regarding whether a GPIO can be connected to a MSS I/O or not.

#### **GPIO**[31:16]

GPIO[31:16] are organized in groups that indicate which MSS peripheral they are sharing MSS I/Os with. If a peripheral is used (enabled on the MSS canvas), then the MSS I/O Pad pull-down menu is grayed-out for the corresponding shared GPIOs and an Info icon is displayed next to the pull-down menu. The Info icon indicates that the MSS I/O option cannot be selected because it is already used by a MSS peripheral or, based on the package selected, not bonded.

#### **Example 1**

SPI\_0, SPI\_1, I2C\_0, I2C\_1, UART\_0 and UART\_1 are enabled in the MSS canvas.

- GPIO[31:16] cannot be connected to an MSS I/O. Note the grayed-out menus and the Info icons (Figure 1-1).
- GPIO[31:15] can still be connected to the FPGA fabric. In this example, GPIO[31] is connected to the fabric as an Output and GPIO[30] as an Input.



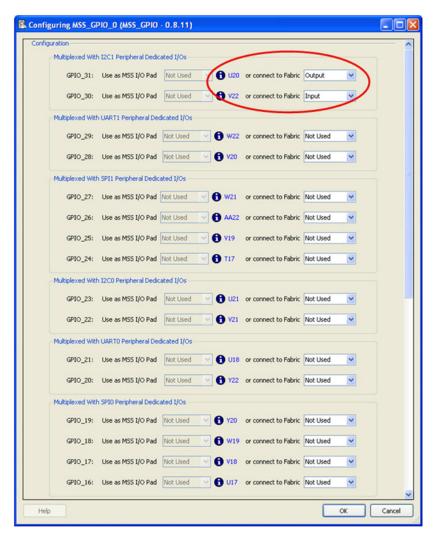


Figure 1-1 · GPIO Configuration Example 1

#### **Example 2**

I2C\_0 and I2C\_1 are disabled in the MSS canvas.

- GPIO[31:30] and GPIO[23:22] can be connected to an MSS I/O (as shown in Figure 1-2).
   In this example, both GPIO[31] and GPIO[30] are connected to a MSS I/O as Output ports.
   In this example, GPIO[23] is connected to a MSS I/O as an Input port and GPIO[22] is connected to an MSS I/O as a Bidirectional port.
- GPIO[29:24,21:16] cannot be connected to an MSS I/O. Note the grayed-out menus and the Info icons.



• GPIO[29:24,21:16] can still be connected to the FPGA fabric. In this example, both GPIO[29] and GPIO[28] are connected to the fabric as **Input** ports.

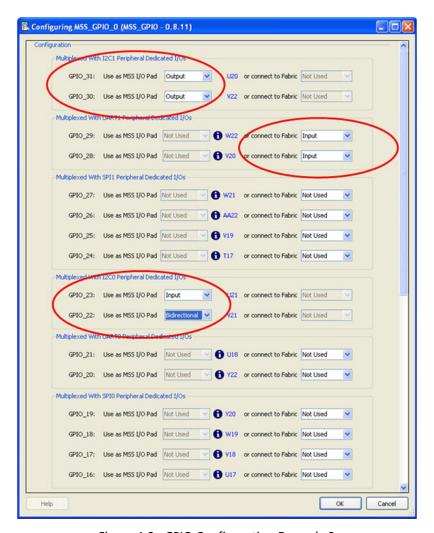


Figure 1-2 · GPIO Configuration Example 2

#### **GPIO[15:0]**

GPIO[15:0] share MSS I/Os that can be configured to connect to the FPGA fabric (this later configuration can be done using MSS I/O Configurator). If an MSS I/O is configured to connect to the FPGA fabric, then the MSS I/O Pad pull-down menu is grayed-out for the corresponding shared GPIOs and an Info icon is displayed next to the pull-down menu. The Info icon indicates that the MSS I/O option cannot be selected because it is already used or, based on the package selected, not bonded.

Note that the blue text in the configurator highlights the package pin name for each MSS I/O associated with a GPIO. This information is useful for planning board layout.

#### **Configuration Options**

#### **Example**

To properly demonstrate how the MSS I/O configurations and the GPIO[15:0] configurations are coupled, Figure 1-3 shows both configurators side by side with the following configuration:

- MSS I/O[15] is used as an INBUF port connected to the FPGA fabric. Consequently, GPIO[15] cannot be connected
  to an MSS I/O.
- GPIO[5] is connected to an MSS I/O as an Input. Consequently MSS I/O[5] cannot be used to connect to the FPGA fabric.
- GPIO[3] is connected to the FPGA fabric as an Output. Consequently MSS I/O[3] cannot be used to connect to the FPGA fabric.

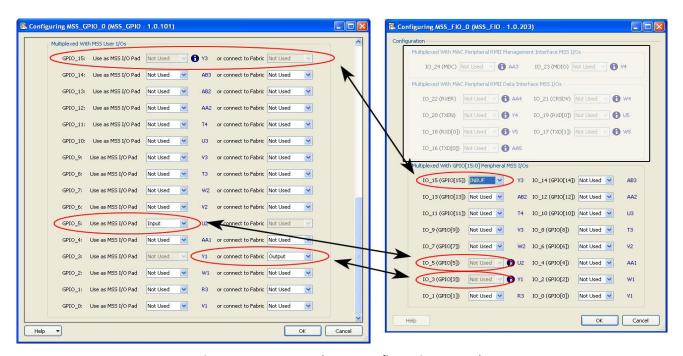


Figure 1-3 · MSSIO and GPIO Configuration Example



# **Port Description**

Table 2-1 · GPIO Port Description

Port Name	Direction	PAD?	Description	
GPIO_ <index>_IN</index>	In	Yes	GPIO port name when GPIO[index] is configured as an MSS I/O Input port	
GPIO_ <index>_OUT</index>	Out	Yes	GPIO port name when GPIO[index] is configured as an MSS I/O Output port	
GPIO_ <index>_TRI</index>	Out	Yes	GPIO port name when GPIO[index] is configured as an MSS I/O Tristate port	
GPIO_ <index>_BI</index>	Inout	Yes	GPIO port name when GPIO[index] is configured as an MSS I/O Bidirectional port	
F2M_GPI_ <index></index>	In	No	GPIO port name when GPIO[index] is configured to connect to the FPGA fabric as an Input port (F2M indicates that the signal is going from the fabric to the MSS)	
M2F_GPO_ <index></index>	In	No	GPIO port name when GPIO[index] is configured to connect to the FPGA fabric as an Output port (M2F indicates that the signal is going from the MSS to the fabric)	

#### Note:

- $\bullet\;$  PAD ports are automatically promoted to top throughout the design hierarchy.
- Non-PAD ports must be promoted manually to the top level from the MSS configurator canvas to be available as the next level of hierarchy.





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