SmartDesign MSS

Ethernet MAC Configuration

Microsemi

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Configuration Options

The SmartFusion Microcontroller Subsystem (MSS) provides one Ethernet MAC hard peripheral.

The actual behavior of the Ethernet MAC must be defined at the application level using the SmartFusion MSS MAC Driver provided by Actel.

In this document, we describe how you can enable the MSS MAC instance and select whether the Ethernet MAC interface is connected to dedicated MSS I/Os or the FPGA fabric.

For more details about the MSS MAC hard peripheral, please refer to the Actel SmartFusion Microcontroller Subsystem User's Guide.

Enabling/Disabling the MAC Instance - On the MSS canvas, you need to enable (default) or disable the MAC instance (Figure 1) based on whether it is being used into your current application. If disabled, the MAC instance is held in reset (lowest power state) after the Actel system boot code is executed.

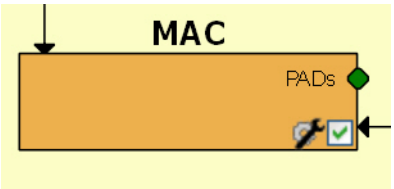

***Figure 1* • MSS MAC Configurator**

Connectivity Options - The MSS Ethernet MAC interface has been split into two groups - RMII Phy Management Interface and RMII Data Interface - (see "Port Description" on page 5 for the detailed port assignments).

You can choose to connect each group separately to either MSS I/Os or to the FPGA fabric as shown in Figure 2.

When using the A2F200M3F device you cannot connect the RMII Phy Management Interface to the FPGA fabric. This restriction does not exist for the A2F500M3G device. In all cases, the Ethernet MAC connectivity is automatically configured by the Actel system boot code.

MSS I/Os allocated to the MAC instance are available to connect to the FPGA fabric if the MAC instance is disabled. Refer to the MSS I/O Configuration document for more details. The MAC group ports are automatically promoted to the top level of the MSS Configurator Canvas so that they are available at the next level of hierarchy.

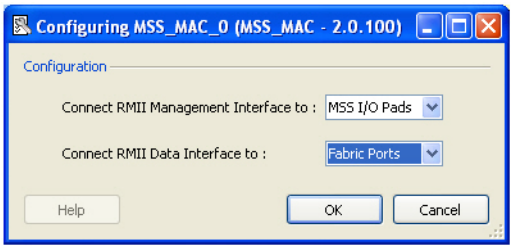

***Figure 2* • MSS MAC Configuration Options**

Rule1 - You cannot use the RMII Management Interface (MDIO, MDC) if any of the corresponding MSS I/Os are being used in the MSS I/O configurator. The following message is displayed in the Warning icon tool tip:

> The RMII Management Interface cannot be selected because the corresponding MSS I/Os have been selected in the MSS I/O configurator

Rule2 - You cannot connect the RMII Management Interface to the FPGA fabric if the MSS I/O IO_22(RXER) has been selected in the MSS I/O configurator. This is related to the RXER/MDEN IOMUX sharing in the architecture. The following message is displayed in the Warning icon tool tip:

> RMII Management Interface connection to the FPGA fabric is not selectable when IO_22(RXER) has been selected in the MSS I/O configurator

Rule3 - You cannot connect the RMII Data Interface (TXD, RXD, TXEN, RXER and CRSDV) to MSS I/Os if any of the corresponding MSS I/Os are being used in the MSS I/O configurator. The following message is displayed in the Warning icon tool tip:

> The RMII Data Interface cannot be connected to MSS I/Os because the corresponding MSS I/Os have been selected in the MSS I/O configurator

Rule4 - You cannot connect the RMII Data Interface (TXD, RXD, TXEN, RXER and CRSDV) to the FPGA fabric if any of the corresponding MSS I/Os are being used in the MSS I/O configurator and the direction of the MSS I/O is not compatible with the MAC port direction (Table 1). The following message is displayed in the Warning icon tool tip:

> The RMII Data Interface cannot be connected to the fabric because the corresponding MSS I/Os selected in the MSS I/O configurator are not compatible in direction with this option

Table 1 • **MAC and MSS I/O Compatibility**

MAC Ports		MSS I/O	
Port	Direction	Port	Compatible Direction
TXD[0]	Output	IO_16	OUTBUF, TRIBUFF
TXD[1]	Output	IO_17	OUTBUF, TRIBUFF
RXD[0]	Input	IO_18	INBUF
RXD[1]	Input	IO_19	INBUF
TXEN	Output	IO_20	OUTBUF, TRIBUFF
CRSDV	Input	IO_21	INBUF
RXER	Input	IO_22	INBUF

Ethernet MAC Clock Selection - If you enable the MAC peripheral on the MSS configurator canvas the MAC clock is automatically selected (read-only) in the Clock configurator. If you use the MSS Clock Configurator you need to select one of the following MAC clock sources.

- The external 10/100 clock (MAC_CLK pin) on the SmartFusion device.
- A clock generated in the MSS Clock Conditioning Circuit (MSS_CCC).

Port Description

Table 2 • **MSS I/O Connectivity Options**

Port Name	Port Group	Direction	PAD?	Description
MDIO	RMII_PHY_MGMT_PADs	INOUT	Yes	RMII management data input and output. The state of the input signal can be checked by reading the CSR9.19 bit. The output signal is driven by the CSR9.18 bit.
MDC	RMII_PHY_MGMT_PADs	OUT	Yes	RMII management clock = 50 MHz. This signal is driven by the CSR9.16 bit.
RXER	RMII_DATA_PADs	IN	Yes	Receive error. If RX_ER is asserted during Ethernet MAC reception, the frame is received and status of the frame is updated with RX_ER.
CRSDV	RMII_DATA_PADs	IN	Yes	Carrier sense and receive data valid. This signal must be asserted by the PHY when either a receive or transmit medium is non-idle. The PHY device should assert MAC_CRSDV when valid data is provided on the RXD signal.
RXD[1:0]	RMII_DATA_PADs	IN	Yes	Receive data recovered and decoded by PHY. The RXD[0] signal is the least significant bit.
TXEN	RMII_DATA_PADs	OUT	Yes	Transmit enable. When asserted, indicates valid data for the PHY on the TXD port.
TXD[1:0]	RMII_DATA_PADs	OUT	Yes	Transmit data. The TXD[0] signal is the least significant bit.

Table 3 • **FPGA Fabric Connectivity Options**

Port Name	Port Group	Direction	PAD?	Description
F2M_MDI	RMII_PHY_MGMT_FAB	IN	No	RMII management data input. The state of the input signal can be checked by reading the CSR9.19 bit
M2F_MDIO	RMII_PHY_MGMT_FAB	OUT	No	RMII management data output. The output signal is driven by the CSR9.18 bit.
M2F_MDC	RMII_PHY_MGMT_FAB	OUT	No	RMII management clock = 50 MHz. This signal is driven by the CSR9.16 bit.
F2M_RXER	RMII_DATA_FAB	IN	No	Receive error. If RX_ER is asserted during Ethernet MAC reception, the frame is received and status of the frame is updated with RX_ER.
F2M_CRSDV	RMII_DATA_FAB	IN	No	Carrier sense and receive data valid. This signal must be asserted by the PHY when either a receive or transmit medium is non-idle. The PHY device should assert MAC_CRSDV when valid data is provided on the RXD signal.
M2F_MDEN	RMII_DATA_FAB	OUT	No	RMII management data output enable.
F2M_RXD[1:0]	RMII_DATA_FAB	IN	No	Receive data recovered and decoded by PHY. The RXD[0] signal is the least significant bit.
M2F_TXEN	RMII_DATA_FAB	OUT	No	Transmit enable. When asserted, indicates valid data for the PHY on the TXD port.
M2F_TXD[1:0]	RMII_DATA_FAB	OUT	No	Transmit data. The TXD[0] signal is the least significant bit.

Note: PAD ports are automatically promoted to top throughout the design hierarchy.

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