Libero SoC v11.8 Programming and Debug Tools Release Notes

03/2017

Microsemi
Power Matters.™

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Fax: +1 (949) 215-4996
Email: sales.support@microsemi.com
www.microsemi.com

About Microsemi
Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions; security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, California, and has approximately 4,800 employees globally. Learn more at www.microsemi.com.

51300169-1/03.17

Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision 1.0

Revision 1.0 is the first publication of this document.

Contents

1 Libero SoC v11.8 Programming and Debug Tools Release Notes

Starting with v11.7, Microsemi introduces a new Programming and Debug Tools installer. This installer is intended for laboratory and production environments where Libero is not installed, and allows you to install the following tools:

- FlashPro/FlashPro Express v11.8
- SmartDebug Standalone v11.8
- Job Manager v11.8 (required component of Microsemi's Secure Production Programming Solution (SPPS), which enables customers to prevent overbuilding of their systems)

These tools are also available with the full Libero SoC v11.8 release.

SmartDebug v11.8 includes the following new features and enhancements:

- FPGA Hardware Breakpoint (FHB) Auto Instantiation feature for SmartFusion2 and IGLOO2 devices in the Enhanced Constraint Flow
- Event Counter
- Frequency Monitor
- User Clock Frequencies Meter, available when FHB is instantiated
- Fabric SRAM Memory Logical View – SmartDebug infers, from flattened netlist, the user Logical definition of uSRAM or LSRAM in a design
- Multiple Lane PRBS Test – allows the user to run the same PRBS test on multiple lanes in a SERDES block
- Active Probe polling – allows the user to select active probe signals to continuously poll for a specified value
- Runtime Improvements

About Libero

Microsemi Libero® System-on-Chip (SoC) design suite offers high productivity with its comprehensive, easy-to-learn, easy-to-adopt development tools for designing with Microsemi's power-efficient flash FPGAs, SoC FPGAs, and rad-tolerant FPGAs. The suite integrates industry-standard synthesis and simulation tools—Synopsys Synplify Pro® and Mentor Graphics ModelSim, respectively—with best-in-class constraints management, debug capabilities, and secure production programming solution.

Libero SoC v11.8 can be used for designing with Microsemi RTG4 Rad-Tolerant FPGAs, SmartFusion2 and SmartFusion® SoC FPGAs, IGLOO®2, IGLOO, ProASIC3®, and Fusion® FPGA families.

To access datasheets, silicon user guides, tutorials, and application notes, visit www.microsemi.com, navigate to the relevant product family page, and click the **Documentation** tab. Development Kits & Boards are listed in the **Design Resources** tab.

Contents

2 What's New in Libero 11.8

2.1 Silicon Feature

No new silicon part is introduced with this release.

2.2 Software Enhancements

Unless otherwise noted, Software Enhancements apply to all SmartFusion2, IGLOO2, and RTG4 devices.

.

2.2.1 SmartDebug: FPGA Hardware Breakpoint, SRAM Logical View, Multiple Lane PRBS Test, Polling

The SmartDebug tool in Libero SoC v11.8 has been enhanced with significant new features.

FPGA Hardware Breakpoint (SmartFusion2 and IGLOO2) - You can automatically instantiate the FPGA Hardware Breakpoint (FHB) module into the user design. This feature is available in the Enhanced Constraint Flow only.

- FHB allows you to select any probe point (via Live-probe feedback) as a trigger to halt the design, and then single-step your design using SmartDebug.
- You can configure FHB to wait for up to 255 user clock cycles after the trigger event is detected before the user clock is halted. The trigger event occurs on the rising edge of the trigger signal selected by the user.
- SmartDebug allows you to:
    - Capture and collect multiple snapshots using the **read_active_probe** Tcl command.
    - Export a VCD waveform file of the selected signals. You can then review the waveform using any waveform viewer that supports VCD file format.
    - Initialize the selected probe points by using the **write_active_probe** Tcl command or the Active Probe GUI before advancing the user clock.
- The FHB module instantiated by the tool includes the Event Counter and the Frequency Meter. The Event Counter is a 32-bit counter that keeps track of the number of times the rising edges have been detected on the selected probe point. The Frequency Meter estimates the frequency of the user clocks, as well as any selected probe points.

See the SmartDebug for Libero SoC v11.8 User Guide for details.

Fabric SRAM Memory Logical View - In addition to the physical view, SmartDebug now supports the logical view of LSRAM and uSRAM as defined by the user through inference from the flattened netlist.

Multiple Lane PRBS Test - You can run the same PRBS test on multiple lanes in a SERDES block.

Active Probe Polling - This feature allows the tool to read iteratively a selected signal or bus until a specified value is read via Active Probe or a maximum count of iterations has been reached.

Runtime Improvements - Faster response time for Add/Delete Probes operations for very large designs.

2.2.2 Secure Production Programming Solution (SPPS): Design Security PUF Keys

Libero SoC v11.8 SPPS adds support for Design Security PUF Keys in M2S060, M2S090, M2S150, M2GL060, M2GL090, and M2GL150 devices.

- Factory PUF ECC key – enables secured production programming at contract manufacturing site without DFK database.
- User PUF AES key – User Encryption Key 3 (UEK3). This support is added to both SPPS flow and non-SPPS flow. The supported use cases are the same as the use cases in UEK1 and UEK2 in both flows. Similar to UEK1 and UEK2, UEK3 can be:
    - Provided by the user in the Security Policy Manager in Libero SoC.
    - Used to encrypt the update bitstream when generating STAPL, SPI, and DAT bitstream files.
    - Injected into the device at the same time UEK1 and UEK2 is programmed via SPPS flow or non-SPPS flow.

  UEK3 is supported in Libero SoC, FlashPro Express, and Job Manager.

  Note: DirectC support for UEK3 is not yet available.

2.2.3 New Operating System Support

Libero SoC v11.8 adds the support of the following Operating Systems:

- Windows 10
- RHEL 7
- CentOS 7

3 Resolved Issues

The following table lists the customer-reported SARS Resolved in Libero SoC v11.8.

Customer Case Number	Description
493642-2046740027	Generating a SVF file with only Erase and Program Array using Designer
493642-2195062181	G4 programming recovery failure when power cut at certain times
493642-2166423130	STAPL JESD71 Standard
493642-2121872068	Programming fails with IDE9.1 PDB file but passes with IDE9.1 STP
493642-2007160699	Improve options naming under Debug security policy (SF2)
493642-1996472989	Backlevel Protection in Update Policy should give some information once enabled
493642-1843877113	Documentation: Debug Security Policy help is not complete
493642-1506975832, 493642-1609820607, 493642-1622538232	Export Active Probe and Memory content from GUI to file
493642-2072395998/493642-2011990594	Support for write count threshold check in SVF
493642-2102623482	Change FP5 Vpump detection level to match with FP4
493642-2246593390	A multi-pass P&R job does not stop with the Stop button
	UJTAG change to support Dual Use case
	Add a phrase in the menu to indicate JTAG mode only
	SPPS: JobManager needs to add support for eNVM placeholder clients
	SPPS: Add TCL to delete ticket by its ID for all SPPS flows (including IHP)
	Active Probe/Live Probe does not work on M2GL150 design/device
	Active Probe : Allow multiple writes of same value to same signal
	Need to add sorting capability to probe insertion selected nets

4 Known Limitations, Issues, and Workarounds

4.1.1 RTG4 - SmartDebug: Device Resets during JTAG Operations with SmartDebug

If the SmartDebug tool (either standalone or within the Libero SoC software) is closed and reopened after performing one or more JTAG operations, the device resets itself.

Workaround:

The device reset problem can be avoided by using the FlashPro5 programmer and setting a value of **1** on the def variable **SMARTDEBUG_RTG4_FLASHPRO5_DISABLE_RESET.**

- For standalone SmartDebug:
  - When invoking the tool from the command line, add the following argument:

    Console >

    ./sdebug.exe **SMARTDEBUG_RTG4_FLASHPRO5_DISABLE_RESET**:1
  - When invoking the tool from the GUI, edit the sdebug.def file and change the value of def variable to '1' in the line below:

    data SMARTDEBUG_RTG4_FLASHPRO5_DISABLE_RESET 0 OVERRIDE
- For SmartDebug invoked from Libero SoC:
  - Edit the sdbg.def file and change the value of def variable to "1" in the line below:

    data SMARTDEBUG_RTG4_FLASHPRO5_DISABLE_RESET 0 OVERRIDE
  - Add the following line in the libero.def file:

    data SMARTDEBUG_RTG4_FLASHPRO5_DISABLE_RESET 1 OVERRIDE
- For Tcl script-driven batch mode operation, add the following def variable and the value in a Tcl script:

  defvar_set -name **SMARTDEBUG_RTG4_FLASHPRO5_DISABLE_RESET** -value 1

Note: When the def variable is set to 1, the LiveProbe set in the previous SmartDebug session is not retained when a subsequent SmartDebug session is invoked.

4.1.2 SmartFusion2/IGLOO2 and RTG4 – SmartDebug Error when Probe Points Exceeds 1000

When more than 1000 probe points belonging to a bus are selected from the Hierarchical view and added to the Live/Active Probes tab, SmartDebug issues the SQL error: "Expression tree is too large (maximum depth 1000)".

4.1.3 SmartDebug – Logical View for LSRAM/uSRAM Known Issues

The following SmartDebug known issues will be fixed in the next release.

- Logical view cannot be reconstructed for LSRAM/uSRAM for port widths of x1 inferred through RTL.
- Logical view cannot be reconstructed for LSRAM/uSRAM configurations when a single net of output bus is used, i.e. A_DOUT[0]/B_DOUT[0] for DPSRAM/uSRAM and RD[0] for TPSRAM and others are unused. The memories can be read/write using physical view.

- Logical view cannot be reconstructed for LSRAM/uSRAM configurations inferred using IP Cores CoreAHBLtoAXI (Verilog flow), CoreFIFO (Verilog and VHDL flow).

4.1.4 SmartDebug – FPGA Hardware Breakpoint (FHB) Auto Instantiation Limitations

- Support is limited to SmartFusion2 and IGLOO2 devices in the Enhanced Constraint Flow only.
- Support is limited to FABCCC driven gated clocks.
- There is no support for EDIF flow and designs having Encrypted IPs.
- Live Probe triggering occurs on the Positive Edge only.
- When a signal connected to logic zero/ground (1'b0) is used as the live probe trigger, disarming the trigger leads to forced halt of DUT.
- FHB auto instantiation feature is not supported for block flow.

4.1.5 Programming - Libero SoC Crashes when Exporting FlashPro Express Job for UEK1 or UEK2 with eNVM

Libero SoC crashes when the Export FlashPro Express Job tool is invoked to generate a programming job encrypted using UEK1/UEK2 where eNVM is the only selected component.

Workaround:

Select both fabric and eNVM components for exporting the programming job encrypted using UEK1 or UEK2.

4.1.6 Programming - SPPS Flow: export_hsmtask fails when set_security_overwrite is followed by set_envm_update

If the user Tcl script has the security overwrite command followed by the eNVM update command, the export of the HSM job fails. In other words, if set_security_overwrite is followed by set_envm_update, the export_hsmtask fails.

Workaround:

If both the security overwrite command and the eNVM update command are required, make sure that the eNVM update command is executed prior to the security overwrite command. Put the set_envm_update Tcl command before the set_security_overwrite Tcl command in the Tcl script.

4.1.7 Programming - No Programming Support for Virtual Machines

Programming is supported for physical machines only and is not supported on any virtual machine (VM).

4.1.8 Programming - Inspect Device Feature Disabled in FlashPro

The Inspect Device feature is disabled in FlashPro for SmartFusion2/IGLOO2 devices beginning with the Libero SoC v11.7 release. Use standalone SmartDebug instead.

4.1.9 Programming - SmartFusion Encrypted STP File Generation

Generating the encrypted STP files for SmartFusion takes 50 times longer than generating the non-encrypted plain STP.

4.1.10 ProASIC3 Devices Programming Action Failed

When programming a ProASIC3 device, the message “Error: A programming file must be loaded before running the command set_program_action” appears.

Workaround:

1. Export the PDB/STAPL file from Libero.
2. Open FlashPro and load the programming file to run programming.

4.1.11 SoftConsole - Restricts ARM® Cortex®-M3 Debug with Debug Pass Key

SoftConsole does not support this feature.

4.1.12 Documentation - Web-based Documentation

Starting with the Libero SoC v11.7 release, most users guides for SmartFusion2, IGLOO2, and RTG4 are available on the Microsemi website. Libero SoC and Programming/Debug tools include links to the website.

If the machine on which the Libero SoC software is installed does not have access to the internet, you (or a site administrator) can download all the Libero SoC v11.7 user guides from the Libero SoC documentation site.

4.1.13 Documents on Linux: Firefox Requirement for Online Help and User Guides

Libero SoC v11.8 requires the “Firefox” executable to be in your PATH variable on Linux. Alternatively, you can access the reference manuals on the Microsemi website, or by clicking **Help > Reference Manuals** in Libero SoC. For the Libero SoC SoC v11.8 release, the “Web Browser” selection in the Libero SoC Preferences dialog box is only used by online help and for some user guide links.

4.1.14 Installation

C++ installation error can be ignored. Required files will install successfully.

On some machines, the InstallShield wizard displays a pop-up message stating:

The installation of Microsoft Visual C++ Redistributable Package (x86) appears to have failed. Do you want to continue the installation?

Click **Yes** to complete the installation.

4.1.15 Antivirus Software Interaction

Many antivirus and host-based intrusion prevention system (HIPS) tools flag executables and prevent them from running. To eliminate this problem, users must modify their security settings by adding exceptions for specific executables. This is configured in the antivirus tool. Contact the tool provider for assistance.

Many users are running Libero SoC successfully with no modification to their antivirus software. Symantec, McAfee, Avira, Sophos, and Avast tools have known issues. The combination of operating system, antivirus tool version, and security settings all contribute to the end result. Depending on the environment, the operation of Libero SoC, ModelSim ME, and/or Synplify Pro ME may or may not be affected.

4.1.16 Installation Issue on Linux

After installation of Libero SoC on Linux, the attempt to run the udev_install script for FlashPro setup fails with the following message:

```
% ./udev_install
/bin/sh^M: bad interpreter: No such file or directory
```

Problem:

The script uses Windows CR/LF line termination instead of UNIX/Linux LF only line termination and, hence, is not a valid shell script.

Workaround:

Run the `dos2unix` command on the script to convert CR/LF line termination to LF only line termination:

```
% dos2unix udev_install
%. /udev_install
```

If the `dos2unix` command is not available, install the command first, and then run `dos2unix`, and `udev_install`:

```
% sudo yum install dos2unix
% dos2unix udev_install
%. /udev_install
```

5 System Requirements

For information about operating system support and minimum system requirements, see the System Requirements web page.

Note: A 64-bit OS is required for designing with SmartFusion2, IGLOO2, and RTG4 devices.

For Linux OS setup instructions, see the Libero SoC Documents web page.

5.1.1 Operating System Support

Supported

- Windows 7, Windows 8.1, Windows 10*
- RHEL 5** and RHEL 6, CentOS 5**, and CentOS 6, RHEL 7* and CentOS 7*
- SuSE 11 SP4 (Libero only. FlashPro Express, SmartDebug, and Job Manager are not supported.)

Note: * New OS support for this release.

** RHEL 5 and CentOS 5 do not support programming using FlashPro5.

Not Supported

- 32-bit operating system
- Windows XP
- Support for the following operating systems will cease in the second half of 2017:
    - RedHat Enterprise Linux 5.x through 6.5
    - CentOS 5.x through 6.5

6 Download Libero SoC v11.8 Programming and Debug Tools

Click the following links to download Libero SoC v11.8 Programming and Debug Tools on Windows and Linux operating systems:

- Windows Download
- Linux Download

Note: Installation requires administrator privileges to the system.