Libero® SoC v2021.1

PDC Commands Reference Guide for PolarFire® and PolarFire SoC FPGAs

Introduction

In the FPGA design world, constraint files are as important as design source files. Physical design constraints (PDC) are used to constrain I/O attributes, placement, and routing during the physical layout phase.

You can enter PDC commands manually using the Libero® SoC Text Editor. PDC commands can also be generated by the Libero SoC interactive tools. The I/O Attribute Editor is the interactive tool for making I/O attributes changes and the Chip Planner is the interactive tool for making floor-planning changes. When changes are made in the I/O Attribute Editor or the Chip Planner, the PDC file(s) are updated to reflect these changes. These PDC commands can be used as part of a script file to constrain the Place and Route step of your design.

Table of Contents

1. About PDC Commands

The following sections describe PDC/NDC commands and families.

1.1 Supported Families

This user guide describes the I/O and Floorplanning PDC commands applicable to PolarFire® and PolarFire SoC FPGA devices.

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1.2 I/O PDC Commands

I/O PDC commands are used to set and reset I/O standards, voltage values, and attributes.

For detailed information about I/Os and I/O standards, refer to the UG0686: PolarFire FPGA User I/O User Guide.

1.3 PDC Syntax Conventions

The following table shows the typographical conventions that are used for the PDC command syntax.

Table 1-1. Typographical Conventions Used for the PDC Command Syntax

Syntax Notation	Description
`command -argument`	Commands and arguments appear in Courier New typeface.
[-argument value]	Optional arguments begin and end with a square bracket.

Note: PDC commands and arguments are case sensitive.

1.3.1 Examples

Syntax for the `set_io` command followed by a sample command starting with `set_io EXT_RST_N \`:

Syntax: `-port_name <port_name> [-pin_name <package_pin>] [-fixed <true|false>] [-io_std <io_std_values>] [-OUT_LOAD <value>] [-RES_PULL <value>] [-LOCK_DOWN <value>] [-CLAMP_DIODE <value>] [-SCHMITT_TRIGGER <value>] [-SLEW <value>] [-VCM_RANGE <value>] [-ODT <value>] [-ODT_VALUE <value>] [-OUT_DRIVE <value>] [-IMPEDANCE <value>] [-SOURCE_TERM <value>] [-IN_DELAY <value>] [-OUT_DELAY <value>]`

Sample command 1:

```
set_io -port_name EXT_RST_N \
-pin_name AD4 \
-fixed true \
-io_std LVCMOS15 \
-IN_DELAY 6 \
-LOCK_DOWN Yes \
-ODT ON \
-ODT_VALUE 240 \
-RES_PULL Down \
```

```
-SCHMITT_TRIGGER ON \
-DIRECTION INPUT
```

Sample command 2:

```
set_io -port_name TX \
-io_std LVCMOS12 \
-OUT_DELAY 8 \
-OUT_DRIVE 10 \
-RES_PULL Hold \
-DIRECTION OUTPUT
```

1.3.2 Wildcard Characters

You can use the following wildcard characters in names used in PDC commands:

Table 1-2. Wildcard Characters in Names Used in PDC Commands

Wildcard	What It Does
\	Interprets the next character literally.
?	Matches any single character.
*	Matches any string.

Note: The matching function requires that you add a slash (\) before each slash in the port, instance, or net name when using wildcard in a PDC command.

1.3.3 Special Characters ([ ], { }, and \)

Sometimes square brackets are part of the command syntax. In these cases, you must either enclose the open and closed square brackets characters with curly brackets or precede the open and closed square brackets characters with a backslash (\). Otherwise, you will receive an error message.

For example:

```
set_io -port_name {P12}
```

Note:
Do not add spaces between in {}. For example: {PORT1} will succeed and { PORT1 } will not.

1.3.4 Entering Arguments on Separate Lines

To enter an argument on a separate line, must enter a backslash (\) character at the end of the preceding line of the command as shown in the following example:

```
set_io ADDOUT2 \
-iostd PCI \
-port_name \
-out_drive 16 \
-slew High \
-out_load 10 \
-pin_name T21 \
-fixed yes
```

1.4 PDC Naming Conventions

Note: The names of ports, instances, and nets in an imported netlist are sometimes referred to as their original names.

1.4.1 Rules for Displaying Original Names

Port names appear exactly as they are defined in a netlist.

Instances and nets display the original names plus an escape character (\) before each backslash (/) and each slash (\) that is not a hierarchy separator. For example, the instance named A/\B is displayed as A\/\\B.

1.4.2 Which Name Do I Use in PDC Commands?

When writing PDC commands, follow these rules:

- Always use the macro name as it appears in the netlist.
- Names from a netlist: For port names, use the names exactly as they appear in the netlist. For instance and net names, add an escape character (\) before each backslash (\) and each slash (/) that is not a hierarchy separator.
- For wildcard names, always add an extra backslash (\) before each backslash.
- Always apply the PDC syntax conventions to any name in a PDC command.

The following table provides examples of names as they appear in an imported netlist and the names as they should appear in a PDC file.

Table 1-3. Sample Names in an Imported Netlist and PDC File

Type of Name and Its Location	Name in the Imported Netlist	Name to Use in PDC File
Port name in a netlist	A/:B1	A/:B1
Instance name in a netlist	A/:B1 A$(1)	A\/:B1 A$(1)
Instance name in the netlist but using a wildcard character in a PDC file	A/:B1	A\\\/:B*
Net name in a netlist	Net1/:net1	Net1\\/:net1

When exporting PDC commands, the software always exports names using the PDC rules described in this section.

1.4.3 Case Sensitivity When Importing PDC Files

The following table shows the case sensitivity in the PDC file based on the source netlist.

Table 1-4. Case Sensitivity in the PDC File Based on a Source Netlist

File Type	Case Sensitivity
Verilog	Names in the netlist are case sensitive.
VHDL	Names in the netlist are not case sensitive unless those names appear between slashes (\).

For example, in VHDL, capital “A” and lowercase “a” are the same name, but \A\ and \a\ are two different names. However, in a Verilog netlist, an instance named “A10” will fail if spelled as “a10” in the `set_io` command:

`set_io -port_name A10 -pin_name W5` (This command will succeed.)

2. I/O PDC Commands

I/O PDC commands are used to set and reset I/O standards, voltage values, and attributes.

For detailed information about I/Os and I/O standards, refer to the UG0686: PolarFire FPGA User I/O User Guide.

2.1 set_iobank

This PDC command sets the input/output supply voltage (vcci) and the input reference voltage (vref) for the specified I/O bank.

All banks have a dedicated vref pin. Do not set any pin on these banks. There are two types of I/O banks:

- General-Purpose IO (GPIO)
- High-Speed IO (HSIO)

Each bank type supports a different set of I/O standards as listed in the following table.

Table 2-1. set_iobank Standards

I/O Types	Supported I/O Standards
HSIO	LVCMOS12, LVCMOS15, LVCMOS18, SSTL18I, SSTL18II, HSUL18I, HSUL18II, SSTL15I, SSTL15II, HSTL15I, HSTL15II, SSTL135I, SSTL135II, HSTL135I, HSTL135II, HSTL12I, HSTL12II, HSUL12I, SLVSE15, POD12I, POD12II, SLVS18, HCSL18, LVDS18, RSDS18, MINILVDS18, SUBLVDS18, PPDS18, SHIELD18, SHIELD15, SHIELD135, SHIELD12
GPIO	LVTTL, LVCMOS33, PCI, LVCMOS12, LVCMOS15, LVCMOS18, LVCMOS25, SSTL25I, SSTL25II, SSTL18I, SSTL18II, HSUL18I, HSUL18II, SSTL15I, SSTL15II, HSTL15I, HSTL15II, SLVS33, SLVS25, HCSL33, HCSL25, MIPI25, MIPIE25, LVPECL33, LVPECLE33, LVDS25, LVDS33, RSDS25, RSDS33, MINILVDS25, MINILVDS33, SUBLVDS25, SUBLVDS33, PPDS25, PPDS33, SLVSE15, MLVDSE25, BUSLVDSE25, LCMDS33, LCMDS25, SHIELD33, SHIELD25, SHIELD18, SHIELD15, SHIELD12

The following provide examples of using the `set_iobank` command with the supported arguments described in the following sections.

```
set_iobank -bank_name <bank_name>\
[-vcci <vcci_voltage>]\
[-vref <vref_voltage>]\
[-fixed <value>]\
[-update_iostd <value>]\
[-auto_calib <value>]\
[-auto_calib_ramp_time <value>]
```

2.1.1 Arguments

-bank_name <*bank_name*>

Specifies the name of the bank. I/O banks are numbered 0 through N (bank0, bank1,...bankN). The number of I/O banks varies with the device. Refer to the datasheet for your device to determine how many banks it has.

-vcci <*vcci_voltage*>

Sets the input/output supply voltage. Enter one of the values in the following table.

Table 2-2. -vcci Values

Vcci Voltage	Compatible Standards
3.3 V	LVTTL, LVCMOS33, PCI, LVDS33, LVPECL33, LVPECLE33, SLVS33, HCSL33, RSDS33, MINILVDS33, SUBLVDS33
2.5 V	LVCMOS25, SSTL25I,SSTL25II, PPDS25, SLVS25, HCSL25, MLVDSE25, MINILVDS25, RSDS25, SUBLVDS25, LVDS25, MLVDSE25, BUSLVDSE25
1.8 V	LVCMOS18, SSTL18I, SSTL18II, HSUL18I, HSUL18II, SLVS18, HCSL18, LVDS18, RSDS18, MINILVDS18, SUBLVDS18, PPDS18
1.5 V	LVCMOS15, SSTL15I, SSTL15II, HSTL15I, HSTL15II, SLVSE15
1.35 V	HSTL135I, HSTL135II, SSTL135I, SSTL135II
1.2 V	LVCMOS12, HSUL12I, HSTL12I, POD12I, MIPI12

-vref <*vref_voltage*>

Sets the input reference voltage. Enter one of the values in the following table.

Table 2-3. -vref Values

Vref Voltage	Compatible Standards
1.25 V	SSTL25I
1.0 V	SSTL18I,HSUL18I
0.75 V	POD12I, HSTL15I, SSTL15I, HSUL12I, HSTL12I
0.67 V	SSTL135I, HSTL135I

-fixed <*value*>

Specifies whether the I/O technologies (vcci and vccr voltages) assigned to the bank are locked. Enter one of the values in the following table.

Table 2-4. -fixed Values

Value	Description
true	The technologies are locked.
false	The technologies are not locked.

-update_iostd <*value*>

For I/Os placed on the bank, this command specifies whether placement is kept and the host is changed to one that is compatible with this bank setting.

Table 2-5. -update_iostd Values

Value	Description
true	If there are I/Os placed on the bank, we keep the placement and change the host to one that is compatible with this bank setting. Check the I/O attributes to see the one used by the tool.
false	If there are I/Os placed and locked on the bank, the command will fail. If they are placed I/Os they will be unplaced.

-auto_calib <*value*>

Specifies whether the I/O bank is auto-calibrated at power up. Values are true or false. The default value is true.

Note: This argument is not supported for MPF300TS_ES, MPF300T_ES, and MPF300XT devices.

-auto_calib_ramp_time <*value*>

Specifies the I/O bank VDDI supply ramp time (in ms) if the I/O bank is auto-calibrated. Values can be 1–50. The default value is 50.

Note: Not supported for MPF300TS_ES, MPF300T_ES, and MPF300XT devices.

2.1.2 Exceptions

Any pins assigned to the specified I/O bank that are incompatible with the default technology are unassigned.

2.1.3 Examples

The following example assigns 3.3 V to the input/output supply voltage (vcci) for I/O bank 0.

```
set_iobank -bank_name bank0 -vcci 3.3
```

2.2 reserve

This PDC command reserves the named pins in the current device package.

```
reserve -pin_name "list of package pins"
```

2.2.1 Arguments

-pin_name "*list of package pins*"

Specifies the package pin name(s) to reserve. You can reserve one or more pins.

2.2.2 Exceptions

None

2.2.3 Examples

```
reserve -pin_name "F2"
```

```
reserve -pin_name "F2 B4 B3"
```

```
reserve -pin_name "124 17"
```

2.3 set_io

The `set_io` command assigns an I/O technology, places, or locks the I/O at a given pin location. Two I/O types are available for PolarFire:

- GPIO
- HSIO

Each I/O type supports different I/O standards.

Table 2-6. set_io Standards

I/O Types	Supported I/O Standards
HSIO	LVCMOS12, LVCMOS15, LVCMOS18, SSTL18I, SSTL18II, HSUL18I, HSUL18II, SSTL15I, SSTL15II, HSTL15I, HSTL15II, SSTL135I, SSTL135II, HSTL135I, HSTL135II, HSTL12I, HSTL12II, HSUL12I, SLVSE15, POD12I, POD12II, SLVS18, HCSL18, LVDS18, RSDS18, MINILVDS18, SUBLVDS18, PPDS18, LCMDS18, SHIELD18, SHIELD15, SHIELD135, SHIELD12
GPIO	LVTTL, LVCMOS33, PCI, LVCMOS12, LVCMOS15, LVCMOS18, LVCMOS25, SSTL25I, SSTL25II, SSTL18I, SSTL18II, HSUL18I, HSUL18II, SSTL15I, SSTL15II, HSTL15I, HSTL15II, SLVS33, HCSL33, HCSL25, MIPI25, MIPIE25, LVPECL33, LVPECL25, LVPECLE33, LVDS25, LVDS33, RSDS25, RSDS33, MINILVDS25, MINILVDS33, SUBLVDS25, SUBLVDS33, PPDS25, PPDS33, SLVSE15, MLVDSE25, BUSLVDSE25, LCMDS33, LCMDS25, SHIELD33, SHIELD25, SHIELD18, SHIELD15, SHIELD12

Note: LCMDS18 IOSTD is not supported for MPF300XT devices.

TThe following show the syntaxes for this command:

```
set_io
-port_name <port_name>\
[-pin_name <package_pin>] \
[-fixed <true|false>] \
[-io_std <io_std_values>] \
[-OUT_LOAD <value>] \
[-RES_PULL <value>] \
[-LOCK_DOWN <value>] \
[-CLAMP_DIODE <value>] \
[-SCHMITT_TRIGGER <value>] \
[-SLEW <value>] \
[-VCM_RANGE <value>] \
[-ODT <value>] \
[-ODT_VALUE] \
[-OUT_DRIVE <value>] \
[-IMPEDANCE <value>] \
[-SOURCE_TERM <value>] \
[-IN_DELAY <value>] \
[-OUT_DELAY <value>]
```

2.3.1 Arguments

-port_name <*port_name*>

Specifies the portname of the I/O macro.

-pin_name <*package_pin*>

Specifies the package pin name(s) on which to place the I/O.

-io_std <*value*>

Sets the I/O standard for this macro. If the voltage standard used with the I/O is not compatible with other I/Os in the I/O bank, assigning an I/O standard to a port will invalidate its location and automatically unassign the I/O.

The following table lists the supported values for -io_std and their corresponding I/O standards. Some I/O standards support only single I/O or differential I/Os, while others support both single and differential I/Os.

Table 2-7. -io_std Values and Corresponding I/O Standards

-io_std Value	I/O Standard	
	Single	Differential
LVTTL	YES	NO
LVCMOS33	YES	NO
LVCMOS25	YES	NO
LVCMOS18	YES	NO
LVCMOS15	YES	NO

.....continued

-io_std Value	I/O Standard	
	Single	Differential
LVCMOS12	YES	NO
PCI	YES	NO
POD12I	YES	YES
POD12II	YES	YES
PPDS33	NO	YES
PPDS25	NO	YES
PPDS18	NO	YES
SLVS33	NO	YES
SLVS25	NO	YES
SLVS18	NO	YES
HCSL33	NO	YES
HCSL25	NO	YES
HCSL18	NO	YES
SLVSE15	NO	YES
BUSLVDSE	NO	YES
BUSLVDSE25	NO	YES
MLVDSE	NO	YES
MLVDSE25	NO	YES
LVDS	NO	YES
LVDS25	NO	YES
LVDS18	NO	YES
BUSLVDS	NO	YES
BUSLVDSE25	NO	YES
MLVDS	NO	YES
MIPI25	NO	YES
MIPIE25	NO	YES
MIPIE33	NO	YES
MINILVDS	NO	YES
MINILVDS33	NO	YES
MINILVDS25	NO	YES
MINILVDS18	NO	YES
RSDS	NO	YES
RSDS33	NO	YES
RSDS25	NO	YES

.....continued

-io_std Value	I/O Standard	
	Single	Differential
RSDS18	NO	YES
LVPECL (only for inputs)	NO	YES
LVPECL33	NO	YES
LVPECLE33	NO	YES
HSTL15I	YES	YES
HSTL15II	YES	YES
HSTL135I	YES	YES
HSTL135II	YES	YES
HSTLI2I	YES	YES
HSTL12II	YES	YES
SSTL18I	YES	YES
SSTL18II	YES	NO
SSTL15I	YES	YES
SSTL15II	YES	NO
SSTL135I	YES	YES
SSTL135II	YES	YES
SSTL25I	YES	YES
SSTL25II	YES	YES
HSUL18I	YES	YES
HSUL18II	YES	YES
HSUL12I	YES	YES
HSUL12II	YES	YES
SUBLVDS33	NO	YES
SUBLVDS25	NO	YES
SUBLVDS18	NO	YES
LCMDS33	NO	YES
LCMDS25	NO	YES
LCMDS18	NO	YES
SHIELD33	YES	NO
SHIELD25	YES	NO
SHIELD18	YES	NO
SHIELD15	YES	NO
SHIELD135	YES	NO
SHIELD12	YES	NO

-fixed <*value*>

Specifies whether the location of this port is fixed (i.e., locked). Locked ports are not moved during layout. The default value is true. You can enter one of the following values:

Table 2-8. -fixed Values

Value	Description
true	The location of this port is locked.
false	The location of this port is unlocked.

-OUT_LOAD <*value*>

Sets the output load (in pF) of output signals. The default is 5.

Direction: Output

-RES_PULL <*value*>

Allows you to include a weak resistor for either pull-up or pull-down of the input and output buffers. Not all I/O standards have a selectable resistor pull option.

The following table shows the acceptable values for the -RES_PULL attribute for the input buffer.

Table 2-9. -RES_PULL Values (Input Buffer)

I/O Standard	Value	Description
LVCMOS25, LVCMOS33, LVTTL, PCI, LVCMOS18, LVCMOS15, LVCMOS12	Up	Includes a weak resistor for pull-up of the input buffer.
	Down	Includes a weak resistor for pull-down of the input buffer.
	Hold	Holds the last value.
	None	Does not include a weak resistor.

For I/O standards in the table above, the default is Up. For all other I/O standards, the value is None.

The default is None.

The following table shows the acceptable values for the -RES_PULL attribute for the output buffer.

Table 2-10. -RES_PULL Values (Output Buffer)

I/O Standard	Value	Description
LVCMOS25, LVCMOS33, LVTTL, PCI, LVCMOS18, LVCMOS15, LVCMOS12	Up	Includes a weak resistor for pull-up of the output buffer.
	Down	Includes a weak resistor for pull-down of the output buffer.
	None	Does not include a weak resistor.

For all I/O standards, the default value for output buffer is None.

Direction: Inout

-LOCK_DOWN <*value*>

Security feature that locks down the I/Os if tampering is detected. Values are ON and OFF. The default is OFF.

Direction: Inout

-CLAMP_DIODE <*value*>

Specifies whether to add a power clamp diode to the I/O buffer. This attribute option is available to all I/O buffers with I/O technology set to LVTTL. A clamp diode provides circuit protection from voltage spikes, surges, electrostatic discharge, and other over-voltage conditions.

Values are OFF and ON.

The following table lists the values for GPIO standards. For HSIO standards, the value is always ON.

Table 2-11. -CLAMP_DIODE Values

I/O Standard	Values
LVCMOS12, LVCMOS15, LVCMOS18, SSTL18I, SSTL18II, SSTL15I, SSTL15II, HSTL15I, HSTL15II, LVTTL, LVCMOS33, LVCMOS25, SSTL25I, SSTL25II, SLVS25, HCSL25, LVDS25, RSDS25, MINILVDS25, SUBLVDS25, PPDS25, LCMDS25	OFF, ON. The default is ON.
MIPI25	OFF, ON. The default is OFF.
HSUL18I, HSUL18II, SLVSE15, PCI, SLVS25, SLVS33, HCSL33, HCSL25, MIPIE33, MIPIE25, LVPECL33, LVPECL25, LVPECLE33, LVDS25, LVDS33, RSDS25, RSDS33, MINILVDS25, MINILVDS33, SUBLVDS25, SUBLVDS33, PPDS25, PPDS33, MLVDSE25, BUSLVDSE25, LCMDS25, LCMDS33	ON

Direction: Inout

-SCHMITT_TRIGGER <*value*>

Specifies whether this I/O has an input Schmitt trigger. The Schmitt trigger introduces hysteresis on the I/O input. This allows very slow moving or noisy input signals to be used with the part without false or multiple I/O transitions taking place in the I/O.

For the following I/O standards, the values are OFF and ON. The default is OFF.

Table 2-12. -SCHMITT_TRIGGER Values

I/O Standard	Values
GPIO	
LVCMOS25, LVCMOS33, LVTTL, PCI	OFF, ON
HSIO	
LVCMOS18, LVCMOS15	OFF, ON

For all other I/O standards, the value is OFF.

Direction: Input

-SLEW <*value*>

Sets the output slew rate. Slew control affects only the falling edges for some families. Slew control affects both rising and falling edges. Not all I/O standards have a selectable slew. Whether you can use the slew attribute depends on which I/O standard you have specified for this command.

The following I/O standards have values OFF and ON. The default is OFF.

Table 2-13. -SLEW Values

I/O Standard	Values
LVCMOS25, LVCMOS33, LVTTL, PCI	OFF, ON

For all other I/O standards, the value is OFF.

Direction: Output

-VCM_RANGE <*value*>

Sets the VCM input range.

The following table lists the supported values and I/O standards.

Table 2-14. -VCM_RANGE Values

I/O Standard	Values
GPIO	
HSTL15I, HSTL15II, HSUL18I, HSUL18II, SSTL15I, SSTL15II, SSTL18I, SSTL18II, SSTL25I, SSTL25II	MID
HCSL33, HCSL25, LVDS33, LVDS25, LVPECL33, LVPECLE33, MINILVDS33, MINILVDS25, MIPI25, MIPIE25, MLVDSE25, PPDS33, PPDS25, RSDS33, RSDS25, SLVS33, SLVS25, SLVSE15, BUSLVDSE25, SUBLVDS33, SUBLVDS25 Note: While assigning VCM input range for true differential I/Os in the same bank, a mix of MID, LOW values cannot be assigned for the I/Os. You can assign only MID or only LOW values for all differential I/Os in the same bank.	MID, LOW. The default is MID.
LCMDS33, LCMDS25	LOW
HSIO	
HSTL12I, HSTL12II, HSTL135I, HSTL135II, HSTL15I, HSTL15II, HSUL12I, HSUL18I, HSUL18II, LVSTL11I, LVSTL11II, POD12I, POD12II, SSTL135I, SSTL135II, SSTL15I, SSTL15II, SSTL18I, SSTL18II	MID
SLVSE15, LVDS18, HCSL18, MINILVDS18, PPDS18, RSDS18, SLVS18, SUBLVDS18 Note: While assigning VCM input range for true differential I/Os in the same bank, a mix of MID, LOW values cannot be assigned for the I/Os. You can assign only MID or only LOW values for all differential I/Os in the same bank.	MID, LOW. The default is MID.
LCMDS18	LOW

Direction: Input

-ODT <*value*>

On-die termination (ODT) is the technology where the termination resistor for impedance matching in transmission lines is located inside a semiconductor chip instead of on a printed circuit board.

Values are OFF and ON.

The following table lists acceptable values.

Table 2-15. -ODT Values

I/O Standard	Values
LVCMOS12, LVCMOS15, LVCMOS18, LVCMOS25, HSUL18I, HSUL18II	OFF, ON. The default is OFF.
SSTL15I, SSTL15II, SSTL18I, SSTL18II, HSUL12I, POD12I, POD12II, SSTL135I, SSTL135II, HSTL15I, HSTL15II, LVDS33, LVDS25, LVPECL33, LVPECLE33, LVPECL25, MINILVDS33, MINILVDS25, RSDS33, RSDS25, SUBLVDS33, SUBLVDS25, HSTL12I, HSTL12II, HSTL135I, HSTL135II, LCMDS33, LCMDS25	OFF, ON. The default is ON.

Direction: Input

-ODT_VALUE

Sets the ODT value in Ohms.

Values vary depending on the I/O standard. The following table lists acceptable values.

Table 2-16. -ODT_VALUE Values

I/O Standard	Values
LVCMOS12, LVCMOS15, LVCMOS18	120, 240. The default is 120.

.....continued	
I/O Standard	**Values**
LVCMOS25	120
HSUL12I	60, 120, 240. The default is 120.
SSTL15I, SSTL15II	20, 30, 40, 60, 120. The default is 30.
SSTL135I, SSTL135II	20, 30, 40, 60, 120. The default is 40.
SSTL18I, SSTL18II	50, 75, 150. The default is 50.
POD12I, POD12II	34, 40, 48, 60, 80, 120, 240. The default is 60.
LVDS33, LVDS25, LVPECL33, LVPECL25, MINILVDS33, MINILVDS25, RSDS33, RSDS25, SLVSE15, SUBLVDS33, SUBLVDS25,LCMDS33, LCMDS25	100
HSTL15I, HSTL15II, HSUL18I, HSUL18II, HSTL12I, HSTL12II, HSTL135I, HSTL135II	50

Direction: Inout

-OUT_DRIVE <*value*>

Sets the strength of the output buffer to 1.5, 2, 3.5, 4, 6, 8, 10, 12, 16, or 20 in mA, weakest to strongest. The list of I/O standards for which you can change the output drive and the list of values you can assign for each I/O standard is family-specific. Not all I/O standards have a selectable output drive strength.

Each I/O standard has a different range of legal output drive strength values. The values you can choose depend on which I/O standard you specified for this command. The following table lists acceptable values.

Table 2-17. -OUT_DRIVE Values

I/O Standard	Values
GPIO	
LVCMOS12	2, 4, 6, 8. Default is 8.
LVCMOS15	2, 4, 6, 8, 10. Default is 8.
LVCMOS18	2, 4, 6, 8, 10, 12. Default is 8.
LVCMOS25	2, 4, 6, 8, 12, 16. Default is 8.
LVCMOS33, LVTTL	2, 4, 8, 12, 16, 20. Default is 8.
LVDS25, LVDS33, MINILVDS25, MINILVDS33, LCMDS33, LCMDS25	3, 3.5, 4, 6. Default is 6.
PPDS25, PPDS33, RSDS25, RSDS33	1.5, 2, 3. Default is 3.
SUBLVDS25, SUBLVDS33	1, 1.5, 2. Default is 2.
BUSLVDSE25, MLVDSE25, LVPECLE33	16
MIPIE25, SLVSE15	8
PCI	20
HSIO	
LVCMOS12, LVCMOS15	2, 4, 6, 8, 10. Default is 8.
LVCMOS18	2, 4, 6, 8, 10, 12. Default is 8.
SLVSE15	8

Direction: Output

-IMPEDANCE

Sets the impedance value in Ohms.

Values vary depending on the I/O standard. The following table lists acceptable values.

Direction: Output

-SOURCE_TERM

Near-end termination for a differential output I/O. The following table lists acceptable values.

Table 2-18. -SOURCE_TERM Values

I/O Standard	Values
LVDS25, LVDS33, MINILVDS25, MINILVDS33, LCMDS33, LCMDS25, PPDS25, PPDS33, RSDS25, RSDS33, SUBLVDS25, SUBLVDS331	OFF, 100. The default is OFF.

Direction: Output

-IN_DELAY

Sets the input delay.

Input delay applies to all I/O standards. The values are OFF and 0-127, 128, 130, 132, ..., 254. The default value is OFF.

Direction: Input

Note: This attribute will not appear in the I/O attributes and cannot be used in the PDC for some I/Os with dynamic delays, such as DDR I/Os.

-OUT_DELAY

Sets the output delay.

Output delay applies to all I/O standards. The values are OFF and 0–127. The default value is OFF.

Direction: Output

Note: This attribute will not appear in the I/O attributes and cannot be used in the PDC for some I/Os with dynamic delays, such as DDR I/Os.

2.3.2 Examples

```
set_io -port_name IO_in\[2\]
-io_std LVCMOS25 \
-fixed true\
```

2.3.3 I/O Directions Not Supported

The following table lists I/O directions that are **not** supported for I/O standards.

Table 2-19. I/O Directions That are Not Supported (set_io)

I/O Direction	IO_STD Value
Input	SLVSE15, MLVDSE25, BUSLVDSE25, MIPIE33, LVPECLE33, SHIELD33, SHIELD25, SHIELD18, SHIELD15, SHIELD135, SHIELD12
Output	SLVS33, SLVS25, HCSL33, HCSL25, LVPECL33, LVPECL25, MIPI25, LVDS18, RSDS18, MINILVDS18, SUBLVDS18, PPDS18, SLVS18, HCSL18, LCMDS18
Tribuff	SLVS33, SLVS25, HCSL33, HCSL25, LVPECL33, LVPECL25, MIPI25, LVDS18, RSDS18, MINILVDS18, SUBLVDS18, PPDS18, SLVS18, HCSL18, LVDS25, LVDS33, RSDS25, RSDS33, MINILVDS25, MINILVDS33, SUBLVDS25, SUBLVDS33, PPDS25, PPDS33, LCMDS25, LCMDS33, LCMDS18

.....continued	
I/O Direction	**IO_STD Value**
Inout	LVDS33, LVDS18, LVDS25, RSDS18, RSDS33, RSDS25, MINILVDS18, MINILVDS33, MINILVDS25, SUBLVDS18, SUBLVDS33, SUBLVDS25, PPDS18, PPDS33, PPDS25, SLVS33, SLVS25, HCSL33, HCSL25, LVPECL33, LVPECL25, MIPI25, MIPIE25, SLVS18, HCSL18, SHIELD33, SHIELD25, SHIELD18, SHIELD15, SHIELD135, SHIELD12, LCMDS25, LCMDS33, LCMDS18

2.4 set_location

This PDC command assigns the specified macro to a particular location on the chip.

```
set_location -inst_name <macro_inst_name> -fixed <true|false> -x <integer> -y
<integer>
```

2.4.1 Arguments

-inst_name

Specifies the instance name of the macro in the netlist to assign to a particular location on the chip.

-fixed <true | false>

Sets whether the location of this instance is fixed (that is, locked). Locked instances are not moved during layout. The default is yes. The following table shows the acceptable values for this argument.

Table 2-20. -inst_name Values

Value	Description
true	The location of this instance is locked.
false	The location of this instance is unlocked.

-x -y

The x and y coordinates specify where to place the macro on the chip. Use the Chip Planner tool to determine the x and y coordinates of the location.

2.4.2 Exceptions

None

2.4.3 Example

This example assigns and locks the macro with the name “mem_data_in\[57\]” at the location x=7, y=2:

```
set_location -inst_name mem_data_in\[57\] -fixed true -x 7 -y 2
```

2.4.4 DDR3 Memory Placement

DDR3 memory needs to be placed in specific locations on the PolarFire chip to meet timing requirements. For DDR3 memory placement, the `set_location` command has the following syntax:

```
set_location -inst_name <hierarchical path to DDR instance> -location <edge>_<anchor>
```

-inst_name <*hierarchical path to DDR instance*>

Specifies the hierarchical path to the DDR instance.

-location <*edge*>_<*anchor*>

Specifies the edge_anchor location.

2.4.4.1 Example

```
set_location -inst_name {DDR3_TOP/DDR3_0}\ -location {NORTH_NE}
```

The maximum DDR width varies with the die/package combinations and the location they are placed in. See the following table for the correct location to place the DDR3 memory. The numbers in the table refer to the maximum DDR3 width.

Table 2-21. Locations for Placing DDR3 Memory

Die/Package	Location (Edge_Anchor} Edge={NORTH/SOUTH/WEST}, Anchor={NE/NW/SE/SW}					
	NORTH_NE	NORTH_NW	SOUTH_SE	SOUTH_SW	WEST_NW	WEST_SW
MPF200/FULLPKGE	16	16	Invalid Loc	40	64	40
MPF300/FCG1152	64	72	16	40	72	64
MPF300/FCG484	8	8	Invalid Loc	32	Invalid Loc	16
MPF300/FCVG484	16	16	Invalid Loc	40	16	16

2.4.5 PLL Placement

For PLL placement, the `set_location` command has the following syntax:

```
set_location -inst_name <hierarchical inst name> -location <PLL location>
```

-inst_name <*hierarchical inst name*>

Specifies the hierarchical instance name.

-location <*PLL location*>

Specifies the PLL location. Location can be one of the following:

- PLL0_NW
- PLL1_NW
- PLL0_NE
- PLL1_NE
- PLL0_SW
- PLL1_SW
- PLL0_SE
- PLL1_SE

For more information, see Placement Rules for PLLs and DLLs .

2.4.6 DLL Placement

For DLL placement, the `set_location` command has the following syntax:

```
set_location -inst_name <hierarchical inst name> -location <DLL location>
```

-inst_name <*hierarchical inst name*>

Specifies the hierarchical instance name.

-location <*DLL location*>

Specifies the DLL location. Location can be one of the following:

- DLL0_NW
- DLL1_NW
- DLL0_NE
- DLL1_NE
- DLL0_SW
- DLL1_SW
- DLL0_SE
- DLL1_SE

For more information, see Placement Rules for PLLs and DLLs.

2.4.7 TxPLL Placement

For TxPLL placement, the `set_location` command has the following syntax:

```
set_location -inst_name <hierarchical inst name> -location <TxPLL location>
```

-inst_name <*hierarchical inst name*>

Specifies the hierarchical instance name.

-location <*TxPLL location*>

Specifies the TxPLL location. Location can be one of the following:

- Q2_TXPLL0
- Q2_TXPLL_SSC
- Q2_TXPLL1
- Q0_TXPLL0
- Q0_TXPLL_SSC
- Q0_TXPLL1
- Q1_TXPLL0
- Q1_TXPLL_SSC
- Q1_TXPLL1
- Q3_TXPLL_SSC
- Q3_TXPLL1

For more information, see Placement Rules for Transceivers.

2.4.8 Placement Rules for PLLs and DLLs

The following error messages indicate non-compliance with placement rules for PLL and DLL.

PRPF_010: There can be a maximum of 6 PLL/DLL reference and/or fabric clocks coming driven by the FPGA fabric in the <NW|SW|NE|SE> location.

There are four “corners” (NW, SW, NE, NW) that PLL and DLL instances can be placed in on each MPF300 or MPF200 FPGA device.

You can place multiple PLL/DLL instances in each corner. However, for each corner, the sum total of PLL/DLL reference clocks and fabric clocks that the fabric drives must be six or less.

PRPF_011: There can be a maximum of 2 PLL/DLL reference clocks coming driven by the FPGA fabric in the <NW|SW|NE|SE> location.

For each corner, only two PLL/DLL reference clocks can be driven by the fabric.

2.4.9 Placement Rules for RGMII, SGMII, and IOG CDR Interfaces

Placement rules must be adhered to for RGMII, SGMII, and IOG CDR interfaces. Non-compliance with these rules may result in the following errors:

PRPF_001: Port <port name> for Interface <*inst name*> must be placed before running Place & Route.

All PADs must be placed using the `set_io` command.

PRPF_002: Interface <*inst name*> has ports that must be assigned to the same physical lane. The current port assignment for this interface does not meet this requirement.

For the SGMII interface and IOG CDR, all RX_ and TX_ PADs must be placed in the same lane. For the RGMII interface, all RX [ ] PADs and the RXCLK PAD must be placed in the same lane.

PRPF_003: The current Interface <*inst name*> port assignment requires that pin <pin name (functional pin name)> be reserved. You must not assign any port to that package pin.

For the SGMII interface and IOG CDR, the DQS_N pin of the lane is reserved for internal use. It must be left unused.

PRPF_004: You must not assign <*inst name*> to any location. Use the set_io command to assign any Interface port to package pins. This instance will automatically be placed.

IOD instances with TRAINING/OVERLAY should not be placed by users. These are internal instances, and will be handled by the tool.

PRPF_005: Port <*port name*> for Interface <inst name> must be assigned to <*pin name (functional pin name*)>.

For the RGMII interface, RX_CLK must be assigned to the DQS (P pad) of the lane.

2.4.10 Placement Rules for Transceivers

For PolarFire designs with the transceiver (XCVR) interface, some placement rules apply. Non-compliance with these rules may result in the following errors. For more information about rules for transceivers, refer to UG0677: User Guide PolarFire FPGA Transceiver

PRPF_007: TxPLL <*inst name*> must be placed before running Place & Route.

Transceiver Tx PLLs must be placed by the user with the `set_location` command before running Place and Route.

PRPF_008: Dedicated XCVR ports <*port name*>* must be placed before running Place & Route.

The transceiver interface has dedicated ports. These must be placed using the `set_io` command.

PRPF_009: Dedicated XCVR reference clock port <*port name*> must be placed before running Place & Route.

All transceiver reference clock PADs must be placed using the `set_io` command before running layout.

PRPF_008: Dedicated XCVR ports <*port name*>* must be placed before running Place & Route.

The transceiver interface has dedicated ports. These must be placed using the `set_io` command.

PRPF_009: Dedicated XCVR reference clock port <*port name*> must be placed before running Place & Route.

All transceiver reference clock PADs must be placed using the `set_io` command before running layout.

PRPF_009: Dedicated XCVR reference clock port <*port name*> must be placed before running Place & Route.

The transceiver interface has dedicated ports. These must be placed using the `set_io` command.

PRPF_008: Dedicated XCVR ports <*port name*>* must be placed before running Place & Route.

PRPF_009: Dedicated XCVR reference clock port <port name> must be placed before running Place & Route.

All transceiver reference clock PADs must be placed using the `set_io` command before running layout.

3. Netlist Attributes PDC Commands

Netlist Attributes PDC commands are used to set netlist-specific constraints. These commands are placed in a Compile Netlist Constraint (`*.ndc`) file and used by the Libero SoC Compile engine to optimize the post-synthesis netlist.

3.1 set_ioff

This command specifies whether or not a register is combined with an I/O during Synthesis. I/Os are combined with a register to achieve better clock-to-out and input-to-clock timing. This command is placed in a Compile Netlist Constraint (`*.ndc`) file that the Constraint Manager passes to Synthesis as a constraint in the Libero SoC Constraint Flow.

```
set_ioff -port_name <portname> \ [-IN_REG true/1|false/0] \
[-OUT_REG true/1|false/0] \ [-EN_REG true/1|false/0]
```

Note: This command is supported only as an NDC file to be read before Compile/Synthesis. At least one of the options above must be specified to use this command. Only one option can be enabled at a time. Microchip supports combining only one FF with the I/O, and the fanout must be 1.

3.1.1 Arguments

-port_name <*portname*>

Specifies the name of the I/O port to be combined with a register. The port can be an input, output, or inout port. Wildcard characters are supported.

-IN_REG

Specifies whether the input register is combined into the port <portname>. Valid values are “true/1” or “false/0”.

-OUT_REG

Specifies whether the output register is combined into the port <portname>. Valid values are “true/1” or “false/0”.

-EN_REG

Specifies whether the enable register is combined into the port <portname>. Valid values are “true/1” or “false/0”.

3.1.2 Example

The following command specifies that for the port minicoat[1], the output register is combined into the port, but is not combined into the input register or the enable register:

```
set_ioff -port_name {minicoat[1]} –IN_REG 0 –OUT_REG 1 –EN_REG 0
```

The following command specifies that for the port my_in_out[19], the enable register is combined into the port, but is not combined into the input register or the output register:

```
set_ioff {my_in_out[19]} –IN_REG 0 –OUT_REG 0 – EN_REG 1
```

The `set_ioff` command applies to scalar I/Os only. For an I/O bus, use the for loop available in Tcl. The following command combines each scalar member of the 32-bit I/O bus DataA with input registers:

```
for { set i 0 } { i &lt; 32 } { incr i } { set_ioff -port_name "DataA\[$i\]" -IN_REG
1 }
```

Alternatively, you can use a wildcard to include all scalar signals of an I/O bus:

```
set_ioff -port_name {DataA[*]} -IN_REG 1
```

3.1.3 Return Value

The command returns “0” on success and “1” on failure.

3.1.4 Error Messages

The following error messages are related to this command:

```
Error: [19138170]: PDCPF-426: IN_REG: Invalid argument value: 'yes' (expecting TRUE,
1, true, FALSE, 0 or false). [set_ioff -port_name PAD -IN_REG yes][[D:/designs/
test_ioff_ioedit/constraint/test.ndc]
```

```
Error: [19137989]: PDCPF-01: Port name doesn't exist in the netlist or is not
connected to an IoCell macro. [set_ioff -port_name PAD253 -IN_REG 1]
```

```
Error: [19138170]: PDCPF-426: Required parameter 'port_name' is missing. [set_ioff]
[[D:/ designs/test_ioff_ioedit/constraint/test.ndc]
```

3.2 set_preserve

This command sets a preserve property on instances before compile, so compile will preserve these instances and not combine them.

```
set_preserve -inst_name <instance_name>
```

3.2.1 Arguments

-inst_name

Specifies the full hierarchical name of the macro in the netlist to preserve.

3.2.2 Example

```
set_preserve -inst_name “test1/AND2_0”
```

4. Floorplanning PDC Commands

Floorplanning PDC commands are used to create and edit user regions and to assign/unassign logic to these regions.

4.1 assign_region

This PDC command constrains a set of macros to a specified region.

```
assign_region -region_name <region_name> -inst_name <macro_name>+
```

4.1.1 Arguments

-region_name

Specifies the region to which the macros are assigned. The macros are constrained to this region. Because the define_region command returns a region object, you can write a simpler command such as assign_region [define_region]+ [macro_name]+

-inst_name

Specifies the macro(s) to assign to the region. You must specify at least one macro name. The following table lists the wildcard characters you can use in macro names.

Table 4-1. Supported Wildcard Characters in Macro Names

Wildcard	What It Does
\	Interprets the next character as a non-special character
?	Matches any single character
*	Matches any string

Note: The region must be created before you can assign macros to it. If the region creation PDC command and the macro assignment command are in different PDC files, the order of the PDC files is important.

Note: You can assign only hard macros or their instances to a region. You cannot assign a group name. A hard macro is a logic cell consisting of one or more silicon modules with locked relative placement.

Note: The macro name must be a name with full hierarchical path.

4.1.2 Examples

In the following example, two macros are assigned to a region:

```
assign_region -region_name UserRegion1 -inst_name "test_0/AND2_0 test_0/AND2_1"
```

In the following example, all macros whose names have the prefix des01/Counter_1 (or all macros whose names match the expression des01/Counter_1/*) are assigned to a region:

```
assign_region -region_name User_region2 -inst_name des01/Counter_1/*
```

4.2 assign_net_macros

This PDC command assigns to a user-defined region all the macros that are connected to a net.

```
assign_net_macros -region_name <region_name> -net_name <net_name> -include_driver
<true|false>
```

4.2.1 Arguments

-region_name

Specifies the name of the region to which you are assigning macros. The region must exist before you use this command. See define_region (rectangular) or define_region (rectilinear). Because the define_region command returns a region object, you can write a simple command such as assign_net_macros [define_region]+ [net]+

-net_name

You must specify at least one net name. Net names are AFL-level (flattened netlist) names. These names match your netlist names most of the time. When they do not, you must export AFL and use the AFL names. Net names are case insensitive. Hierarchical net names from ADL are not allowed. The following table lists the wildcard characters you can use in net names.

Table 4-2. Supported Wildcard Characters in Net Names

Wildcard	What It Does
\	Interprets the next character as a non-special character
?	Matches any single character
*	Matches any string

-include_driver

Specifies whether to add the driver of the net(s) to the region. Enter one of the values in the following table.

Table 4-3. -include_driver Values

Value	Descriptions
true	Include the driver in the list of macros assigned to the region (default).
false	Do not assign the driver to the region.

Observe the following guidelines and see define_region for more information:

- Placed macros (not connected to the net) that are inside the area occupied by the net region are automatically unplaced.
- Net region constraints are internally converted into constraints on macros. PDC export results as a series of assign_region <region_name> macro1 statements for all the connected macros.
- If the region does not have enough space for all of the macros, or if the region constraint is impossible, the constraint is rejected and a warning message appears in the Log window.
- For overlapping regions, the intersection must be at least as big as the overlapping macro count.
- If a macro on the net cannot legally be placed in the region, it is not placed and a warning message appears in the Log window.
- Net region constraints may result in a single macro being assigned to multiple regions. These net region constraints result in constraining the macro to the intersection of all the regions affected by the constraint.

4.3 define_region

This PDC command defines either a rectangular region or a rectilinear region.

```
define_region -region_name <region_name> -type <inclusive|exclusive|empty> -x1
<integer> -y1 <integer> -x2 <integer> -y2 <integer> [-route <true|false>]
```

Note: The -route parameters are optional. To define region colors, use the Display option in the Chip Planner.

4.3.1 Arguments

-region_name <*region_name*>

Specifies the region name. The name must be unique. Do not use reserved names such as “bank0” and “bank<N>” for region names. If the region cannot be created, the name is empty. A default name is generated if a name is not specified in this argument.

-type <inclusive | exclusive | empty>

Specifies the region type. The following table shows the acceptable values for this argument.

Table 4-4. -type Values

Region Type	Description
Empty	Empty regions cannot contain macros
Exclusive	Only contains macros assigned to the region
Inclusive	Can contain macros both assigned and unassigned to the region

-x1 -y1 -x2 -y2

Specifies the series of coordinate pairs that constitute the region. These rectangles may or may not overlap. They are given as x1 y1 x2 y2 (where x1, y1 is the lower left and x2 y2 is the upper right corner in row/column coordinates). You must specify at least one set of coordinates.

-route <*value*>

Specifies whether to direct the routing of all nets internal to a region to be constrained within that region. A net is internal to a region if its source and destination pins are assigned to the region. The following table shows the acceptable values for this argument.

Table 4-5. -route Values

Constrain Routing Value	Description
true	Constrain the routing of nets within the region as well as the placement.
false	Do not constrain the routing of nets within the region. Only constrain the placement. This is the default value.

Note: Local clocks and global clocks are excluded from the -route option. Also, interface nets are excluded from the -route option because they cross region boundaries.

An empty routing region is an empty placement region. If -route is “true”, then no routing is allowed inside the empty region. However, local clocks and globals can cross empty regions.

An exclusive routing region is an exclusive placement region (rectilinear area with assigned macros) along with the following additional constraints:

- For all nets internal to the region (the source and all destinations belong to the region), routing must be inside the region (that is, such nets cannot be assigned any routing resource which is outside the region or crosses the region boundaries).
- Nets without pins inside the region cannot be assigned any routing resource which is inside the region or crosses any region boundaries.

An inclusive routing region is an inclusive placement region (rectilinear area with assigned macros) along with the following additional constraints:

- For all nets internal to the region (the source and all destinations belong to the region), routing must be inside the region (that is, such nets cannot be assigned any routing resource which is outside the region or crosses the region boundaries).
- Nets not internal to the region can be assigned routing resources within the region.

4.3.2 Description

Unlocked macros in empty or exclusive regions are unassigned from that region. You cannot create empty regions in areas that contain locked macros.

Use inclusive or exclusive region constraints if you intend to assign logic to a region. An inclusive region constraint with no macros assigned to it has no effect. An exclusive region constraint with no macros assigned to it is equivalent to an empty region.

Note: If macros assigned to a region exceed the area's capacity, the region's Properties Window displays the overbooked resources (over 100 percent resource utilization) in red.

4.3.3 Examples

The following example defines an empty rectangular region called UserRegion1 with lower-left co- ordinates (100,46) and upper-right co-ordinates (102,50).

```
define_region -region_name UserRegion1 -type empty -x1 100 -y1 46 -x2 102 -y2 50
```

The following example defines an inclusive rectilinear region with the name UserRegion2. This region contains two rectangular areas, one with lower-left co-ordinates (12,39) and upper-right coordinates (23,41) and another rectangle with lower-left co-ordinates (12,33) and upper-right co-ordinates (23,35).

```
define_region -region_name UserRegion2 -type exclusive -x1 12 -y1 39 -x2 23 -y2 41 -x1
12 -y1 33\ -x2 23 -y2 35
```

The following examples define three regions with three different colors:

```
define_region -region_name UserRegion0 -color 128 -x1 50 -y1 19 -x2 60 -y2 25
define_region -region_name UserRegion1 -color 16711935 -x1 11 -y1 2 -x2 55 -y2 29
define_region -region_name UserRegion2 -color 8388736 -x1 61 -y1 6 -x2 69 -y2 19
```

For more information about regions, see assign_region.

4.4 move_region

This PDC command moves the named region to the specified coordinates.

```
move_region -region_name <region_name> -x1 <integer> -y1 <integer> -x2 <integer> -y2
<integer>
```

4.4.1 Arguments

-region_name

Specifies the name of the region to move. This name must be unique.

-x1 -y1 -x2 -y2

Specifies the series of coordinate pairs representing the location in which to move the named region. These rectangles can overlap. They are given as x1, y1, x2, y2, where x1, y1 represents the lower-left corner of the rectangle and x2 y2 represents the upper-right corner. You must specify at least one set of coordinates.

4.4.2 Example

This example moves the region named UserRegion1 to a new region with lower-left co-ordinates (0,40) and upper-right co-ordinates (3,42):

```
move_region -region_name UserRegion1 -x1 0 -y1 40 -x2 3 -y2 42
```

For more information about regions, see define_region.

5. A – Packages/Memory Types

This appendix provides device, package, slot, and memory type information.

Device	Package	Slot	Memory Type
PA5M100	FCG484	NORTH_NE	DDR3
PA5M100	FCG484	NORTH_NE	DDR4
PA5M100	FCG484	NORTH_NE	QDR II+ x18
PA5M100	FCG484	NORTH_NE	QDR II+ x8
PA5M100	FCG484	NORTH_NE	QDR II+ x9
PA5M100	FCG484	NORTH_NW	DDR3
PA5M100	FCG484	NORTH_NW	DDR4
PA5M100	FCG484	NORTH_NW	QDR II+ x18
PA5M100	FCG484	NORTH_NW	QDR II+ x8
PA5M100	FCG484	NORTH_NW	QDR II+ x9
PA5M100	FCG484	SOUTH_SW	DDR3
PA5M100	FCG484	SOUTH_SW	QDR II+ x18
PA5M100	FCG484	SOUTH_SW	QDR II+ x8
PA5M100	FCG484	SOUTH_SW	QDR II+ x9
PA5M100	FCSG325	NORTH_NE	DDR3
PA5M100	FCSG325	NORTH_NE	DDR4
PA5M100	FCSG325	NORTH_NE	QDR II+ x18
PA5M100	FCSG325	NORTH_NE	QDR II+ x8
PA5M100	FCSG325	NORTH_NE	QDR II+ x9
PA5M100	FCSG325	NORTH_NW	DDR3
PA5M100	FCSG325	NORTH_NW	DDR4
PA5M100	FCSG325	NORTH_NW	QDR II+ x18
PA5M100	FCSG325	NORTH_NW	QDR II+ x8
PA5M100	FCSG325	NORTH_NW	QDR II+ x9
PA5M100	FCSG325	SOUTH_SW	DDR3
PA5M100	FCSG536	NORTH_NE	DDR3
PA5M100	FCSG536	NORTH_NE	DDR4
PA5M100	FCSG536	NORTH_NE	QDR II+ x18
PA5M100	FCSG536	NORTH_NE	QDR II+ x8
PA5M100	FCSG536	NORTH_NE	QDR II+ x9
PA5M100	FCSG536	NORTH_NW	DDR3
PA5M100	FCSG536	NORTH_NW	DDR4
PA5M100	FCSG536	NORTH_NW	QDR II+ x18

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Device	Package	Slot	Memory Type
PA5M100	FCSG536	NORTH_NW	QDR II+ x8
PA5M100	FCSG536	NORTH_NW	QDR II+ x9
PA5M100	FCSG536	SOUTH_SW	DDR3
PA5M100	FCSG536	SOUTH_SW	QDR II+ x18
PA5M100	FCSG536	SOUTH_SW	QDR II+ x8
PA5M100	FCSG536	SOUTH_SW	QDR II+ x9
PA5M100	FCSG536	WEST_NW	DDR3
PA5M100	FCSG536	WEST_NW	QDR II+ x8
PA5M100	FCSG536	WEST_NW	QDR II+ x9
PA5M100	FCVG484	NORTH_NE	DDR3
PA5M100	FCVG484	NORTH_NE	DDR4
PA5M100	FCVG484	NORTH_NE	QDR II+ x18
PA5M100	FCVG484	NORTH_NE	QDR II+ x8
PA5M100	FCVG484	NORTH_NE	QDR II+ x9
PA5M100	FCVG484	NORTH_NW	DDR3
PA5M100	FCVG484	NORTH_NW	DDR4
PA5M100	FCVG484	NORTH_NW	QDR II+ x18
PA5M100	FCVG484	NORTH_NW	QDR II+ x8
PA5M100	FCVG484	NORTH_NW	QDR II+ x9
PA5M100	FCVG484	SOUTH_SW	DDR3
PA5M100	FCVG484	SOUTH_SW	QDR II+ x18
PA5M100	FCVG484	SOUTH_SW	QDR II+ x8
PA5M100	FCVG484	SOUTH_SW	QDR II+ x9
PA5M100	FCVG484	WEST_NW	DDR3
PA5M100	FCVG484	WEST_NW	QDR II+ x8
PA5M100	FCVG484	WEST_NW	QDR II+ x9
PA5M100	FULLPKG	NORTH_NE	DDR3
PA5M100	FULLPKG	NORTH_NE	DDR4
PA5M100	FULLPKG	NORTH_NE	QDR II+ x18
PA5M100	FULLPKG	NORTH_NE	QDR II+ x8
PA5M100	FULLPKG	NORTH_NE	QDR II+ x9
PA5M100	FULLPKG	NORTH_NW	DDR3
PA5M100	FULLPKG	NORTH_NW	DDR4
PA5M100	FULLPKG	NORTH_NW	QDR II+ x18
PA5M100	FULLPKG	NORTH_NW	QDR II+ x8

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Device	Package	Slot	Memory Type
PA5M100	FULLPKG	NORTH_NW	QDR II+ x9
PA5M100	FULLPKG	SOUTH_SW	DDR3
PA5M100	FULLPKG	SOUTH_SW	QDR II+ x18
PA5M100	FULLPKG	SOUTH_SW	QDR II+ x8
PA5M100	FULLPKG	SOUTH_SW	QDR II+ x9
PA5M100	FULLPKG	WEST_NW	DDR3
PA5M100	FULLPKG	WEST_NW	QDR II+ x8
PA5M100	FULLPKG	WEST_NW	QDR II+ x9
PA5M200	FCG484	NORTH_NE	DDR3
PA5M200	FCG484	NORTH_NE	DDR4
PA5M200	FCG484	NORTH_NE	QDR II+ x18
PA5M200	FCG484	NORTH_NE	QDR II+ x8
PA5M200	FCG484	NORTH_NE	QDR II+ x9
PA5M200	FCG484	NORTH_NW	DDR3
PA5M200	FCG484	NORTH_NW	DDR4
PA5M200	FCG484	NORTH_NW	QDR II+ x18
PA5M200	FCG484	NORTH_NW	QDR II+ x8
PA5M200	FCG484	NORTH_NW	QDR II+ x9
PA5M200	FCG484	SOUTH_SW	DDR3
PA5M200	FCG484	SOUTH_SW	QDR II+ x18
PA5M200	FCG484	SOUTH_SW	QDR II+ x8
PA5M200	FCG484	SOUTH_SW	QDR II+ x9
PA5M200	FCG484	WEST_SW	DDR3
PA5M200	FCG484	WEST_SW	QDR II+ x8
PA5M200	FCG484	WEST_SW	QDR II+ x9
PA5M200	FCG784	NORTH_NE	DDR3
PA5M200	FCG784	NORTH_NE	DDR4
PA5M200	FCG784	NORTH_NE	QDR II+ x18
PA5M200	FCG784	NORTH_NE	QDR II+ x36
PA5M200	FCG784	NORTH_NE	QDR II+ x8
PA5M200	FCG784	NORTH_NE	QDR II+ x9
PA5M200	FCG784	NORTH_NW	DDR3
PA5M200	FCG784	NORTH_NW	DDR4
PA5M200	FCG784	NORTH_NW	QDR II+ x18
PA5M200	FCG784	NORTH_NW	QDR II+ x36

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Device	Package	Slot	Memory Type
PA5M200	FCG784	NORTH_NW	QDR II+ x8
PA5M200	FCG784	NORTH_NW	QDR II+ x9
PA5M200	FCG784	SOUTH_SW	DDR3
PA5M200	FCG784	SOUTH_SW	QDR II+ x18
PA5M200	FCG784	SOUTH_SW	QDR II+ x8
PA5M200	FCG784	SOUTH_SW	QDR II+ x9
PA5M200	FCG784	WEST_NW	DDR3
PA5M200	FCG784	WEST_NW	QDR II+ x18
PA5M200	FCG784	WEST_NW	QDR II+ x36
PA5M200	FCG784	WEST_NW	QDR II+ x8
PA5M200	FCG784	WEST_NW	QDR II+ x9
PA5M200	FCG784	WEST_SW	DDR3
PA5M200	FCG784	WEST_SW	QDR II+ x18
PA5M200	FCG784	WEST_SW	QDR II+ x8
PA5M200	FCG784	WEST_SW	QDR II+ x9
PA5M200	FCSG325	NORTH_NE	DDR3
PA5M200	FCSG325	NORTH_NE	DDR4
PA5M200	FCSG325	NORTH_NE	QDR II+ x18
PA5M200	FCSG325	NORTH_NE	QDR II+ x8
PA5M200	FCSG325	NORTH_NE	QDR II+ x9
PA5M200	FCSG325	NORTH_NW	DDR3
PA5M200	FCSG325	NORTH_NW	DDR4
PA5M200	FCSG325	NORTH_NW	QDR II+ x18
PA5M200	FCSG325	NORTH_NW	QDR II+ x8
PA5M200	FCSG325	NORTH_NW	QDR II+ x9
PA5M200	FCSG325	SOUTH_SW	DDR3
PA5M200	FCSG536	NORTH_NE	DDR3
PA5M200	FCSG536	NORTH_NE	DDR4
PA5M200	FCSG536	NORTH_NE	QDR II+ x18
PA5M200	FCSG536	NORTH_NE	QDR II+ x8
PA5M200	FCSG536	NORTH_NE	QDR II+ x9
PA5M200	FCSG536	NORTH_NW	DDR3
PA5M200	FCSG536	NORTH_NW	DDR4
PA5M200	FCSG536	NORTH_NW	QDR II+ x18
PA5M200	FCSG536	NORTH_NW	QDR II+ x8

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Device	Package	Slot	Memory Type
PA5M200	FCSG536	NORTH_NW	QDR II+ x9
PA5M200	FCSG536	SOUTH_SW	DDR3
PA5M200	FCSG536	SOUTH_SW	QDR II+ x18
PA5M200	FCSG536	SOUTH_SW	QDR II+ x8
PA5M200	FCSG536	SOUTH_SW	QDR II+ x9
PA5M200	FCSG536	WEST_NW	DDR3
PA5M200	FCSG536	WEST_NW	QDR II+ x18
PA5M200	FCSG536	WEST_NW	QDR II+ x8
PA5M200	FCSG536	WEST_NW	QDR II+ x9
PA5M200	FCSG536	WEST_SW	DDR3
PA5M200	FCSG536	WEST_SW	QDR II+ x8
PA5M200	FCSG536	WEST_SW	QDR II+ x9
PA5M200	FCVG484	NORTH_NE	DDR3
PA5M200	FCVG484	NORTH_NE	DDR4
PA5M200	FCVG484	NORTH_NE	QDR II+ x18
PA5M200	FCVG484	NORTH_NE	QDR II+ x8
PA5M200	FCVG484	NORTH_NE	QDR II+ x9
PA5M200	FCVG484	NORTH_NW	DDR3
PA5M200	FCVG484	NORTH_NW	DDR4
PA5M200	FCVG484	NORTH_NW	QDR II+ x18
PA5M200	FCVG484	NORTH_NW	QDR II+ x8
PA5M200	FCVG484	NORTH_NW	QDR II+ x9
PA5M200	FCVG484	SOUTH_SW	DDR3
PA5M200	FCVG484	SOUTH_SW	QDR II+ x18
PA5M200	FCVG484	SOUTH_SW	QDR II+ x8
PA5M200	FCVG484	SOUTH_SW	QDR II+ x9
PA5M200	FCVG484	WEST_NW	DDR3
PA5M200	FCVG484	WEST_NW	QDR II+ x8
PA5M200	FCVG484	WEST_NW	QDR II+ x9
PA5M200	FCVG484	WEST_SW	DDR3
PA5M200	FCVG484	WEST_SW	QDR II+ x8
PA5M200	FCVG484	WEST_SW	QDR II+ x9
PA5M200	FULLPKG	NORTH_NE	DDR3
PA5M200	FULLPKG	NORTH_NE	DDR4
PA5M200	FULLPKG	NORTH_NE	QDR II+ x18

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Device	Package	Slot	Memory Type
PA5M200	FULLPKG	NORTH_NE	QDR II+ x36
PA5M200	FULLPKG	NORTH_NE	QDR II+ x8
PA5M200	FULLPKG	NORTH_NE	QDR II+ x9
PA5M200	FULLPKG	NORTH_NW	DDR3
PA5M200	FULLPKG	NORTH_NW	DDR4
PA5M200	FULLPKG	NORTH_NW	QDR II+ x18
PA5M200	FULLPKG	NORTH_NW	QDR II+ x36
PA5M200	FULLPKG	NORTH_NW	QDR II+ x8
PA5M200	FULLPKG	NORTH_NW	QDR II+ x9
PA5M200	FULLPKG	SOUTH_SW	DDR3
PA5M200	FULLPKG	SOUTH_SW	QDR II+ x18
PA5M200	FULLPKG	SOUTH_SW	QDR II+ x8
PA5M200	FULLPKG	SOUTH_SW	QDR II+ x9
PA5M200	FULLPKG	WEST_NW	DDR3
PA5M200	FULLPKG	WEST_NW	QDR II+ x18
PA5M200	FULLPKG	WEST_NW	QDR II+ x36
PA5M200	FULLPKG	WEST_NW	QDR II+ x8
PA5M200	FULLPKG	WEST_NW	QDR II+ x9
PA5M200	FULLPKG	WEST_SW	DDR3
PA5M200	FULLPKG	WEST_SW	QDR II+ x18
PA5M200	FULLPKG	WEST_SW	QDR II+ x8
PA5M200	FULLPKG	WEST_SW	QDR II+ x9
PA5M300	FCG1152	NORTH_NE	DDR3
PA5M300	FCG1152	NORTH_NE	DDR4
PA5M300	FCG1152	NORTH_NE	QDR II+ x18
PA5M300	FCG1152	NORTH_NE	QDR II+ x36
PA5M300	FCG1152	NORTH_NE	QDR II+ x8
PA5M300	FCG1152	NORTH_NE	QDR II+ x9
PA5M300	FCG1152	NORTH_NW	DDR3
PA5M300	FCG1152	NORTH_NW	DDR4
PA5M300	FCG1152	NORTH_NW	QDR II+ x18
PA5M300	FCG1152	NORTH_NW	QDR II+ x36
PA5M300	FCG1152	NORTH_NW	QDR II+ x8
PA5M300	FCG1152	NORTH_NW	QDR II+ x9
PA5M300	FCG1152	SOUTH_SE	DDR3

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Device	Package	Slot	Memory Type
PA5M300	FCG1152	SOUTH_SE	DDR4
PA5M300	FCG1152	SOUTH_SE	QDR II+ x8
PA5M300	FCG1152	SOUTH_SE	QDR II+ x9
PA5M300	FCG1152	SOUTH_SW	DDR3
PA5M300	FCG1152	SOUTH_SW	QDR II+ x18
PA5M300	FCG1152	SOUTH_SW	QDR II+ x8
PA5M300	FCG1152	SOUTH_SW	QDR II+ x9
PA5M300	FCG1152	WEST_NW	DDR3
PA5M300	FCG1152	WEST_NW	QDR II+ x18
PA5M300	FCG1152	WEST_NW	QDR II+ x36
PA5M300	FCG1152	WEST_NW	QDR II+ x8
PA5M300	FCG1152	WEST_NW	QDR II+ x9
PA5M300	FCG1152	WEST_SW	DDR3
PA5M300	FCG1152	WEST_SW	QDR II+ x18
PA5M300	FCG1152	WEST_SW	QDR II+ x36
PA5M300	FCG1152	WEST_SW	QDR II+ x8
PA5M300	FCG1152	WEST_SW	QDR II+ x9
PA5M300	FCG484	NORTH_NE	DDR3
PA5M300	FCG484	NORTH_NE	DDR4
PA5M300	FCG484	NORTH_NE	QDR II+ x18
PA5M300	FCG484	NORTH_NE	QDR II+ x8
PA5M300	FCG484	NORTH_NE	QDR II+ x9
PA5M300	FCG484	NORTH_NW	DDR3
PA5M300	FCG484	NORTH_NW	DDR4
PA5M300	FCG484	NORTH_NW	QDR II+ x18
PA5M300	FCG484	NORTH_NW	QDR II+ x8
PA5M300	FCG484	NORTH_NW	QDR II+ x9
PA5M300	FCG484	SOUTH_SW	DDR3
PA5M300	FCG484	SOUTH_SW	QDR II+ x18
PA5M300	FCG484	SOUTH_SW	QDR II+ x8
PA5M300	FCG484	SOUTH_SW	QDR II+ x9
PA5M300	FCG484	WEST_SW	DDR3
PA5M300	FCG484	WEST_SW	QDR II+ x8
PA5M300	FCG484	WEST_SW	QDR II+ x9
PA5M300	FCG784	NORTH_NE	DDR3

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Device	Package	Slot	Memory Type
PA5M300	FCG784	NORTH_NE	DDR4
PA5M300	FCG784	NORTH_NE	QDR II+ x18
PA5M300	FCG784	NORTH_NE	QDR II+ x36
PA5M300	FCG784	NORTH_NE	QDR II+ x8
PA5M300	FCG784	NORTH_NE	QDR II+ x9
PA5M300	FCG784	NORTH_NW	DDR3
PA5M300	FCG784	NORTH_NW	DDR4
PA5M300	FCG784	NORTH_NW	QDR II+ x18
PA5M300	FCG784	NORTH_NW	QDR II+ x36
PA5M300	FCG784	NORTH_NW	QDR II+ x8
PA5M300	FCG784	NORTH_NW	QDR II+ x9
PA5M300	FCG784	SOUTH_SW	DDR3
PA5M300	FCG784	SOUTH_SW	QDR II+ x18
PA5M300	FCG784	SOUTH_SW	QDR II+ x8
PA5M300	FCG784	SOUTH_SW	QDR II+ x9
PA5M300	FCG784	WEST_NW	DDR3
PA5M300	FCG784	WEST_NW	QDR II+ x18
PA5M300	FCG784	WEST_NW	QDR II+ x36
PA5M300	FCG784	WEST_NW	QDR II+ x8
PA5M300	FCG784	WEST_NW	QDR II+ x9
PA5M300	FCG784	WEST_SW	DDR3
PA5M300	FCG784	WEST_SW	QDR II+ x18
PA5M300	FCG784	WEST_SW	QDR II+ x36
PA5M300	FCG784	WEST_SW	QDR II+ x8
PA5M300	FCG784	WEST_SW	QDR II+ x9
PA5M300	FCSG536	NORTH_NE	DDR3
PA5M300	FCSG536	NORTH_NE	DDR4
PA5M300	FCSG536	NORTH_NE	QDR II+ x18
PA5M300	FCSG536	NORTH_NE	QDR II+ x8
PA5M300	FCSG536	NORTH_NE	QDR II+ x9
PA5M300	FCSG536	NORTH_NW	DDR3
PA5M300	FCSG536	NORTH_NW	DDR4
PA5M300	FCSG536	NORTH_NW	QDR II+ x18
PA5M300	FCSG536	NORTH_NW	QDR II+ x8
PA5M300	FCSG536	NORTH_NW	QDR II+ x9

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Device	Package	Slot	Memory Type
PA5M300	FCSG536	SOUTH_SW	DDR3
PA5M300	FCSG536	SOUTH_SW	QDR II+ x18
PA5M300	FCSG536	SOUTH_SW	QDR II+ x8
PA5M300	FCSG536	SOUTH_SW	QDR II+ x9
PA5M300	FCSG536	WEST_NW	DDR3
PA5M300	FCSG536	WEST_NW	QDR II+ x18
PA5M300	FCSG536	WEST_NW	QDR II+ x8
PA5M300	FCSG536	WEST_NW	QDR II+ x9
PA5M300	FCSG536	WEST_SW	DDR3
PA5M300	FCSG536	WEST_SW	QDR II+ x8
PA5M300	FCSG536	WEST_SW	QDR II+ x9
PA5M300	FCVG484	NORTH_NE	DDR3
PA5M300	FCVG484	NORTH_NE	DDR4
PA5M300	FCVG484	NORTH_NE	QDR II+ x18
PA5M300	FCVG484	NORTH_NE	QDR II+ x8
PA5M300	FCVG484	NORTH_NE	QDR II+ x9
PA5M300	FCVG484	NORTH_NW	DDR3
PA5M300	FCVG484	NORTH_NW	DDR4
PA5M300	FCVG484	NORTH_NW	QDR II+ x18
PA5M300	FCVG484	NORTH_NW	QDR II+ x8
PA5M300	FCVG484	NORTH_NW	QDR II+ x9
PA5M300	FCVG484	SOUTH_SW	DDR3
PA5M300	FCVG484	SOUTH_SW	QDR II+ x18
PA5M300	FCVG484	SOUTH_SW	QDR II+ x8
PA5M300	FCVG484	SOUTH_SW	QDR II+ x9
PA5M300	FCVG484	WEST_NW	DDR3
PA5M300	FCVG484	WEST_NW	QDR II+ x8
PA5M300	FCVG484	WEST_NW	QDR II+ x9
PA5M300	FCVG484	WEST_SW	DDR3
PA5M300	FCVG484	WEST_SW	QDR II+ x8
PA5M300	FCVG484	WEST_SW	QDR II+ x9
PA5M300	FULLPKG	NORTH_NE	DDR3
PA5M300	FULLPKG	NORTH_NE	DDR4
PA5M300	FULLPKG	NORTH_NE	QDR II+ x18
PA5M300	FULLPKG	NORTH_NE	QDR II+ x36

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Device	Package	Slot	Memory Type
PA5M300	FULLPKG	NORTH_NE	QDR II+ x8
PA5M300	FULLPKG	NORTH_NE	QDR II+ x9
PA5M300	FULLPKG	NORTH_NW	DDR3
PA5M300	FULLPKG	NORTH_NW	DDR4
PA5M300	FULLPKG	NORTH_NW	QDR II+ x18
PA5M300	FULLPKG	NORTH_NW	QDR II+ x36
PA5M300	FULLPKG	NORTH_NW	QDR II+ x8
PA5M300	FULLPKG	NORTH_NW	QDR II+ x9
PA5M300	FULLPKG	SOUTH_SE	DDR3
PA5M300	FULLPKG	SOUTH_SE	DDR4
PA5M300	FULLPKG	SOUTH_SE	QDR II+ x8
PA5M300	FULLPKG	SOUTH_SE	QDR II+ x9
PA5M300	FULLPKG	SOUTH_SW	DDR3
PA5M300	FULLPKG	SOUTH_SW	QDR II+ x18
PA5M300	FULLPKG	SOUTH_SW	QDR II+ x8
PA5M300	FULLPKG	SOUTH_SW	QDR II+ x9
PA5M300	FULLPKG	WEST_NW	DDR3
PA5M300	FULLPKG	WEST_NW	QDR II+ x18
PA5M300	FULLPKG	WEST_NW	QDR II+ x36
PA5M300	FULLPKG	WEST_NW	QDR II+ x8
PA5M300	FULLPKG	WEST_NW	QDR II+ x9
PA5M300	FULLPKG	WEST_SW	DDR3
PA5M300	FULLPKG	WEST_SW	QDR II+ x18
PA5M300	FULLPKG	WEST_SW	QDR II+ x36
PA5M300	FULLPKG	WEST_SW	QDR II+ x8
PA5M300	FULLPKG	WEST_SW	QDR II+ x9
PA5M500	FCG1152	NORTH_NE	DDR3
PA5M500	FCG1152	NORTH_NE	DDR4
PA5M500	FCG1152	NORTH_NE	QDR II+ x18
PA5M500	FCG1152	NORTH_NE	QDR II+ x36
PA5M500	FCG1152	NORTH_NE	QDR II+ x8
PA5M500	FCG1152	NORTH_NE	QDR II+ x9
PA5M500	FCG1152	NORTH_NW	DDR3
PA5M500	FCG1152	NORTH_NW	DDR4
PA5M500	FCG1152	NORTH_NW	QDR II+ x18

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Device	Package	Slot	Memory Type
PA5M500	FCG1152	NORTH_NW	QDR II+ x36
PA5M500	FCG1152	NORTH_NW	QDR II+ x8
PA5M500	FCG1152	NORTH_NW	QDR II+ x9
PA5M500	FCG1152	SOUTH_SE	DDR3
PA5M500	FCG1152	SOUTH_SE	DDR4
PA5M500	FCG1152	SOUTH_SE	QDR II+ x18
PA5M500	FCG1152	SOUTH_SE	QDR II+ x8
PA5M500	FCG1152	SOUTH_SE	QDR II+ x9
PA5M500	FCG1152	SOUTH_SW	DDR3
PA5M500	FCG1152	SOUTH_SW	QDR II+ x18
PA5M500	FCG1152	SOUTH_SW	QDR II+ x8
PA5M500	FCG1152	SOUTH_SW	QDR II+ x9
PA5M500	FCG1152	WEST_NW	DDR3
PA5M500	FCG1152	WEST_NW	QDR II+ x18
PA5M500	FCG1152	WEST_NW	QDR II+ x36
PA5M500	FCG1152	WEST_NW	QDR II+ x8
PA5M500	FCG1152	WEST_NW	QDR II+ x9
PA5M500	FCG1152	WEST_SW	DDR3
PA5M500	FCG1152	WEST_SW	QDR II+ x18
PA5M500	FCG1152	WEST_SW	QDR II+ x36
PA5M500	FCG1152	WEST_SW	QDR II+ x8
PA5M500	FCG1152	WEST_SW	QDR II+ x9
PA5M500	FCG784	NORTH_NE	DDR3
PA5M500	FCG784	NORTH_NE	DDR4
PA5M500	FCG784	NORTH_NE	QDR II+ x18
PA5M500	FCG784	NORTH_NE	QDR II+ x36
PA5M500	FCG784	NORTH_NE	QDR II+ x8
PA5M500	FCG784	NORTH_NE	QDR II+ x9
PA5M500	FCG784	NORTH_NW	DDR3
PA5M500	FCG784	NORTH_NW	DDR4
PA5M500	FCG784	NORTH_NW	QDR II+ x18
PA5M500	FCG784	NORTH_NW	QDR II+ x36
PA5M500	FCG784	NORTH_NW	QDR II+ x8
PA5M500	FCG784	NORTH_NW	QDR II+ x9
PA5M500	FCG784	SOUTH_SW	DDR3

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Device	Package	Slot	Memory Type
PA5M500	FCG784	SOUTH_SW	QDR II+ x18
PA5M500	FCG784	SOUTH_SW	QDR II+ x8
PA5M500	FCG784	SOUTH_SW	QDR II+ x9
PA5M500	FCG784	WEST_NW	DDR3
PA5M500	FCG784	WEST_NW	QDR II+ x18
PA5M500	FCG784	WEST_NW	QDR II+ x36
PA5M500	FCG784	WEST_NW	QDR II+ x8
PA5M500	FCG784	WEST_NW	QDR II+ x9
PA5M500	FCG784	WEST_SW	DDR3
PA5M500	FCG784	WEST_SW	QDR II+ x18
PA5M500	FCG784	WEST_SW	QDR II+ x36
PA5M500	FCG784	WEST_SW	QDR II+ x8
PA5M500	FCG784	WEST_SW	QDR II+ x9
PA5M500	FULLPKG	NORTH_NE	DDR3
PA5M500	FULLPKG	NORTH_NE	DDR4
PA5M500	FULLPKG	NORTH_NE	QDR II+ x18
PA5M500	FULLPKG	NORTH_NE	QDR II+ x36
PA5M500	FULLPKG	NORTH_NE	QDR II+ x8
PA5M500	FULLPKG	NORTH_NE	QDR II+ x9
PA5M500	FULLPKG	NORTH_NW	DDR3
PA5M500	FULLPKG	NORTH_NW	DDR4
PA5M500	FULLPKG	NORTH_NW	QDR II+ x18
PA5M500	FULLPKG	NORTH_NW	QDR II+ x36
PA5M500	FULLPKG	NORTH_NW	QDR II+ x8
PA5M500	FULLPKG	NORTH_NW	QDR II+ x9
PA5M500	FULLPKG	SOUTH_SE	DDR3
PA5M500	FULLPKG	SOUTH_SE	DDR4
PA5M500	FULLPKG	SOUTH_SE	QDR II+ x18
PA5M500	FULLPKG	SOUTH_SE	QDR II+ x8
PA5M500	FULLPKG	SOUTH_SE	QDR II+ x9
PA5M500	FULLPKG	SOUTH_SW	DDR3
PA5M500	FULLPKG	SOUTH_SW	QDR II+ x18
PA5M500	FULLPKG	SOUTH_SW	QDR II+ x8
PA5M500	FULLPKG	SOUTH_SW	QDR II+ x9
PA5M500	FULLPKG	WEST_NW	DDR3

.....continued

Device	Package	Slot	Memory Type
PA5M500	FULLPKG	WEST_NW	QDR II+ x18
PA5M500	FULLPKG	WEST_NW	QDR II+ x36
PA5M500	FULLPKG	WEST_NW	QDR II+ x8
PA5M500	FULLPKG	WEST_NW	QDR II+ x9
PA5M500	FULLPKG	WEST_NW	RLDRAM II
PA5M500	FULLPKG	WEST_SW	DDR3
PA5M500	FULLPKG	WEST_SW	QDR II+ x18
PA5M500	FULLPKG	WEST_SW	QDR II+ x36
PA5M500	FULLPKG	WEST_SW	QDR II+ x8
PA5M500	FULLPKG	WEST_SW	QDR II+ x9

6. Revision History

Revision	Date	Description
B	04/2021	Editorial updates only. No technical content updates.
A	11/2020	Document converted to Microchip template. Initial Revision.

7. Microchip FPGA Technical Support

Microchip FPGA Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, and worldwide sales offices. This section provides information about contacting Microchip FPGA Products Group and using these support services.

7.1 Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

- From North America, call **800.262.1060**
- From the rest of the world, call **650.318.4460**
- Fax, from anywhere in the world, **650.318.8044**

7.2 Customer Technical Support

Microchip FPGA Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microchip FPGA Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

You can communicate your technical questions through our Web portal and receive answers back by email, fax, or phone. Also, if you have design problems, you can upload your design files to receive assistance. We constantly monitor the cases created from the web portal throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

Technical support can be reached at soc.microsemi.com/Portal/Default.aspx.

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), log in at soc.microsemi.com/Portal/Default.aspx, go to the **My Cases** tab, and select **Yes** in the ITAR drop-down list when creating a new case. For a complete list of ITAR-regulated Microchip FPGAs, visit the ITAR web page.

You can track technical cases online by going to My Cases.

7.3 Website

You can browse a variety of technical and non-technical information on the Microchip FPGA Products Group home page, at www.microsemi.com/soc.

7.4 Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support at (https://soc.microsemi.com/Portal/Default.aspx) or contact a local sales office.

Visit About Us for sales office listings and corporate contacts.

The Microchip Website

Microchip provides online support via our website at www.microchip.com/. This website is used to make files and information easily available to customers. Some of the content available includes:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip design partner program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

Product Change Notification Service

Microchip's product change notification service helps keep customers current on Microchip products. Subscribers will receive email notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, go to www.microchip.com/pcn and follow the registration instructions.

Customer Support

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Embedded Solutions Engineer (ESE)
- Technical Support

Customers should contact their distributor, representative or ESE for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in this document.

Technical support is available through the website at: www.microchip.com/support

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods being used in attempts to breach the code protection features of the Microchip devices. We believe that these methods require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Attempts to breach these code protection features, most likely, cannot be accomplished without violating Microchip's intellectual property rights.
- Microchip is willing to work with any customer who is concerned about the integrity of its code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is "unbreakable." Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

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