Libero® SoC v2022.2

SmartDesign User Guide

Introduction

SmartDesign is a visual block-based design creation and entry tool for the instantiation, configuration, connection of Microchip IPs, user-generated IPs, and custom and glue-logic HDL modules. This tool provides a canvas for stitching together the various design components. The final result from SmartDesign is a design rule checked and synthesis ready HDL file. A generated SmartDesign can be the entire FPGA design or a component subsystem to be reused in a larger design.

The following design objects can be instantiated in the SmartDesign canvas.

- Microchip IP Cores
- User-generated or third-party IP Cores
- HDL design files
- HDL core design files
- Basic macros
- Other SmartDesign components generated from SmartDesign in the current Libero® SoC project or imported from other Libero SoC projects.
- Reusable design blocks published from Libero SoC

Important:
This document is updated frequently. The latest version of this document is available at this location: Libero SoC Design Suite Documentation.

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1. About SmartDesign

This section provides an overview of SmartDesign.

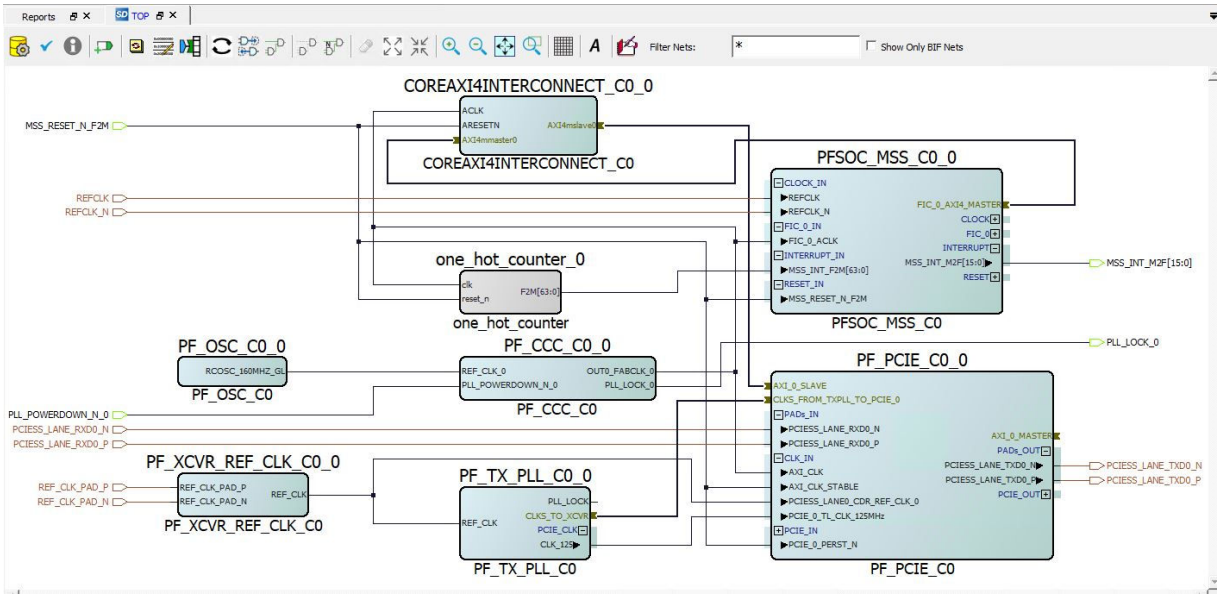
1.1 Canvas Layout

The SmartDesign canvas places all components in columns, with the nets vertically routed in the space between columns. Top-level input ports are placed in the leftmost column. Top-level output ports and inout ports are placed in the rightmost column.

Components can be moved up and down the columns. When components are instantiated in SmartDesign, they are placed in an existing column or a new column created for them. When components are moved up and down, the column boundaries are shown. When components are moved horizontally, the instance can be moved to a different column, the column it is in can be moved, or a new column can be created at the new location for the instance.

The following figure shows the SmartDesign canvas.

Figure 1-1. SmartDesign Canvas



1.2 SmartDesign in the Libero SoC Design Flow

SmartDesign allows create a component in which you can stitch together HDL modules, HDL Cores, configures IPs, re-usable design blocks, Microchip primitives and lower level SmartDesign components, and other components types. A SmartDesign can be the top level of your design or a sub-module of your design. The **Files** tab lists your SmartDesign files in alphabetical order.

To build your design, perform the following procedure:

1. **Instantiating components:** This step is analogous to inserting design components onto the canvas. In this step you add one or more building blocks, HDL modules, components, and schematic modules from the Project Manager to your design. The components can be design blocks, IP cores from the Catalog, basic macros, design blocks, and other SmartDesign components files available in the Project Manager Design Hierarchy tab Component node or the Component tab into the Libero SoC project.
2. **Connecting bus interfaces:** In this step, you can add connectivity via standard bus interfaces to your design. This step is optional and can be skipped if you prefer manual connections. Components generated from the Catalog may include predefined interfaces that allow for automatic connectivity and design rule checking when used in a design.

3. **Connecting instances:** The Canvas allows create manual connections between ports of the instances in your design. Unused ports can be tied off to GND or VCC; input buses can be tied to a constant, and you can leave an output open by marking it as unused.
4. **Generating the SmartDesign component:** In this step, you generate the SmartDesign component HDL file. This component can be used by downstream processes, such as synthesis and simulation, or you can instantiate this SmartDesign component into another SmartDesign. When you generate your SmartDesign, the tool invokes the Design Rules Checker to verify the connectivity of your design. Undriven and floating ports, along with other Design Rule Check (DRC) violations, are reported in the Log/Message window. Any errors must be addressed before a component can be generated successfully. The design flow cannot proceed if a component used in the design is not generated.

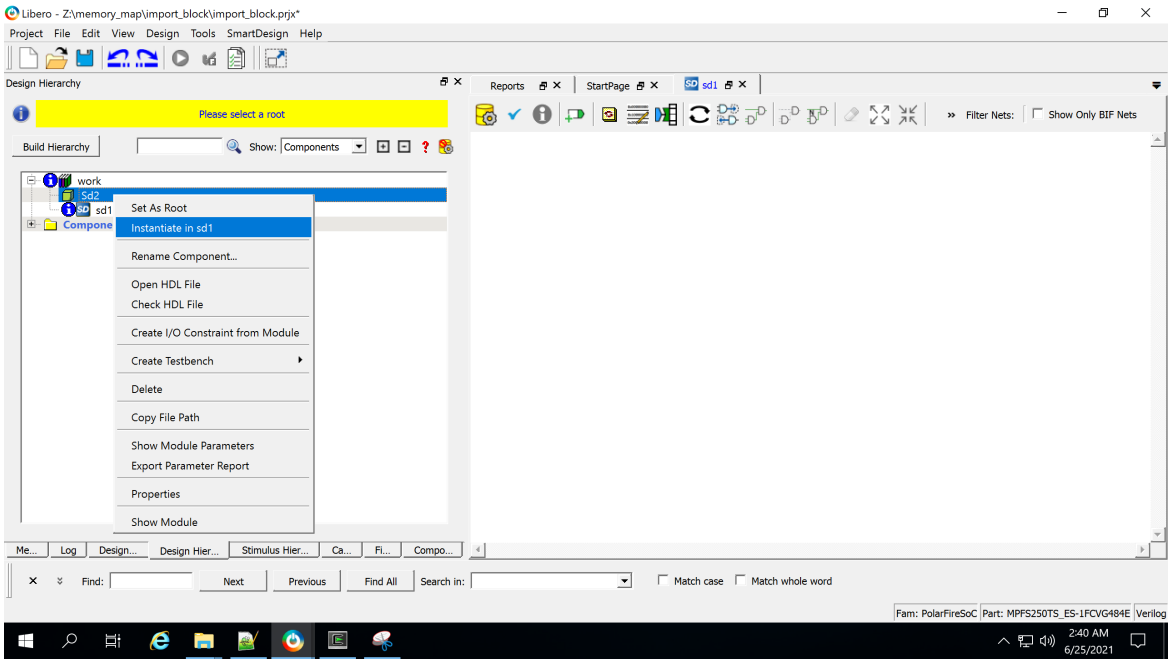
1.3 Instantiating Components into SmartDesign Canvas

For all the following design objects, drag and drop or right click **Object > Instantiate** to instantiate the design objects:

- IP cores—There are two methods for instantiating IP cores:
  - Drag the IP core from the IP catalog and drop in the SmartDesign canvas. This prompts to enter the name of a component; you can configure the IP and click on **OK**. The configured IP generates and a component creates, and further this component instantiates into the canvas.
  - In the IP catalog, right click on the core and chose the **Configure Core** menu, this prompts to enter the name of a component and you can configure the IP and click on **OK** a component generates. The component is available in the **Project Manager Design Hierarchy tab** or **Component tab** for drag and drop instantiation in the canvas.

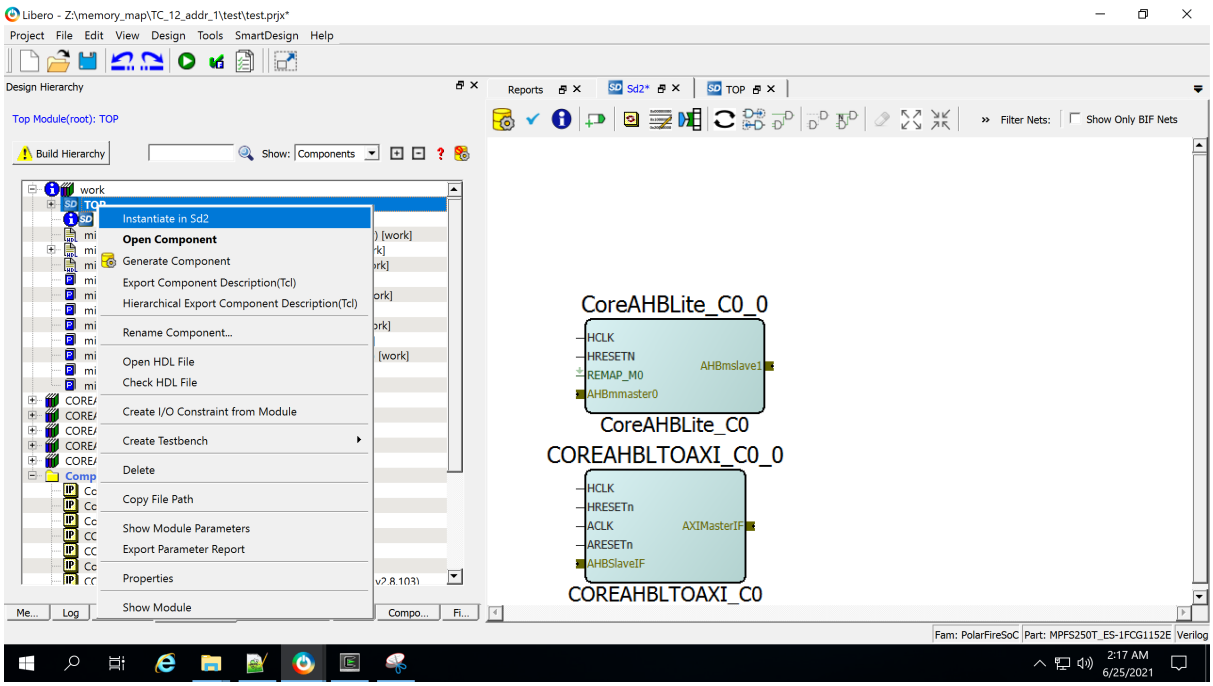
  IP cores displayed in the catalog as italics are cores that are available in Microchip IP Core Repositories, but are not yet downloaded to the vault (the disk location where downloaded cores are stored). Download the IP core prior to configuration and instantiation.
- HDL files—To instantiate HDL modules, drag the HDL module from the Design Hierarchy into the SmartDesign Canvas.
- HDL Cores—HDL cores are typically parametrized HDL modules with or without bus interface ports. An HDL core is created from an HDL module in the Design Hierarchy. It is used to generate a core has been generated out of it (right click **HDL file > Create Core from HDL**). Drag and drop the HDL core module into the SmartDesign canvas. Parametrized HDL cores are configurable inside the SmartDesign canvas. Open the configurator to set the values for the parameters. An bus interface may also be added to the HDL core, and it shows up in the SmartDesign with a bus interface pin that can be used to easily connect to the appropriate bus IP core inside SmartDesign Canvas.
- Design Blocks file—Drag and drop the design blocks from the Design Hierarchy into the SmartDesign canvas. Design blocks are components whose layout might have been completed in a different Libero SoC project and exported/published for use in a top-level design as a component with placement and optional routing information. Design blocks are typically use to control timing for design blocks that have very tight timing constraints that are difficult to meet within the full design. The design blocks must be imported into the current Libero SoC project to be instantiated in SmartDesign. The following figure shows how to instantiate a design block.

Figure 1-2. Design Block Instantiation



- SmartDesign Components—Another SmartDesign component (`*.cxf`) can be instantiated in the SmartDesign. Drag and drop the Smart Design component (`*.cxf`) from the Design Hierarchy into the SmartDesign canvas. Instantiation can also be performed by right clicking the module name in the Design Hierarchy and choosing **Instantiate**. The component (`*.cxf`) and its corresponding HDL files and IP cores must be imported into the current project and configured before instantiating in the new SmartDesign project.

Figure 1-3. SmartDesign Component Instantiation

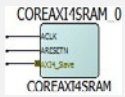
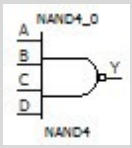
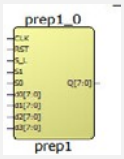
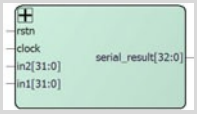
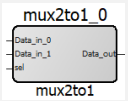
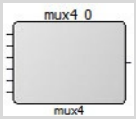


1.4 SmartDesign Canvas and Component Display

The SmartDesign Canvas window can be docked/undocked by clicking the icon. The canvas displays different component types with different colors. When mouse over the component, a tool-tip displays the type and name of the component. For IP Cores, the core version is also displayed.

The following table lists the component types and their appearance in the SmartDesign canvas.

Table 1-1. Component Type and Name in Canvas

Graphic Display	Component Type	Tool-tip Information
	IP Cores	Core: COREAXI4SRAM 2.1.105
	Basic Macros/Macro Library from Catalog	Macro: NAND4
	Design Blocks	Block: prep1
	SmartDesign Components	SmartDesign: adder_shift32
	HDL Module	HDL: mux2
	HDL Module	HDL Core: mux4

1.5 SmartDesign Tcl Commands

For details about the Tcl commands supported by SmartDesign, see the Tcl Commands Reference Guide.

2. SmartDesign Actions, Hotkeys, and Menu Items

This section describes the SmartDesign actions, hotkeys, and menu items.

2.1 SmartDesign Actions

Use the following list of actions across the top of the SmartDesign canvas to.

- Generate the HDL for the components
- Invoke design rule check
- Control the canvas display
- View memory map
- Manage synthesis attributes
- Save the SmartDesign to PDF

The following table lists the SmartDesign toolbar actions. So, mouse over the icon to view or see the action name in a tool-tip.

Figure 2-1. SmartDesign Actions Toolbar

Table 2-1. SmartDesign Actions

Action/Tool-tip	Description
Generate Component	Generates the SmartDesign component. Converts the visual design created into an HDL file that is used during synthesis and/or simulation of the design. Generating a SmartDesign automatically invokes the Design Rule Checker (DRC). DRC error messages are generated in the Message window. All errors must be fixed for a successful generation. Generating a SmartDesign components invalidates the synthesis state of the design if the component is used in that design.
Design Rule Check	Invokes the Design Rule Checker (DRC). You can invoke the checker at any time to validate the state of your design. If the design has DRC violations, errors appear in the Message window. **Note:** Design generation fails if there are any DRC violations.
Add Port	Adds a new top-level port to the design. A pop-up window appears to enter the name of the port and the direction (Input/Output/Inout). Input ports are added in the leftmost column of the canvas. Output and Inout ports are added in the rightmost column. Alternatively, right click the empty space inside the canvas and choose **Add Port**.
Manage Synthesis Attributes	Opens a split window in the canvas, which can be used to add or manage synthesis attributes or directives on the SmartDesign module, ports, nets, and instances.
View Memory Map	Opens the **View Memory Map** window. It shows the memory map of the current SmartDesign component. For each initiator in the design, the memory map shows the hierarchical Advanced Microcontroller Bus Architecture (AMBA) subsystem connectivity through buses and bridges to all. Targets are addressed by the Initiator.

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Action/Tool-tip	Description
Smart Search and Connect	Opens a split window in the canvas that enables you search for various items and make connections more quickly. This window lists the ports, pins, instances, and nets in the design, and allows you to filter, search, and select items and make a connection directly.
Reset Layout	Click to reset the layout view. Clicking this button removes all presentation information (position, size, highlights, and modified pin orders).
Auto-arrange Layout	Click to redo the layout of where components are placed on the screen. Only the location (x-y coordinates) of the instances and ports are changed. All presentation information remains intact.
Compress Layout	Click to push the instances and ports towards each other in order to remove extra white space between them on the screen. The relative positions of the instances on the screen are preserved. The result is a more compact display of the design.
Hide Nets	Toggle button. Click to hide nets and make them invisible on the canvas. All nets on the canvas are hidden. This button has precedence over net filtering and overrides all net filters. To hide some but not all nets, use the **Filter Net** widget at the rightmost of the toolbar. It hides net and their net names too (if present). When a net is hidden, the net stubs that the hidden net is connected to are still visible. Selecting the net stubs shows the RATS net connection of the net.
Show Nets	Toggle button. Click to show/hide nets. All nets on the canvas are shown/hidden. If nets are shown, all nets matching the net filter (at the far right of the toolbar) are shown.
Show/Hide Net Names	Toggle button. Click to show net names displayed alongside the net. Hiding net names makes the canvas less cluttered for big designs. Net names are always displayed in a tool-tip when the mouse is hovered on the net.
Unhighlighted All	Remove all highlighting of all design objects (nets, pins, ports, and instances) on the canvas. This option is active only if design objects are already highlighted.
Expand All Instances	Expand in place all SmartDesign components instantiated in the current SmartDesign to display within the current canvas, the next hierarchy down.
Fold All Instances	Collapse the hierarchy of all expanded SmartDesign instances.
Zoom In	Zoom in on the canvas.
Zoom Out	Zoom out the canvas.
Zoom to Fit	Adjust the zoom so that everything on the canvas fits within the visible view port with no extra empty space around the design.

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Action/Tool-tip	Description
Zoom to Selection	Click this icon and drag the mouse to draw a rectangle which, when released, causes a zoom in so that the visible view port area is approximately the size of the drawn rectangle.
Show Grid	Click to show a background grid behind the items on the canvas. If the grid does not appear when the button is clicked, zoom in until the grid shows. The grid pattern may not show if the canvas is zoomed too far out.
Add Note	Click to enter the Add Note mode. The next mouse click on the canvas opens a dialog box for entering the text and font size of the text (anchored at the mouse click location).
Save to PDF	Click this icon to open a dialog box that allows save a picture of all/part of the design to a PDF document.

2.2 SmartDesign Hotkeys

The following table lists the Hotkeys available in the SmartDesign canvas.

Table 2-2. SmartDesign Hotkeys

Hotkey	Description
CTRL + "w"	Maximize/Minimize the canvas work area.
CTRL + "+"/CTRL + = scroll wheel up	Zoom in (same as clicking the Zoom In button in toolbar or pressing CTRL+ mouse)
CTRL + "-"	Zoom out (same as clicking the Zoom Out button in toolbar or pressing CTRL + mouse scroll wheel down)
CTRL + "c"	Copy selected instances, ports, and nets with all their properties to the Clipboard.
CTRL + "v"	If there is a copy/cut information of an instance or port available in Clipboard, paste them. Cut data is removed from the source SmartDesign after paste.
CTRL + "x"	Cut selected instances, ports, and nets.
CTRL + "h"	Create Hierarchical SmartDesign out of the selected portion. 4.2. Creating Hierarchical Smart Design
CTRL + "k", CTRL + "f"	Open/close the **Smart Search and Connect** tool.
CTRL + "t"	Open/close the **Manage Synthesis Attributes** tool.
CTRL + "z"	Undo the last operation.
CTRL + "y"	Redo the last operation.
SHIFT + click	Click one item and SHIFT + click another item. The first clicked item, the second clicked item and all items of the same type between the first and second clicks are selected. This command is helpful when multiple items need to be selected for the same command (promotion to top-level/Add to group).
CTRL + click	Control + click is a toggle switch that selects or de-selects an item hovering your mouse cursor.

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Hotkey	**Description**
CTRL+SHIFT+click and drag	Selects a pin of an instance and drag it to a new location. This is not available for macros and expanded in place instances.

2.3 Click and Drag Operations

The following table lists the mouse click and drag operations available in the SmartDesign canvas.

Table 2-3. Mouse Click and Drag Actions

Mouse Actions	Description
Left-click and drag towards the top-left corner, and release.	Zoom in. The distance your cursor is dragged determines the magnitude of the zoom-in and is indicated by a positive integer in red.
Left-click and drag towards the top-right corner, and release.	Zoom out. The distance your cursor is dragged determines the magnitude of the zoom- out and is indicated by a negative integer in red.
Left-click and drag towards bottom left, and release	Zoom to fit. Change the display to fit the canvas view area snugly.
Left-click and drag toward bottom right, and release	Draw a rectangle on the canvas. Instances, pins and ports must be fully contained inside the rectangle to be selected. Nets partially inside the rectangle are selected.

3. SmartDesign User Actions

The SmartDesign tool has a rich set of menu items. Right click a design object to access the menu.

- Configure IPs
- Make connections between design objects
- Rename design objects
- Highlight design objects
- Traverse up or down the hierarchy of instances
- Assign attributes of pins/nets/buses.

The list of the available user actions varies with the design object. Some actions are common to all objects, while other actions are unique to a design object (net/instances/pins/ports).

Note: Port/Instance/Net names must contain only alphanumerical characters and underscores. Names, that are violating this rule, will not be accepted by the **Add Port** or **Modify/Rename** dialog box.

3.1 Net Actions

When a net or multiple nets are selected, the following actions are available in the right click menu.

3.1.1 Connect

This action combines all selected pins/ports to form a connection. Selecting a net is functionally equivalent to selecting all pins and ports to which this net is connected. This action can also be used to connect a net to another net if one of the nets is not driven.

3.1.2 Go to Driver

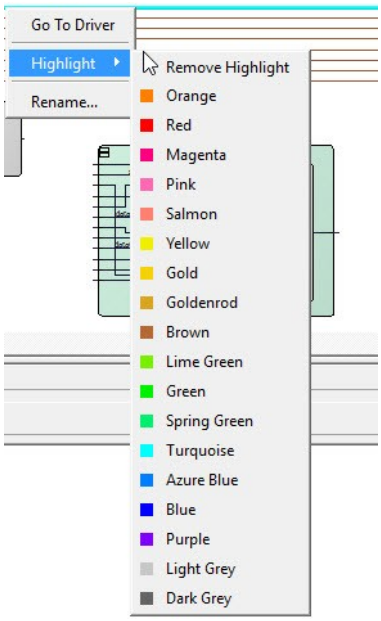
When a net is selected, the Go to Driver action centers the view on the net's driver pin/port, zooms away, and selects the net driver. Go to Driver traces the net to the driver at the local level of hierarchy. It does not traverse hierarchy. This action is not available when multiple nets are selected or the selected net has no driver. In the later case the net is displayed as a dotted line.

3.1.3 Highlight

Right click a design object (nets/pins/ports/bus interface/instance) to opens a menu of colors for highlighting. Clicking a color selects that color to highlight the selected design objects. If any design objects are already highlighted then highlighting a different color overwrites the previous highlight color. The highlight action is available when a single or multiple design objects are selected.

Note: Highlighting a net highlights the net and all the pins/ports (through the hierarchy) connected to the net.

Figure 3-1. Highlight Colors



To remove the highlight on a single design object, right click the design object and select **Remove Highlight**.

To remove all highlighted design objects, click the **Unhighlighted All** icon in the toolbar.

3.1.4 Rename

The rename action opens a dialog box for a new net name to be entered to replace the old name. Clicking **OK** changes the net name to the new net name if it is valid (for example, if it is not already used). Clicking **OK** prints an error in the Log window and the dialog box does not close if the name already exists or is invalid.

3.1.5 Delete

Deletes the net.

3.2 Instance Actions

When one or more instances are selected, the following actions are available in the right click menu.

3.2.1 Configure

If the instance is a SmartDesign component, the Configure action opens the SmartDesign canvas for edits. If the selected instance is an IP or HDL Core, the **Configure** button opens the Configurator dialog box for the core to be configured. If the selected instance is an HDL, the configure action opens the HDL file in the text editor. This action is equivalent to double clicking the instance. This action is available only when one single instances is selected.

3.2.2 Modify HDL

This action opens the instance's HDL source file in the text editor. Available only when an instance of an HDL Core is selected.

Note: This option is not available, for HDL modules. To open an HDL file, double click the HDL component on the SmartDesign canvas or right click the HDL component and choose **Configure**.

3.2.3 Highlight

This action opens a menu with multiple highlight color selections. Clicking that color selects that color to highlight the selected items. If any items are already highlighted then highlighting a different color overwrites the previous highlight color. The action is available when a single or multiple nets are selected.

Highlighting an instance automatically highlights the non-highlighted pins of the instance as well. Clicking the **Unhighlight all** icon in the toolbar removes the highlight color of all highlighted design objects, including highlighted nets.

This action is also available in the right click menu of low-level instances in the Expanded Inplace view.

3.2.4 Rename

This action opens the **Rename** dialog box that allows to rename the instance. If the instance name is valid, click **OK** to save the change and close the dialog box.

If the instance name is not valid or it already exists, when you click **OK**, an warning message appears in the **Log** window.

3.2.5 Delete

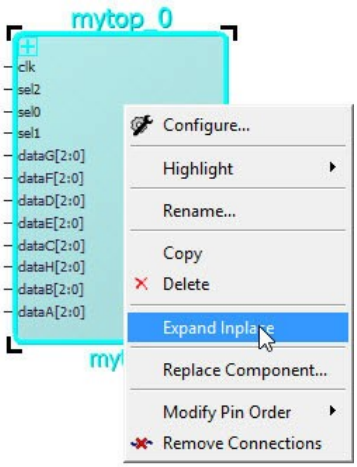
This action deletes the selected item. When multiple items are selected, all are deleted.

Note: Not all design objects can be deleted. Pad ports cannot be deleted.

3.2.6 Expand Inplace and Fold Instance

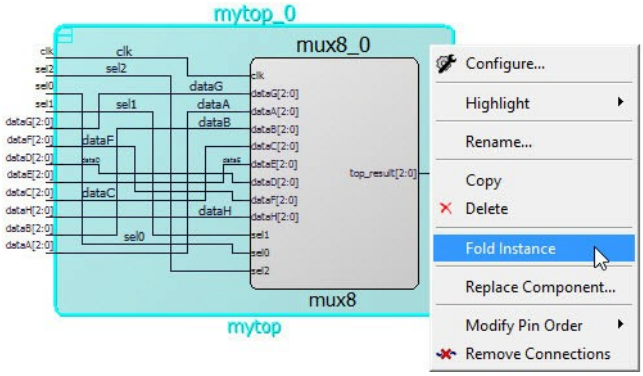
The Expand Inplace action is equivalent to clicking the **+** (Expand) sign in the top-left corner of the instance. It causes the selected instance to expand (to expose the next level of hierarchy for a SmartDesign component instance) in place. Only SmartDesign component instances can be expanded in place. If only one instance is selected, the view port zooms to the instance after the expand or fold is completed. This action is for SmartDesign components and is read-only. No changes can be made to the expanded hierarchy. Changes to the components at the lower level of hierarchy must be made by opening the low-level component directly. For more information, see Expand and Fold Instance.

Figure 3-2. Expand Inplace



The Fold Instance action is a toggle switch. It is equivalent to clicking the **-** (Fold) sign of an expanded instance. It causes the expanded hierarchy of the instance to collapse to the top level.

Figure 3-3. Fold Instance



3.2.7 Replace Component

This action brings up the Replace Component for Instance(s) dialog box. The Instance(s) section shows the below information:

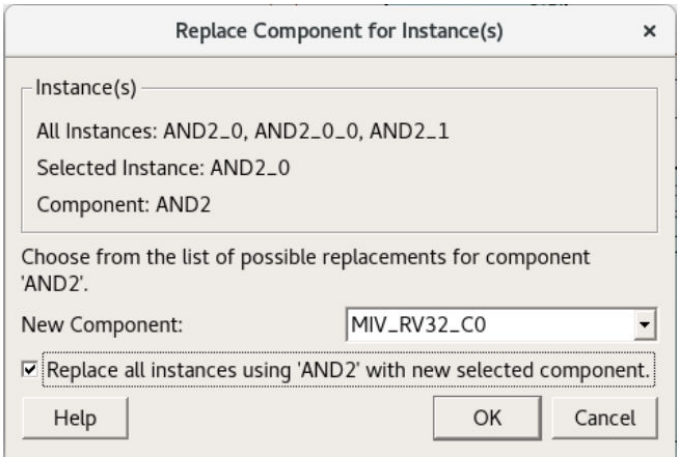
- All instances: All the instances related to the selected instance will be replaced.
- Selected Instance: The selected instance that needs to be replaced.
- Component: The component related to the selected instance.
- Users can choose the **New Component** from the drop-down list.
- On selecting **Replace all instances using <component_name> with new selected component** option and clicking **OK** replaces every instance of that component in the current design with an instance of the **New Component** that was selected.
- All pins that have the same name on the new component keeps their connections, whereas pins that no longer exist loses their connection and a warning prints in the Log window. The dialog box closes.

If the **Replace all instances using <component_name> with new selected component** option is unchecked, only the selected instance will be replaced.

Note: The **Replace all instances using <component_name> with new selected component** option is selected by default.

Selecting an instance and clicking **OK** for a non-valid component closes the dialog box and prints an error in the Log window.

Figure 3-4. Replace Component Dialog Box



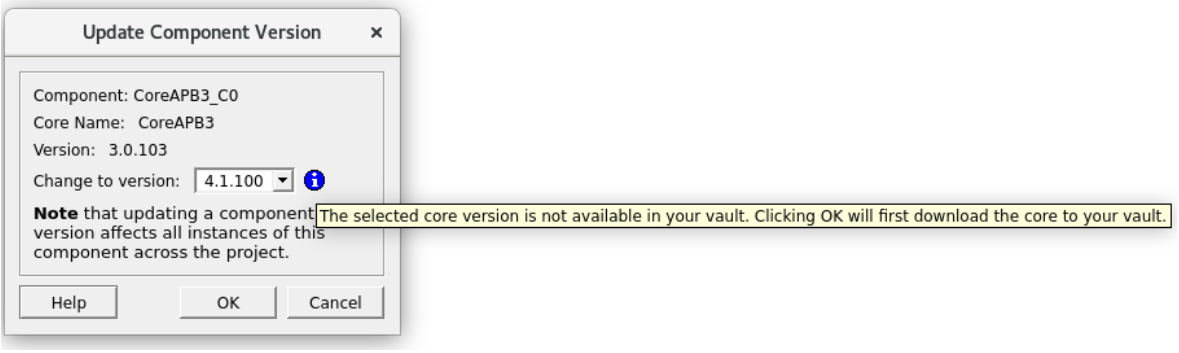
3.2.8 Update Component Version

The Update Component Version dialog box enables you to update a component of an instance with another version. You can restore or update your component without creating a new instance or losing your connections.

To update a component version in your design:

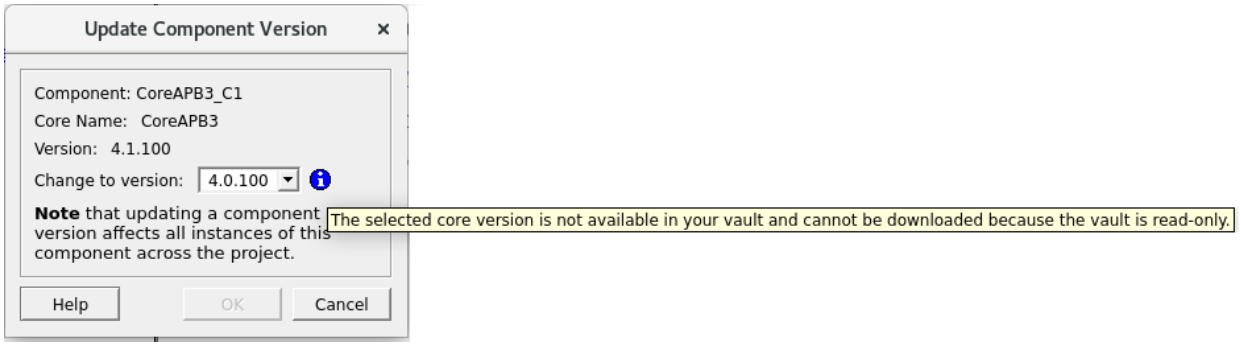
1. Select the component in the Design Hierarchy or from the SmartDesign canvas, right click and choose **Update Component Version**. The Update Component Version dialog box appears, (as shown in the following figure).

   Figure 3-5. Update Component Version Dialog Box



2. In the **Change to version** drop-down list, select the version you want to update it with and click **OK**. On clicking **OK**, the core downloads automatically to the vault and the component in the SmartDesign canvas updates with the version selected as it appears in the tool-tip in the figure above.
   If the vault is read-only, selecting remote core renders the **OK** button inactive and displays the following tool-tip message as shown in the figure below.

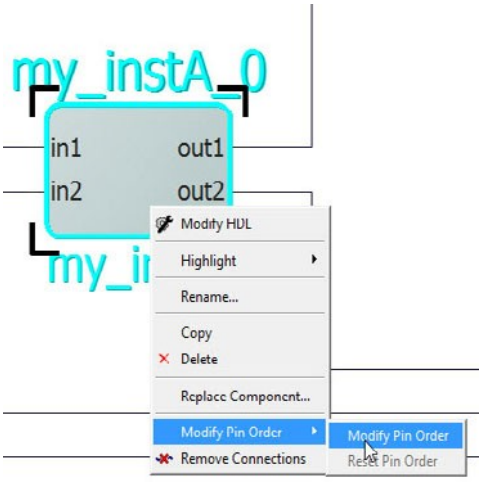
Figure 3-6. Update Component Version Dialog Box - Read-Only Vault



3.2.9 Modify Pin Order

This a toggle switch. Right click an instance to open the drop-down menu. Select **Modify Pin Order**. A pop-up window provides instructions on how to reset pin order. The **Modify Pin Order > Modify Pin Order** menu provides instruction on how to modify the pin order on an instance. Press CTRL+SHIFT and click to select the pin you want to move.

Figure 3-7. Modify Pin Order



Drag the mouse to a new location and release the mouse. The pin is moved to a new location. By default, input pins are on the left of the instance while output pins/inout pins are on the right. **Modify Pin Order** allows place the pins on any one of the four sides of the instance. A pin that has been moved away from default locations is identified by a bold arrowhead. An inward-pointing arrowhead indicates an input pin and an outward-pointing arrowhead indicates an output pin. Inout pins do not have an arrowhead when they are moved away from the default locations (right side of instance).

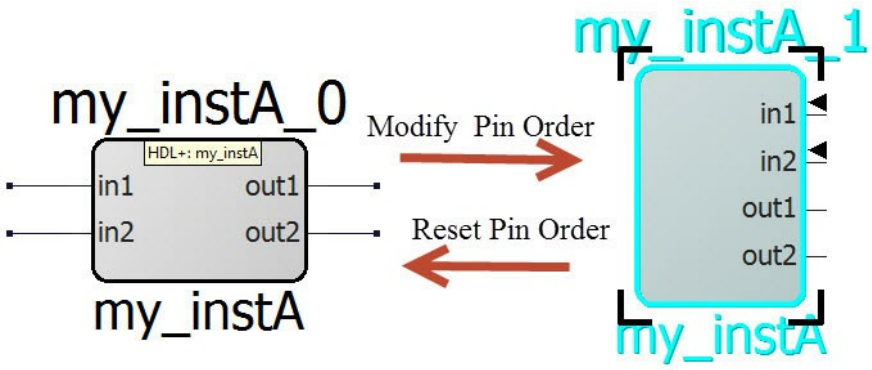
Note: If there are two instances on the canvas that communicate with each other in a way where the outputs of one component instance A communicates with the inputs of another component instance B and vice versa, modifying the pin order gives a less cluttered view of the SmartDesign component. See Modify Pin Order Before Connections for details.

Note: **Modify Pin Order** is disabled when the instance is expanded in place. The modified pin order may not be preserved when an instance is expanded but will retain the set order when folded.

3.2.10 Reset Pin Order

The Modify Pin Order > Reset Pin Order menu action and resets the instance pin order to its default order.

Figure 3-8. Modify/Reset Pin Order



3.2.11 Remove Connections

This action disconnects all pins that can be disconnected from nets. Pins that cannot be disconnected (for example pins connected to pads) are logged in the Log window.

3.2.12 Help

Opens the handbook, release notes, or configuration user guides for the core.

3.3 Pin/Port Actions

Right click a pin or a port and the drop-down menu appears. Not all actions appear for every port/pin.

3.3.1 Connect

The Connect action adds a net to the design that connects the selected pins/ports. This is the only pin/port action that takes selected nets into account. Selecting a net works as if you selected all of the nets connected pins/ports.

3.3.2 Disconnect

This action disconnects all selected non-pad pins/ports from their attached net if it is allowed (not violating the DRC rules).

3.3.3 Promote to Top-Level

This option is available to input/output/inout pins (scalar and bus), slices, and Bus Interfaces (BIF). It creates a top-level port and a net connecting the top-level port to the pin or slices. If a port with that name already exists, a new unique port name is created.

Note: When promoting BIF pin to top, all the BIF port members are renamed to include port's name as a prefix:

```
[BIF_name]_member_name
```

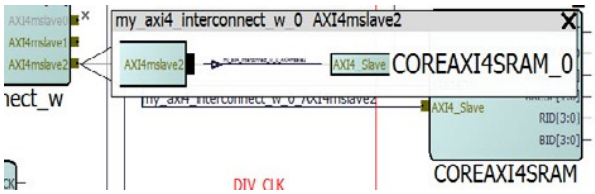
3.3.4 Go to Driver

This action centers on zoom around, and selects the driver of the pin/port. This action is not available for output pins and top-level input ports. The driver cannot be an inout.

3.3.5 Magnify Pin

This action opens the Magnify window to display connection information (driver/load) about the pin. It is equivalent to double clicking the pin.

Figure 3-9. Magnify Pin Window



See Magnify Pin for details.

3.3.6 Highlight

This action opens a menu with multiple highlight color selections. Clicking a color selects that color to highlight the selected items. If any items are already highlighted then highlighting a different color overwrites the previous highlight color. The action is available when a single or multiple pins/ports are selected.

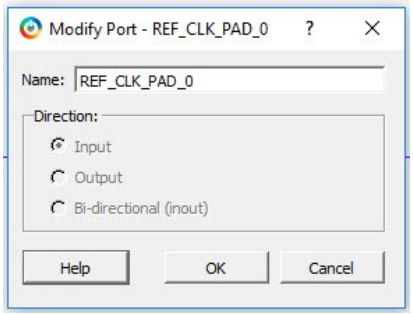
Clicking the **Unhighlight all** icon in the toolbar removes the highlight color of all highlighted design objects, including highlighted pin/ports.

3.3.7 Modify and Rename

This action opens a Modify Port dialog box. It allows the top-level port name and the range to be changed.

Note: When renaming bus interface (BIF) port, all the member ports that have BIF name prefix can also be renamed.

Figure 3-10. Modify/Rename Dialog Box



3.3.8 Delete

This action deletes all selected items that can be deleted: slices, groups, group members, and top-level ports.

The delete action deletes all items selected, even if the selected items are of different types. When a group member is deleted, the member is deleted from the group only. The actual pin is not deleted.

3.3.9 Expanding and Collapsing Bus

Expanding a bus displays the slices of the bus and collapsing the bus hides the slices. Slices with net connections cannot be hidden and cannot be collapsed into the bus.

3.3.10 Flip Bit Order

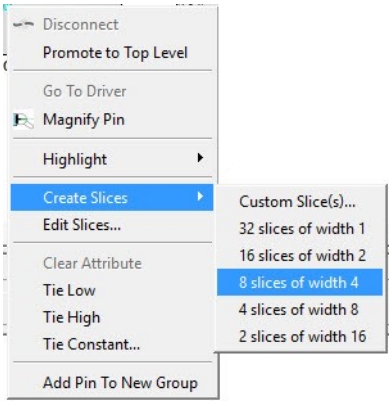
This option is available only to slices. It allows flip the upper range (MSB) and lower range (LSB) of the slice. All connection/tieoff information and presentation information are retained.

3.3.11 Create Slices

Open a menu of slice options that can be created from the bus pin/ports. A custom slice option to create any slice/bit combination of your choice and the more common possible combinations of slices are available. For example, using a 32-bit bus with the Custom Slices option allows the creation of any slice/bit combinations (for example., a slice of 10 bits and another slice of 22 bits). To make it convenient to create slices, common, off-the-shelf bus slices are listed in the drop-down menu; for example:

- 32 slices of width 1
- 16 slices of width 2
- 8 slices of width 4
- 4 slices of width 8
- 2 slices of width 16

Figure 3-11. Slice Creation for a 32-bit Bus



On a components bus pin the slices expands by default.

The directions of the slices (input/out) are indicated by an arrowhead.

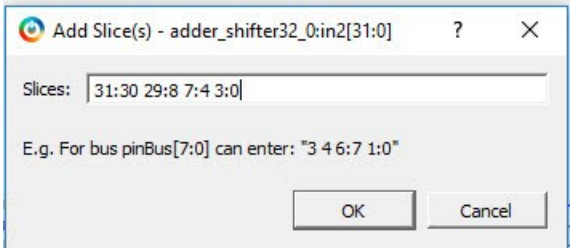
On a top-level bus port the slices places in a column below the bus port.

Note: If slices exist before new off-the-shelf slices are created, the existing slices are deleted first before new ones are created.

3.3.12 Custom Slices

This option opens a dialog box for entering a list of slices. If these slices are all valid, they are added to the bus. If the slices are not valid (for example, slice bits already exist and used in an existing slice), the error is reported in the Log window. The dialog box supports any separator character except colon because the colon is used to specify a range. No characters other than the colon are allowed to be adjacent to the two-range indices.
Note: Creating a custom slice does not delete pre-existing slices.

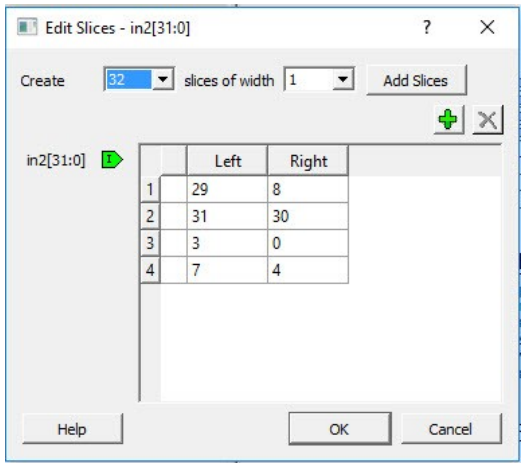
Figure 3-12. Custom Slices Dialog Box



3.3.13 Edit Slices

The Edit Slice option opens the Edit Slices dialog box. It allows existing slices to be modified.

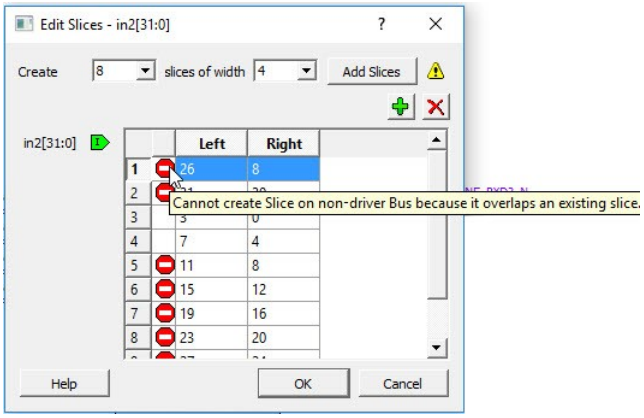
Figure 3-13. Edit Slices Dialog Box



Use the dialog box to change the range of the bits, add a slice or delete a slice. Modifying the slices and clicking **OK** initiates the changes if they are valid and closes the dialog box.

Modifying the slices and clicking **OK** prints an error in the Log and closes the dialog box if the changes are not valid. Some error messages may be reported in the Edit Slice dialog box. Hover your mouse cursor over the error icon to display error details.

Figure 3-14. Tool-tip and Error Message



3.3.14 Clear Attributes

This action clears the pin attributes (Tie to High/Low/Constant or Inversion/Marked Unused).

3.3.15 Mark Unused

This is available to the output pins (scalar and bus) of a component instance. This action specifies the pin/port as unused so it can pass DRC check without being connected.

3.3.16 Invert

This action inverts the input/output scalar pin and port. A bubble is added to indicate inversion.

3.3.17 Tie High and Tie Low

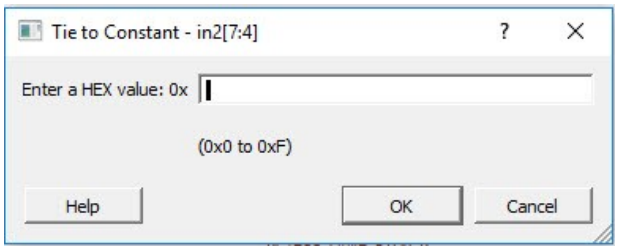
The Tie High action connects the pin (scalar and bus) to VCC. For a bus pin this action deletes all slices. For a group this action is applied to all non-output member pins in the group.

The Tie Low action connects the pin (scalar and bus) to Ground. For a bus pin this action deletes all slices. For a group this action is applied to all non-output member pins in the group.

3.3.18 Tie Constant

This action is available only to bus pins and slices (except single-bit slice). It opens the Tie to Constant dialog box for a constant value in HEX to be entered for the bus pins and slices. Only valid values entered in HEX within parenthesis are allowed.

Figure 3-15. Tie to Constant Dialog Box



3.3.19 Add Pin to New Group and Add Pin to Group

This menu item is available to instance pins. If a group is selected first, right click a pin and choose **Add Pin to Group** to add the pin to the selected group. If no group is selected first, the menu item is called **Add Pin to New Group**, a new group with the default group name Group/Group_1/Group_2/Group_3/ and so on is created, and all selected pins are added to the newly created group.

A pin group can be expanded to display the member pins or collapsed to hide the member pins. Member pins connected to nets cannot be hidden and cannot be collapsed into the group. Only member pins (in a pin group) with Pin Attributes (Tie high/low/marked unused) can be hidden and collapsed into the pin group.

3.3.20 Rename (Group)

This is available only to group pins. It opens the Rename Group dialog box for the group name to be changed. If a valid name is entered, click **OK** renames the group. The new name field defaults to the current group name if no new name is entered in the dialog box.

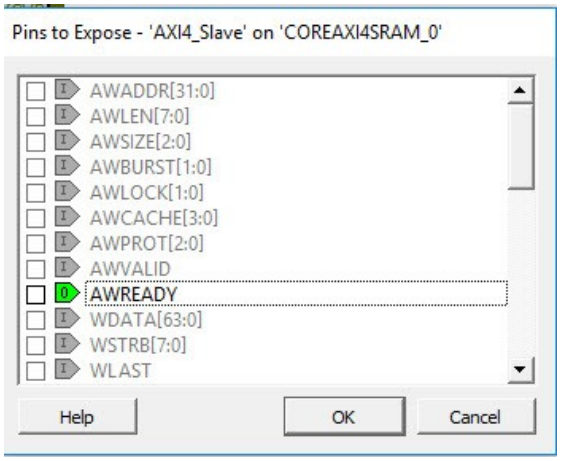
If an invalid name is entered or a pin with that name already exists, click **OK** prints an error in the Log and closes the dialog box.

3.3.21 Show and Hide BIF Pins

This opens the Show Pins to Expose dialog box to display all the Bus Interface Pins available to be exposed or hidden from the instance. Check the pins in the BIF you want to expose and uncheck the pins you want to hide. Hidden pins are not exposes on the interface.

Note: Not all pins can be exposed. The pins that can be exposed depends on the BIF. If the BIF is connected already, none of the input pins can be exposed. If the BIF is not connected, every item in the menu can be exposed.

Figure 3-16. Show to Expose Dialog Box



3.4 Copy, Cut, and Paste

This section describes copy, cut, and paste function within SmartDesign or cross SmartDesigns. The following functionalities are included in SmartDesign:

- Copy and paste
- Cut and paste
- Copy name

3.4.1 Copy and Paste

This function allows copy and paste SmartDesign objects within or across SmartDesigns. Following is the flow:

1. Select any portion of SmartDesign (ports, instances, and nets).
2. Right click any selected objects, and click **Copy** or press**Ctrl + C**.
3. Find any SmartDesign and right click the canvas.
   Note: The Paste button actives if there is at lease one instance or port copied.
4. Click **Paste** or press **Ctrl + V**.
5. The objects are pasted here from the source SmartDesign.

The **Copy** menu action is instance and port driven so individual nets cannot be copied and pasted. When instances and ports are copied, the metadata is not added to the Clipboard, which means that if an original object gets removed, the paste option fails. Users can select multiple instances and/or ports, right click them, and click **Copy** or press **CTRL+C**. Instance, port, and net data are copied to the Clipboard.

Note: **Copy** does not keep object metadata in the Clipboard. Therefore if the original object gets deleted, the paste fails.

Use **CTRL + V** or by just clicking the **Paste** menu action to copy the data on the current SmartDesign canvas. The Copy and Paste keep all the instance/pin/port attributes, names, and properties.

Note: Selected nets are ignored. All nets connected to the selected instances and ports are used instead when doing copying across SmartDesign canvases.

Figure 3-17. Copy Menu Action

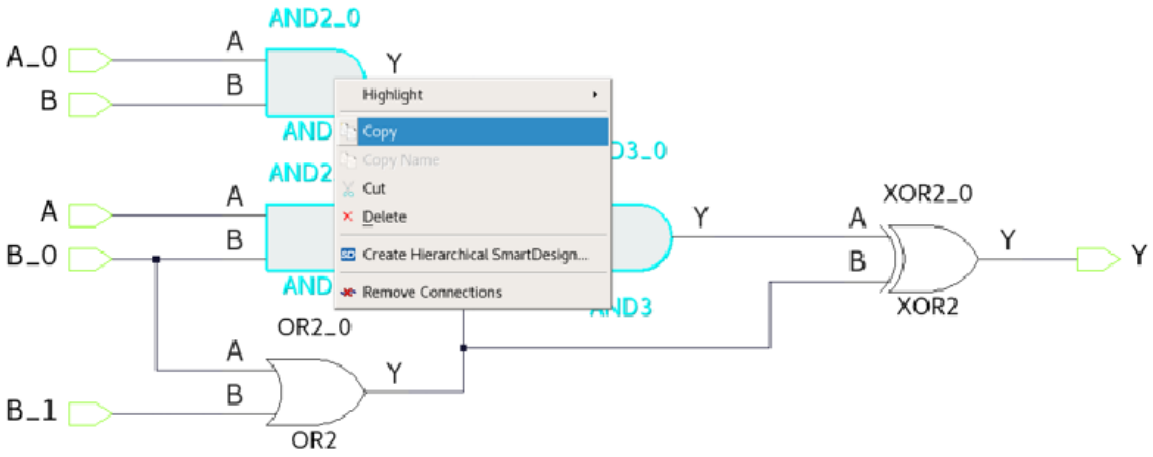
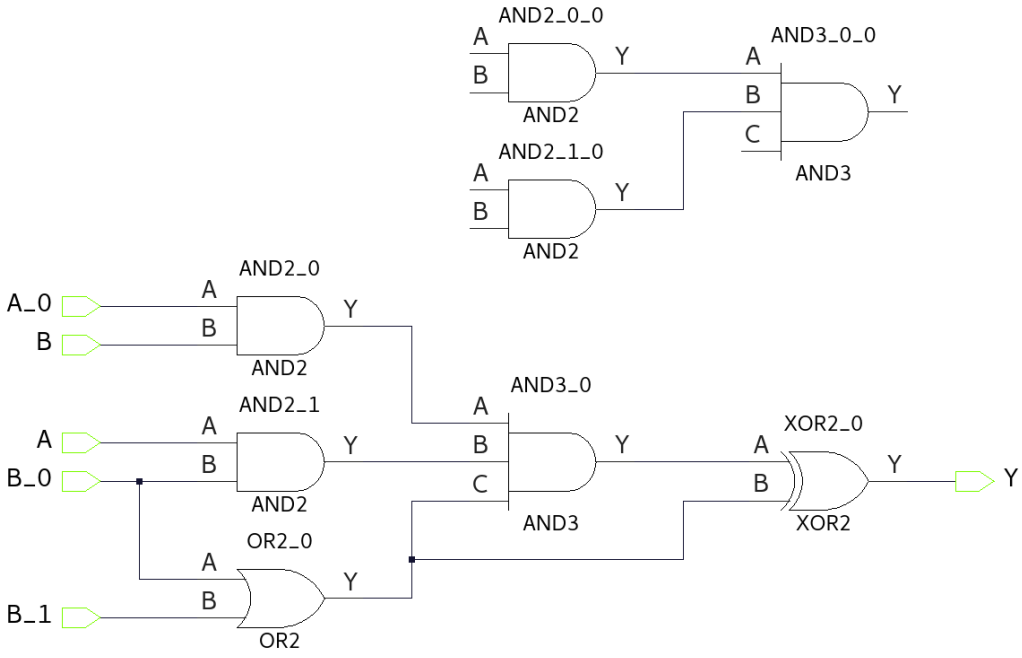


Figure 3-18. SmartDesign (Copy and Paste AND Gates)



3.4.2 Cut and Paste

This function allows to cut and paste SmartDesign objects across SmartDesigns. Following is the flow:

1. Select any portion of SmartDesign (ports, instances, and nets)
2. Right click any selected objects and click **Cut** or press **Ctrl + X**.
3. Selected objects become inactive (highlights in Light Gray color).
4. Go to any SmartDesign and right click on the canvas.

Note: The Paste button actives if there is at least one instance or port copied.

5. Click **Paste** or press **Ctrl + V**.
6. Selected objects appear in the current SmartDesign and are removed from the source SmartDesign.

The **Cut** menu action is instance and port-driven, individual nets cannot be cut and pasted. Users can select multiple instances and/or ports, right click them, and click **Cut** or press **Ctrl + X** hotkeys. Instance and port data are copied to the Clipboard. Net data is retained from the instances and ports.

Note: **Cut** does not keep object metadata in Clipboard. Therefore, if the original object is deleted, paste fails.

Press the **CTRL + V** hotkey or click the **Paste** menu action to paste the Copied data. The Cut&Paste deletes the original object after pasting them.

Note: Cut data is highlighted in "Light Gray" color. Press the **Esc** key to clear everything from the Clipboard and to remove highlights.

Note: **Cut** action does not keep the object meta data in the Clipboard, which means that if the original object gets deleted, the paste fails. There is no ability to undo Cut and Paste.

Figure 3-19. Cut Menu Action

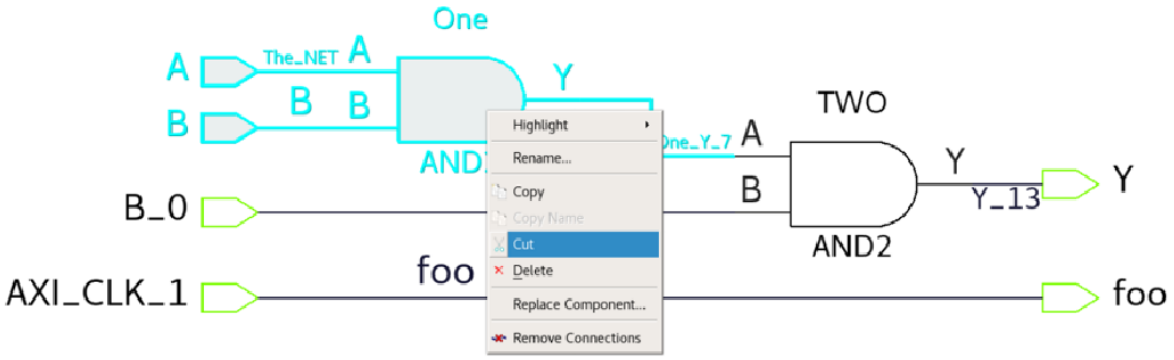
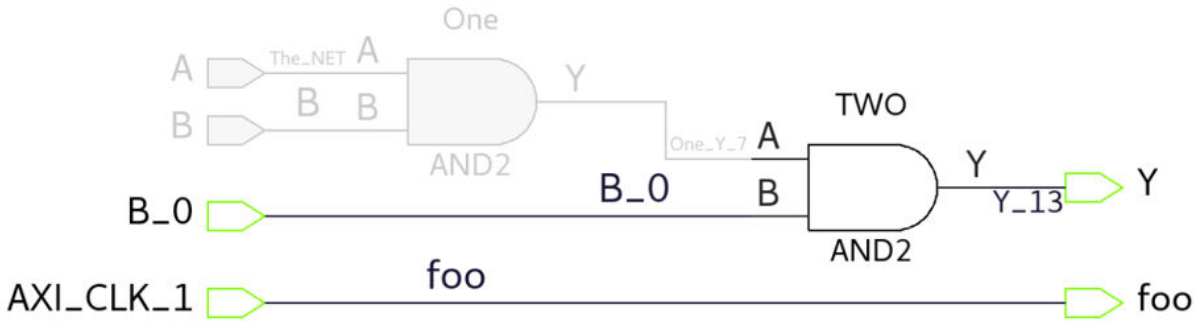


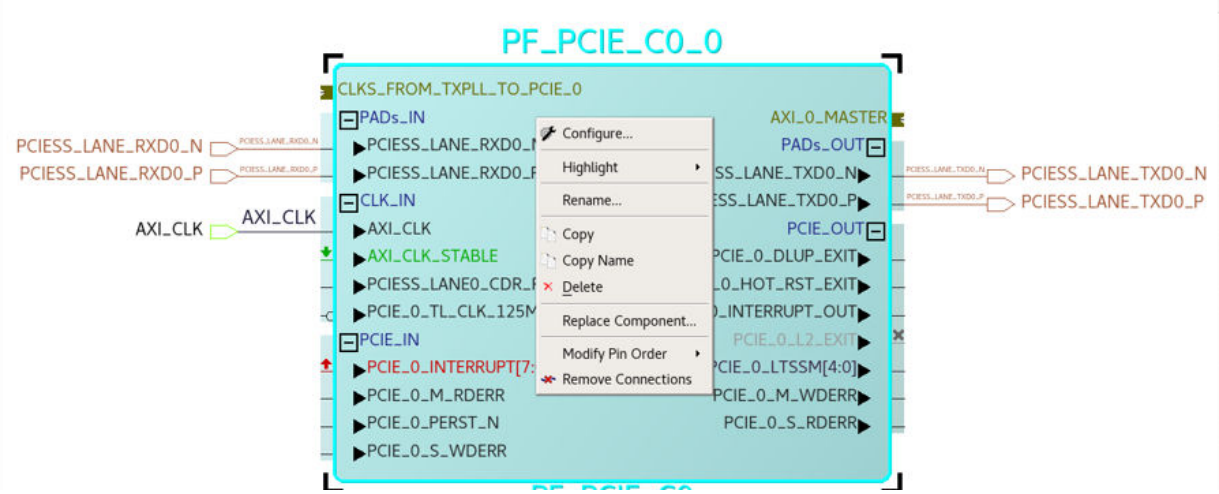
Figure 3-20. Cut Data (AND Gate with Tow Ports - Highlighted in Light Gray)



3.4.3 Copy Name

The **Copy Name** menu action is available for all types of SmartDesign objects: instances, pins, ports, and nets. This action copies the current selected item's name to the Clipboard. When multiple objects are selected, the button becomes inactive.

Figure 3-21. Copy Name Menu Action



3.4.4 Best Practices

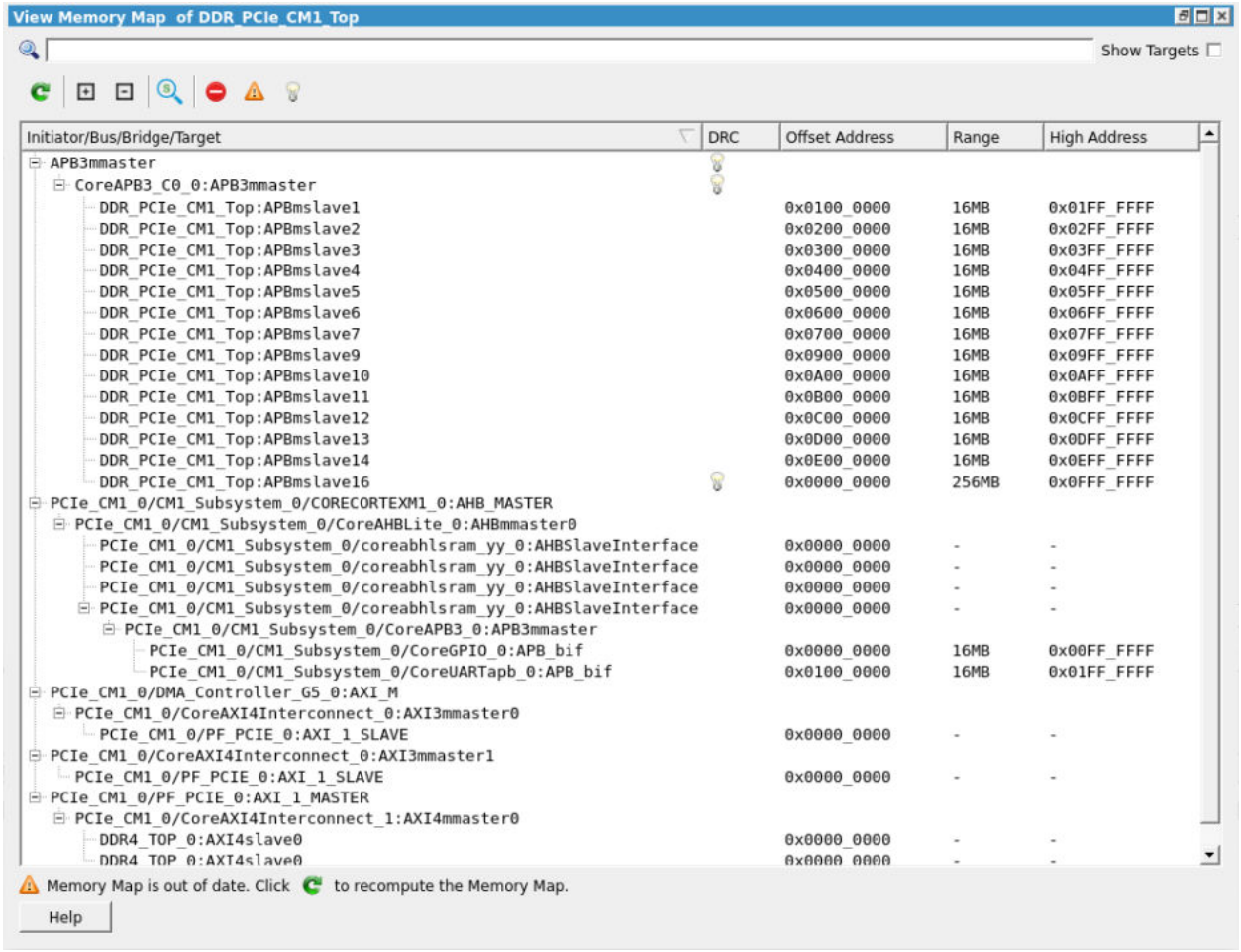
Make sure to follow these best practices using copy, cut, and paste:

- Pad ports and pad nets cannot be copied/pasted.
- Hierarchy instances can also be copied/pasted.
- All the port attributes (tie-off values, inversions) are restored after pasting.
- While copying a bus port, all the slices are copied as well. Slice port cannot be copied individually.
- In the Copy/Cut and Paste TCL commands, bus port names need to be specified without range. Names like "bus_name[10:1]" are treated as invalid.
- Cut and paste do not have an Undo option.
- Cut and paste within a SmartDesign will not do anything.
- Cross Libero copy/cut/paste is not supported.

3.5 View Memory Map

The View Memory Map window constructs the memory map corresponding to various initiators in the SmartDesign component and displays the hierarchy in a tree format. To open the window, right click anywhere on the SmartDesign canvas and select **View Memory Map**. Click the **View Memory Map** icon  in the toolbar at the top of the canvas.

Figure 3-22. View Memory Map Window



This window shows the memory map starting from an initiator in the design to targets connected through bus and bridge cores hierarchically. There can be various types of bus and bridge cores in the hierarchy between the initiator and the targets.

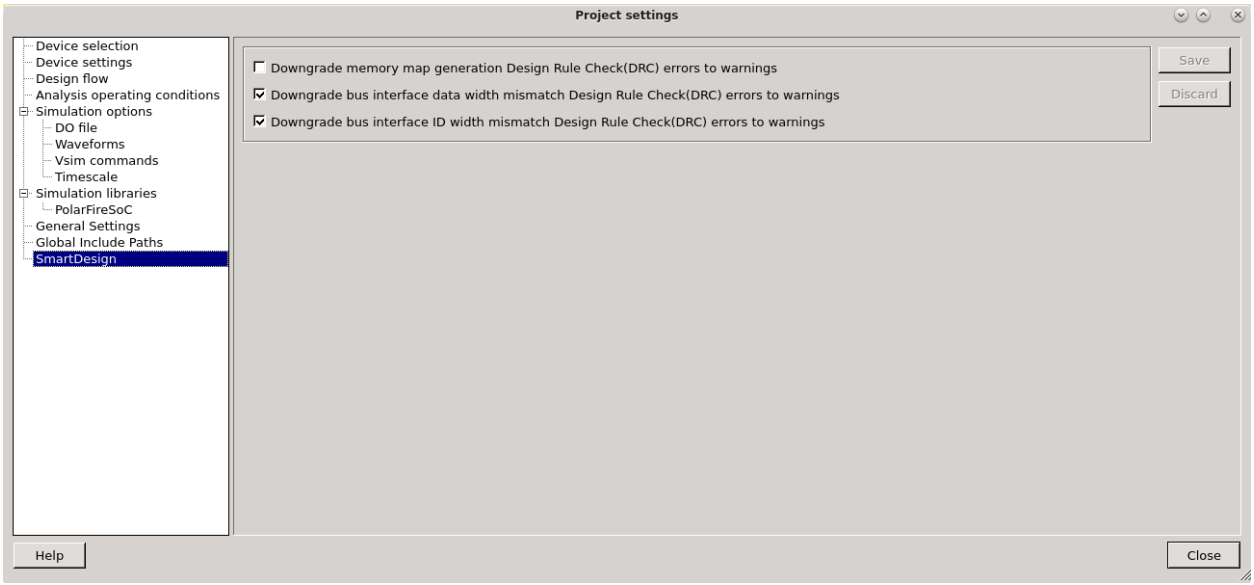
- Initiator Node > Bus > Bridge > Bus > Targets
- Initiator Node > Bus > Targets

Note: The memory map also considers initiators, bus and bridge cores, and targets that are present in other SmartDesign components, which are instantiated under the current SmartDesign's hierarchy.

Each target in the memory map is shown with an Offset Address, Range, High Address, and Design Rule Check (DRC). If DRC exists, an Error or a Warning icon with a tool-tip message is shown. DRC is flagged if a target cannot be accessed completely or partially by the initiator's address space.

If there are any DRCs in the Memory Map corresponding to a Smart Design component and its hierarchy, they are flagged when the SmartDesign component is generated and is printed as messages to the Libero log window. If the DRC are warnings, the SmartDesign component generation passes; however, if the DRCs are errors, the SmartDesign component generation fails. There is an option to downgrade Memory Map DRC errors to warnings and let the SmartDesign component generation to go through without failing.

Figure 3-23. Downgrade Memory Map Generation Design Rule Check (DRC) Errors to Warnings



Note: If Memory Map errors are downgraded to warnings using preceding preference check box, DRC warning targets can not be accessed by the initiator. Check each DRC warning and ensure there are no issues before going further in the design flow.

Note: In PolarFire® SoC MSS based designs, the Fabric Interface Controllers (FICs) FIC_0 and FIC_1 have two regions each, 64 GB and 512 MB. A target accessible by the Coreplex via one FIC region may not be accessible in the other FIC region based on the address spaces and bus configurations. This is a valid design scenario and must not be flagged as an error in the Memory Map DRC section. Therefore, a Memory Map DRC error that is seen in both the regions (64 GB and 512 MB regions) of a FIC stays as an error, and if the DRC error is seen only in one of the two regions of the FIC, it is automatically downgraded to a DRC warning, both in the Memory Map and SmartDesign component generation.

Navigation Actions and Filters

The **View Memory Map** window also provides new buttons and filters at the top of the window for easy navigation and ease of use.

Figure 3-24. View Memory Map Window Actions and Filters

- Search

  You can search for a specific initiator, bus, bridge, and target in the memory map by specifying a full or partial name in the search box.
- Show Targets

  Shows all the initiators and targets under them in the design in a flat hierarchy with their start addresses, ranges and DRCs if any. The initiators, bus, and bridge cores are not shown.
- Refresh

  Updates the content of the Memory map. It becomes active only when something is changed on canvas.
- Expand

  Expands and shows the full hierarchy of all initiators in the memory map starting from the initiator to the targets.
- Collapse

Collapses the full hierarchy of all initiators in the memory map and only shows the top-level initiators in the window.

- Zoom and Center

  Toggle action. If checked, the canvas zooms to the selected item after every selection.

- DRC Filters
  It filters the DRC messages, if any. It categorized the message on the basis of severity: error, warning, and information.

Additional Memory Map functions allow you to sort items by their Offset or High addresses and ranges.

Click the columns of the header to sort the items in ascending or descending order.

Click the first column of the header to see the initial view of the table.

Exporting Memory Map Report

The memory map can also be exported to a JSON or HTML file. Select the **Memory Map Report** option from Libero **File > Export**. In the **Export Memory Map Report** window, you can specify the SmartDesign component for which you want to export the memory map report. Click on the **Browse** button in the window to specify the memory map report file name, type (`.json` or `.html`) and location on disk. A `.json` or `.html` format memory map report file (which can be opened in a web browser or a json viewer in a text editor) is created when you click the **Save** button.

Figure 3-25. Libero Option to Export Memory Map Report

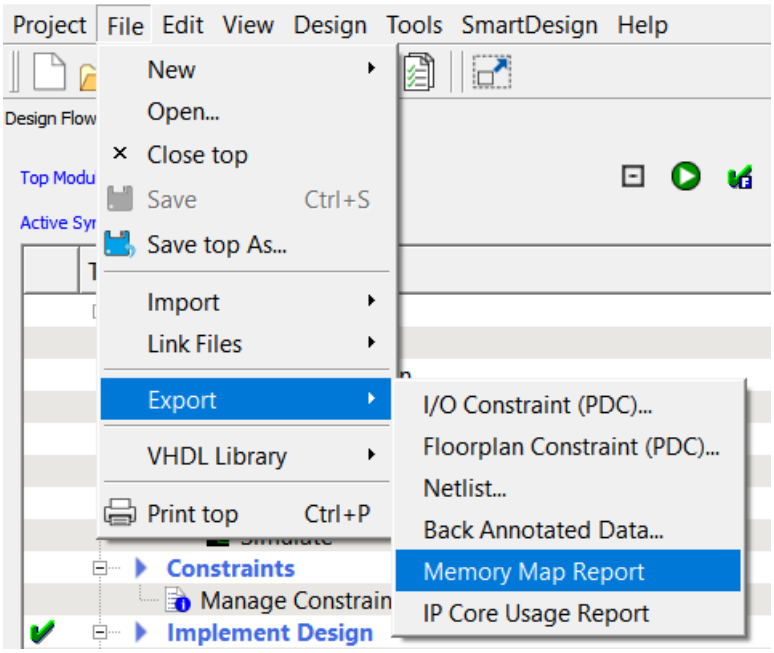


Figure 3-26. Export Memory Map Window (.json format)

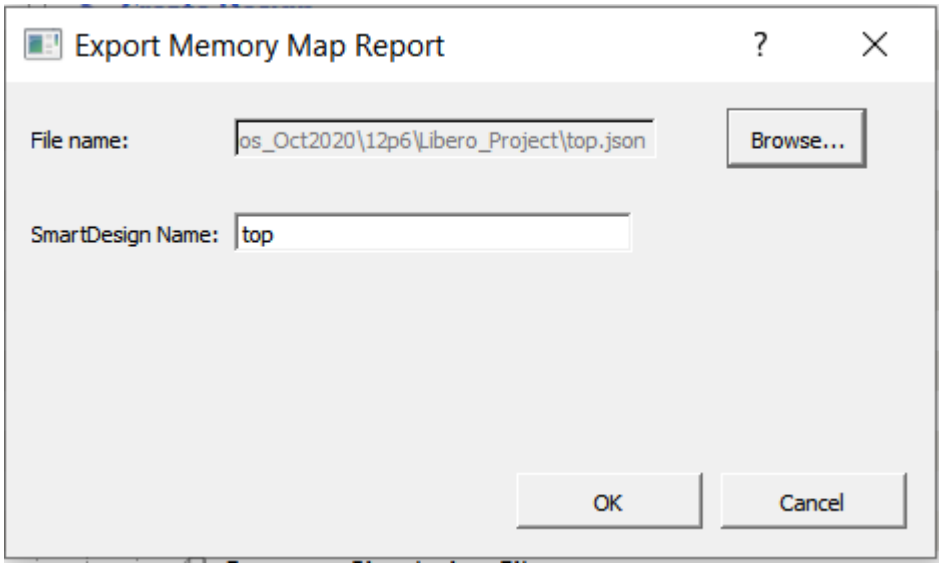


Figure 3-27. Export Memory Map Window (.html format)

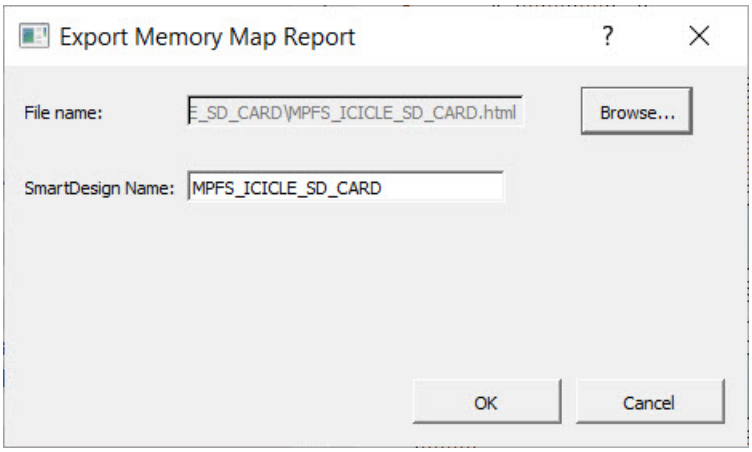
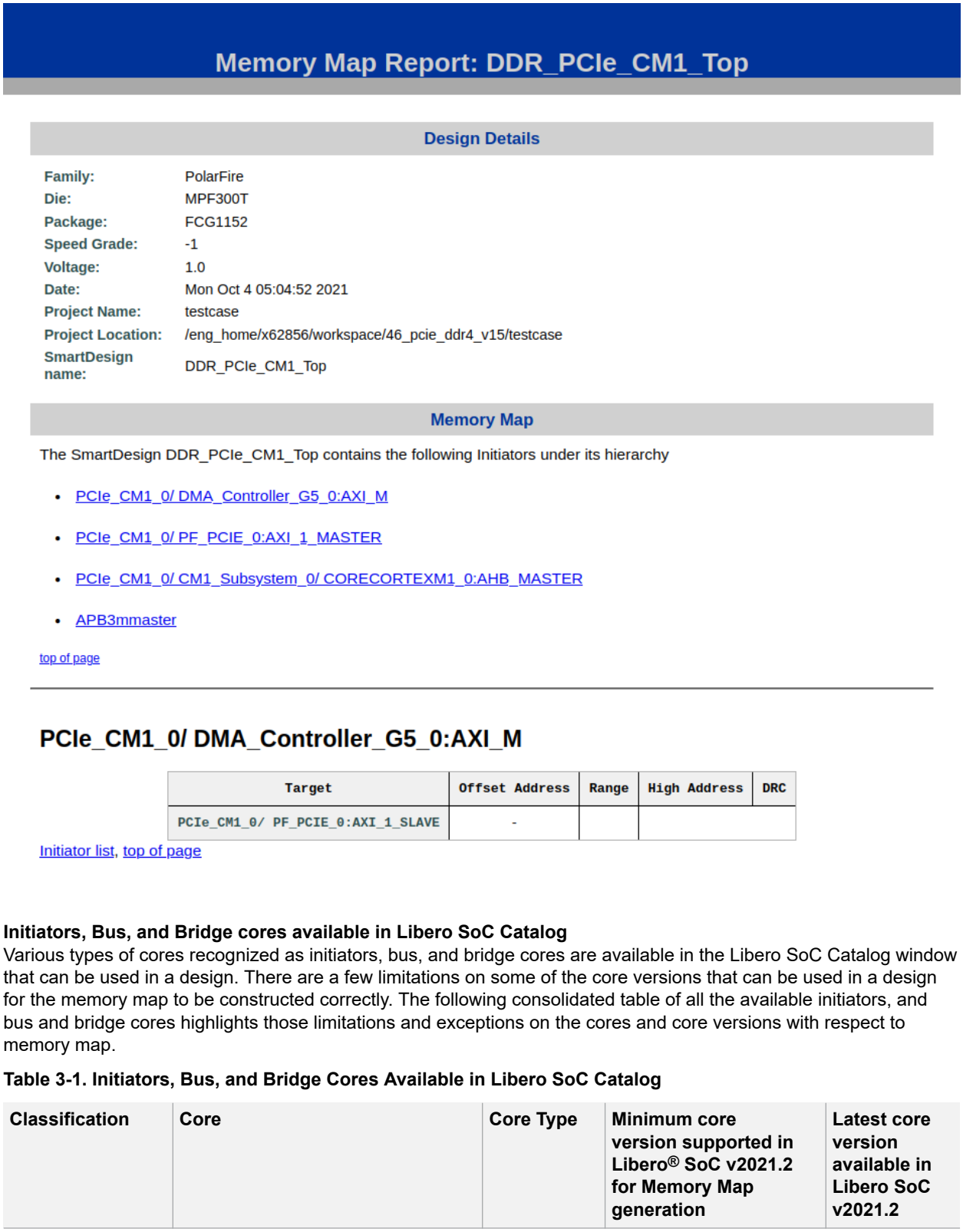


Figure 3-28. Sample Memory Map Report (.json format)


```
{
    "title": "Memory Map Report",
    "date": "Mon Oct  4 05:04:19 2021",
    "project_name": "testcase",
    "project_location": "/eng_home/x62856/workspace/46_pcie_ddr4_v15/testcase",
    "SmartDesign name": "DDR_PCIe_CM1_Top",
    "Initiator/Bus/Bridge/Target OffsetAddress Range HighAddress":[
    {"Node name":"APB3mmaster",
    "Type":"Initiator",
        "Connected Node":[
            {"Node name":"CoreAPB3_C0_0:APB3mmaster",
            "Type":"Bus",
                "Connected Node":[
            {"Node name":"DDR_PCIe_CM1_Top:APBmslave1",
            "Offset Address":"0x0100_0000",
            "Range":"16MB",
            "High Address":"0x01FF_FFFF",
            "Type":"Target"
            },
            {"Node name":"DDR_PCIe_CM1_Top:APBmslave2",
            "Offset Address":"0x0200_0000",
            "Range":"16MB",
            "High Address":"0x02FF_FFFF",
            "Type":"Target"
            },
            {"Node name":"DDR_PCIe_CM1_Top:APBmslave3",
            "Offset Address":"0x0300_0000",
            "Range":"16MB",
            "High Address":"0x03FF_FFFF",
            "Type":"Target"
            },
            {"Node name":"DDR_PCIe_CM1_Top:APBmslave4",
            "Offset Address":"0x0400_0000",
            "Range":"16MB",
            "High Address":"0x04FF_FFFF",
            "Type":"Target"
```

Figure 3-29. Sample Memory Map Report (.html format)



Memory Map Report: DDR_PCIe_CM1_Top

Design Details

Family:	PolarFire
Die:	MPF300T
Package:	FCG1152
Speed Grade:	-1
Voltage:	1.0
Date:	Mon Oct 4 05:04:52 2021
Project Name:	testcase
Project Location:	/eng_home/x62856/workspace/46_pcie_ddr4_v15/testcase
SmartDesign name:	DDR_PCIe_CM1_Top

Memory Map

The SmartDesign DDR_PCIe_CM1_Top contains the following Initiators under its hierarchy

- PCIe_CM1_0/ DMA_Controller_G5_0:AXI_M
- PCIe_CM1_0/ PF_PCIE_0:AXI_1_MASTER
- PCIe_CM1_0/ CM1_Subsystem_0/ CORECORTEXM1_0:AHB_MASTER
- APB3mmaster

top of page

PCIe_CM1_0/ DMA_Controller_G5_0:AXI_M

Target	Offset Address	Range	High Address	DRC
PCIe_CM1_0/ PF_PCIE_0:AXI_1_SLAVE	-			

Initiator list, top of page

Initiators, Bus, and Bridge cores available in Libero SoC Catalog

Various types of cores recognized as initiators, bus, and bridge cores are available in the Libero SoC Catalog window that can be used in a design. There are a few limitations on some of the core versions that can be used in a design for the memory map to be constructed correctly. The following consolidated table of all the available initiators, and bus and bridge cores highlights those limitations and exceptions on the cores and core versions with respect to memory map.

Table 3-1. Initiators, Bus, and Bridge Cores Available in Libero SoC Catalog

Classification	Core	Core Type	Minimum core version supported in Libero® SoC v2021.2 for Memory Map generation	Latest core version available in Libero SoC v2021.2

Initiators	MIV_RV32IMC	AXI, AHBLite and APB3 Initiators	NA. All available production version works.	2.1.100
	MIV_RV32	AXI, AHBLite and APB3 Initiators	NA. All available production version works.	3.0.100
	MIV_RV32IMA_L1_AXI	AXI Initiator	NA. All available production version works.	2.1.100
	MIV_RV32IMA_L1_AHB	AHBLite Initiator	NA. All available production version works.	2.3.100
	MIV_RV32IMAF_L1_AHB	AHBLite Initiator	NA. All available production version works.	2.1.100
	CORERISCV_AXI4	AXI4 Initiator	NA. All available production version works.	2.0.102
	COREAXI4DMACONTROLLER	AXI4 Initiator	NA. All available production versions works.	2.0.100
	COREABC	APB3 Initiator	NA. All available production versions works.	3.8.102

Family specific Initiator cores	PolarFire® SoC Standalone MSS (PolarFire SoC only)	AXI4 Initiator	NA. All available production version works.	v2.0
	System Builder and SmartFusion®2 MSS (SmartFusion2 and IGLOO®2)	AHBLite and APB3 Initiators	NA. All available production version works.	1.1.500
	CORECORTEXM1(PolarFire, PolarFire SoC and RTG4™)	AHBLite Initiator	NA. All available production version works.	3.0.100 and 2.0.100
	PF_PCIE (PolarFire only)	AXI Initiator	NA. All available production version works.	2.0.104
	SERDES_IF, SERDES_IF2, SERDES_IF3 (SmartFusion2 and IGLOO2)	AXI and AHBLite Initiators	NA. All available production version works.	1.2.210, 1.2.212, 1.2.212 respectively
	PCIE_SERDES_IF (RTG4 only)	AXI and AHBLite Initiators	NA. All available production version works.	2.0.100
	COREHPDMACTRL (SmartFusion2 and IGLOO2)	AHBLite Initiator	NA. All available production version works.	2.1.103
	CORESYSSERVICES (SmartFusion2 and IGLOO2)	AHBLite Initiator	NA. All available production version works.	3.2.102
	CoreConfigMaster (SmartFusion2 and IGLOO2)	AHBLite Initiator	NA. All available production version works.	2.1.102
Bus cores	COREAXI4INTERCONNECT	AXI bus	2.5.100	2.8.103
	CoreAHBLite	AHBLite bus	NA. All available production version works.	5.4.102
	CoreAPB3	APB3 bus	NA. All available production version works.	4.1.100
	CoreAXI	AXI bus	NA. All available production version works.	3.2.101
Family specific bus type cores	PF_DRI (PolarFire and PolarFire SoC)	APB bus	This core is not supported for Memory Map generation. Correct addresses and/or hierarchy is not shown for this core in the Memory Map of Libero SoC v2021.2.	1.1.100
	CoreConfigP (SmartFusion2 and IGLOO2)	APB bus	NA. All available production version works.	7.1.100

Bridge cores	COREAXITOAHBL	AXI to AHBLite bridge	Must use v3.5.100 for proper Memory Map generation in Libero SoC v2021.2.	3.5.100
	COREAHBL2AHBL_BRIDGE	AHBLite to AHBLite bridge	This core is not supported for Memory Map generation. Correct addresses and/or hierarchy is not shown for this core in the Memory Map of Libero SoC v2021.2. Supported in a future release.	2.1.108
	COREAHBLTOAXI	AHBLite to AXI bridge	NA. All available production version works.	2.1.101
	COREAHBTOAPB3	AHBLite to APB bridge	NA. All available production version works.	3.1.100
	COREAXITOAXICONNECT	AXI to AXI bridge	This core is not supported for Memory Map generation. Correct addresses and/or hierarchy is not shown for this core in the Memory Map of Libero SoC v2021.2. Supported in a future release.	2.0.101

4. Designing with SmartDesign

SmartDesign is a GUI-driven block-based design entry tool for instantiating, configuring, and connecting various types of design blocks.

The SmartDesign canvas is similar to a canvas, where the components of different types are assembled (instantiated), and connections are made via nets to create a design-rule-checked synthesis-ready HDL file for the complete FPGA design process.
To design with SmartDesign:

1. Create a top-level SmartDesign component (analogous to the canvas).
2. Add top-level ports.
3. Configure/Instantiate components on the top-level SmartDesign.
4. Make the connections (analogous to making wire connections to the different components).
5. Invoke a DRC on the design.
6. Generate the top-level component.

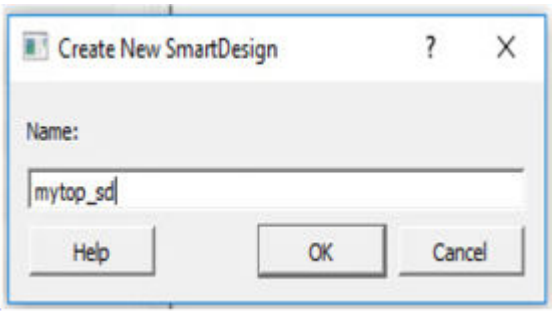
4.1 Create a Top-Level SmartDesign Component

A SmartDesign Component must be first created. This SmartDesign component may be the top level of the design or it may be used as a lower level SmartDesign component (after successful generation) in another design.

To create a SmartDesign Component:

1. From the **File** menu, choose **New > SmartDesign**, or double click **Create SmartDesign** in the Design Flow window. The Create New SmartDesign dialog box opens.

   Figure 4-1. Create New SmartDesign Dialog Box



2. Enter a name and click **OK**. The component appears in the **Design Hierarchy** tab of the Design Explorer.

Note: The component name must be unique in your project.

The main window displays the SmartDesign canvas (the canvas) with the component name you have entered displayed in a tab across the window.

4.2 Creating Hierarchical Smart Design

This feature allows you select any number of instances, nets, and ports and create a new SmartDesign out of it because all the nets and connections from the instance are retained.

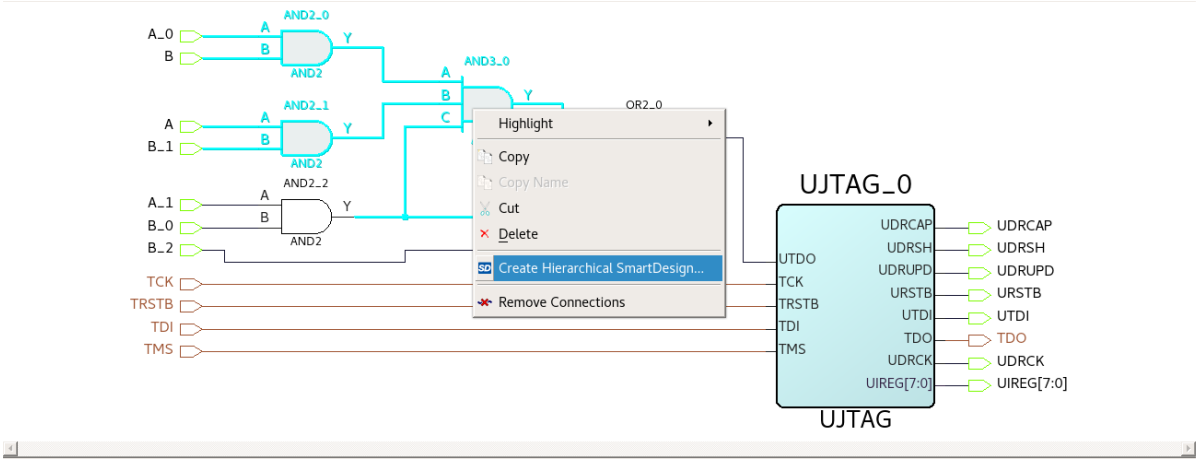
To create a new Hierarchical SmartDesign, perform the following steps:

1. Select any portion of the SmartDesign.
   Note: The selected portion must contain at least one instance.
2. Right click any object, and click **Create Hierarchical SmartDesign**.
3. In the dialog box that appears, enter a suitable Hierarchy name and Click **OK**.
4. A new SmartDesign is created with the specified name and all the selected items will be cut and pasted to that SmartDesign.

5. The new SmartDesign is instantiated, instead of the cut portion of the original SmartDesign.
6. All the connections are restored automatically.

The above Hierarchical SmartDesign creation flow is instance driven. So, the Hierarchical SmartDesign cannot be created out of ports and/or nets. It is not mandatory to select ports and nets, because the flow retains all the nets and the connections from the instances.

Figure 4-2. SmartDesign View with Create Hierarchical SmartDesign (Option for Selected Portion)



The following table lists the error messages that are displayed in the Log window for the mentioned scenarios:

Table 4-1. Error Message

Message	Type	Scenario
Error: SmartDesign with the specified name already exists. Please specify a different name.	Error	If another SmartDesign with the same name already exists.
Error: Cannot create hierarchical SmartDesign '[specified_name]' because it violates HDL naming rules. Please specify a different name.	Error	If specified name violates HDL naming rules.

4.2.1 Best Practices

Hierarchical SmartDesigns can be created by pressing **CTRL+H** shortcut key. Observe the following guidelines when creating a Hierarchical SmartDesign:

- Default name of the "Hierarchical SmartDesign" is: hier_[index].
- Top-level ports are created in the Hierarchical SmartDesign for all the unconnected instance pins.
- Port names for the Hierarchical SmartDesign is created using this formula: [instance_name] + "_pin_" + [pin_name].
- PAD ports do not follow the same naming rules and are promoted to top level automatically.
- If port name already exists, index suffixing is added to the name.
- Sliced ports are created like the regular bus ports.
- A Hierarchical SmartDesign can be created out of a single instance.
- Creating Hierarchical SmartDesign out of the ports is not allowed. At least one instance needs to be selected.

The following figures show an example of a Hierarchical SmartDesign consisting of 3 AND gates.

Figure 4-3. Hierarchical SmartDesign (Port Names Folded Inside the Block)

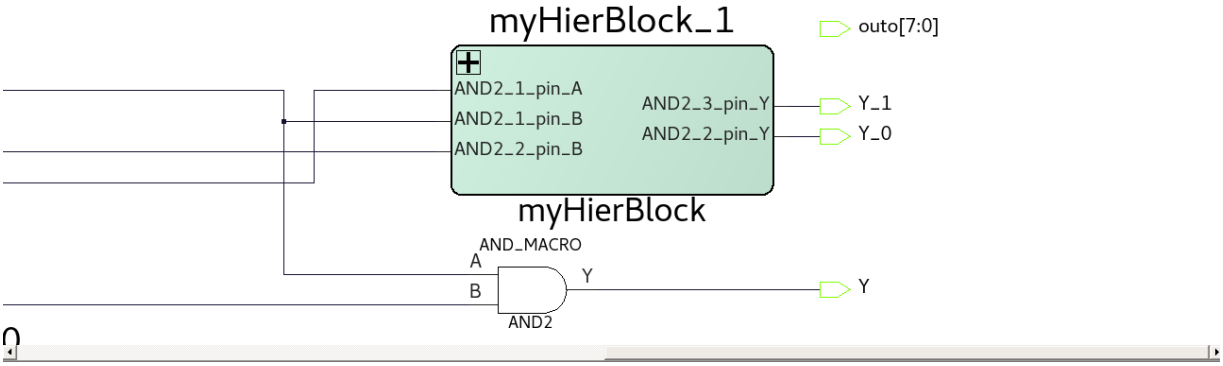
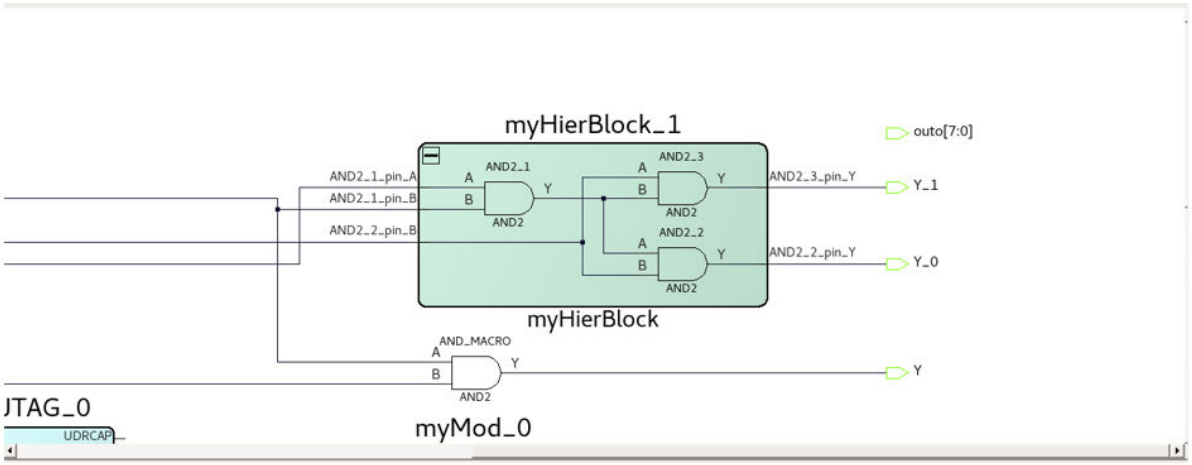


Figure 4-4. Hierarchical SmartDesign (Port Names Expanded Inplace Inside the Block Showing the AND Gates)



4.3 Flattening Hierarchical Smart Design

The **Flattening Hierarchical SmartDesign** action replaces the hierarchical instance with the corresponding instances from the hierarchical SmartDesign. The flattening action copies all the instances from the hierarchical SmartDesign component into the current SmartDesign and restores all inner and outer connections, attributes, slices, and exposed pins.

The following modifications are applied to the flattened design.

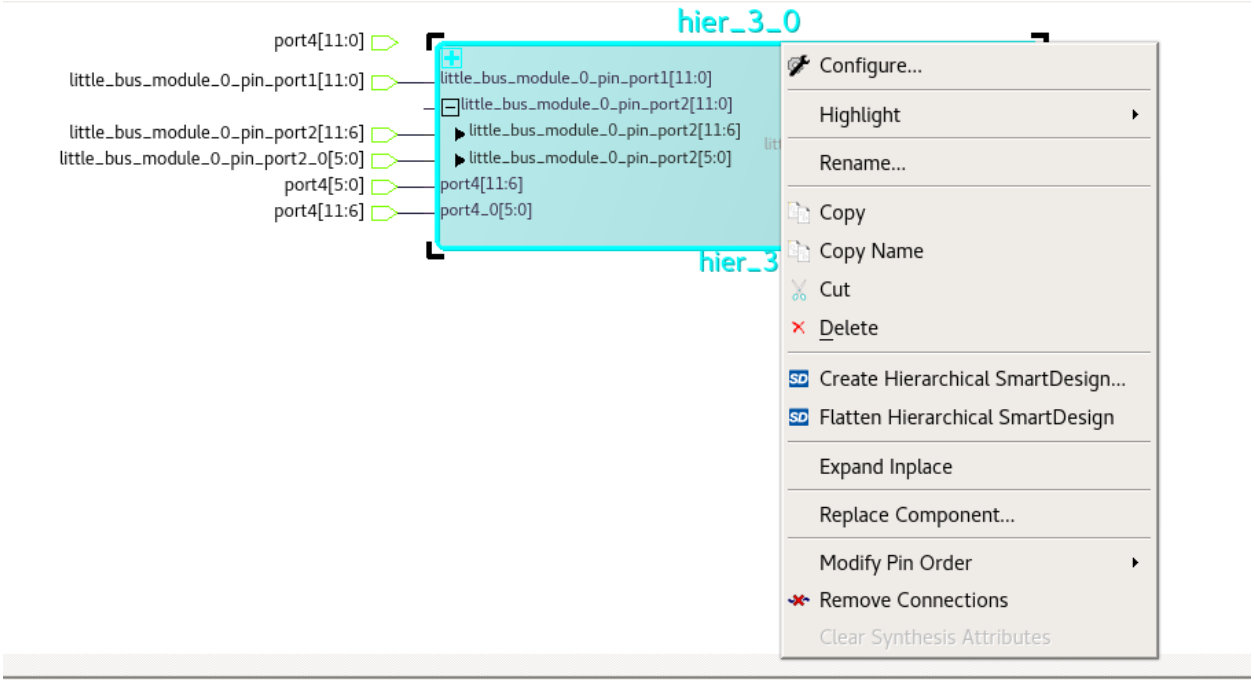
- When there is an inverted pin in the hierarchical instance and a corresponding port or pin (or both) from the hierarchical SmartDesign is also inverted, the resulting pin will be inverted, if inversion count is odd. Otherwise, it will not be inverted.
- When there is an inverted pin in the hierarchical SmartDesign and corresponding pin from the hierarchical instance have another attribute (tied High/Low), the inversion count is odd, then the tied attribute will be flipped.
- Internal nets and inner instances are renamed to <Hierarchical instance name> + "_" <Internal net name/inner instance name>.
- After flattening hierarchical SmartDesign, synthesis attributes of the outer and inner nets are merged. If both have the same attribute, the value of the outer net is used.

4.3.1 Best Practices

Right click on any Hierarchical Smart Design instance and select **Flatten Hierarchical SmartDesign** by right clicking or pressing **CTRL+J** shortcut key. Observe the following guidelines while creating a Flattening Hierarchical SmartDesign:

- Selected instance will be removed.
- All the instances are copied from the Hierarchical Smart Design to the original Smart Design.
- All the connections, attributes, slices, and exposed pins are restored automatically.

Figure 4-5. SmartDesign View with Flatten Hierarchical SmartDesign



4.4 Manage Synthesis Attributes

This feature enables to add or modify the synthesis attributes of the SmartDesign objects (nets, ports, and instances), directly, from the SmartDesign canvas.

Note: Synthesis attributes are not allowed to be configured for the BIF pins, the BIF nets, the Group pins, and the Slices. User defined attributes are not allowed.

The following table lists the synthesis attributes available in the Synopsys® FPGA synthesis tool that can be added from the SmartDesign.

Table 4-2. Synthesis Attribute

Attribute	Object
syn_insert_buffer	Port, instance
syn_keep	Net
syn_maxfan	Port, net, instance
syn_no_compile_point	Module or architecture
syn_noclockbuf	Port, net, module or architecture
syn_noprune	Instance, module or architecture
syn_preserve	Port, module or architecture

.....continued	
Attribute	**Object**
syn_hier	Module or architecture

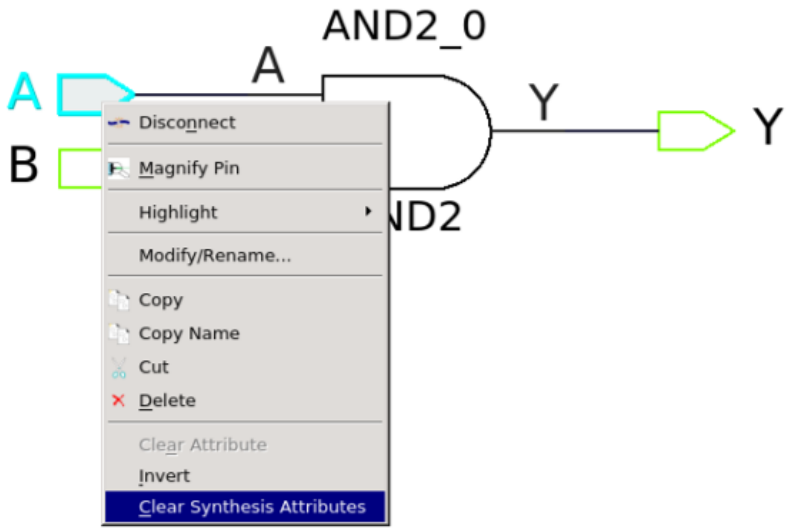
Note: For more details for each attribute, refer to Synplify Pro® ME.

4.4.1 Managing Synthesis Attributes from Canvas

Synthesis attributes can be managed from the canvas or GUI.

- Remove all synthesis attributes:
  To remove all the synthesis attributes from the object, right click the SD module and SD objects (port, net, and instance), and click **Clear Synthesis Attributes** as shown in the following figure.

  Figure 4-6. Clear Synthesis Attributes Menu Action



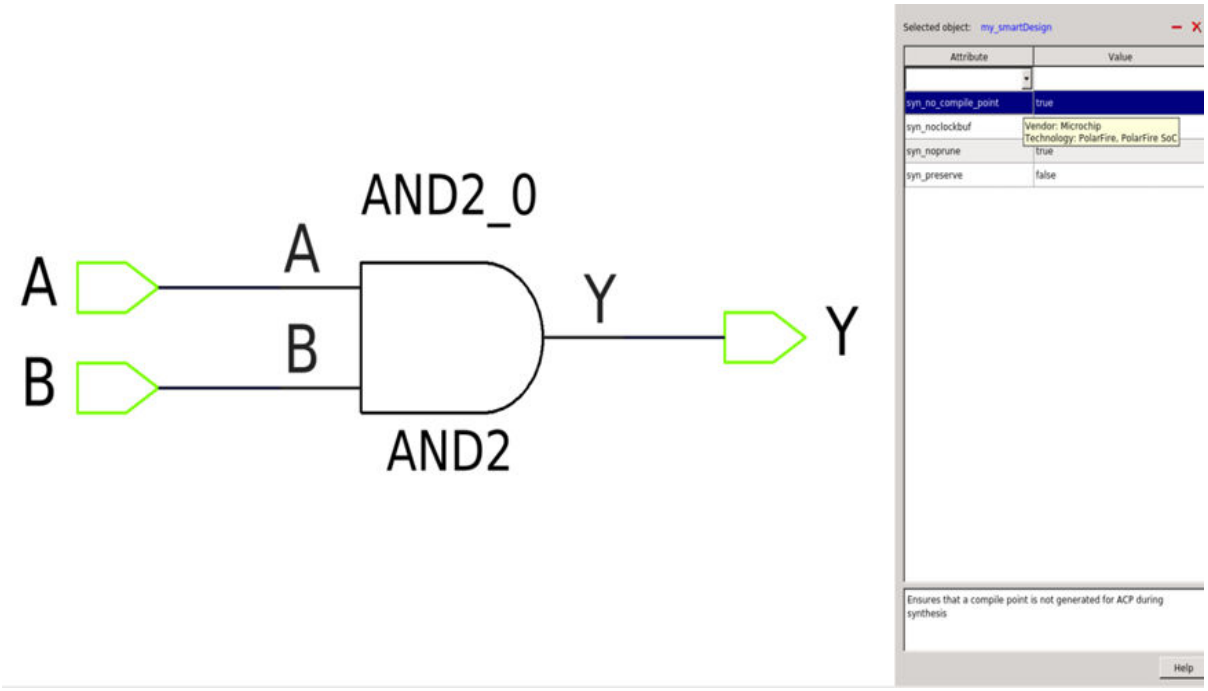
- Manage synthesis attributes:
  You can use **Manage Synthesis attributes** toolbar to open **Manage Synthesis Attributes** window as shown in the following figure. This window allows users to add or modify attributes of the SmartDesign objects.

  After selecting an object (port, net, and instances) in the SmartDesign canvas, the attributes of the selected object are displayed in the **Manage Synthesis Attributes** window. The **Manage Synthesis Attributes** window displays the SmartDesign module attributes if no object is selected. The name of the selected object is displayed on the window.

  All the attributes, reflected in the drop-down menu, are intended for the selected object. As the user selects the attribute from the drop-down list, the attribute is automatically added with a default value. To change the default value of the attribute, double click the value field. The selected attribute description is displayed at the bottom of the window.

  The tool-tip shows the vendor and technology of the attribute. To remove one or more attributes, select them and click **Manage Synthesis Attributes** the **Manage Synthesis Attributes** window Toolbar. To delete all the attributes of the selected object, click **Remove all Synthesis attributes** on the **Manage Synthesis Attributes** window Toolbar.

Figure 4-7. Manage Synthesis Attributes Window



4.5 Configure/Instantiate Components

4.5.1 Configure

This step is required for IP cores such as Clock Conditioning Circuitry (CCC), DDR3/4 Memory Controllers, SRAMs, AMBA Bus Interface cores, and Transceiver Interface cores. These cores are available in the Catalog of the Design Explorer. If the core name appears in italics, double click the core to download the core from the Microchip IP Core Repository to your hard disk (the vault) first. Double click the core in the catalog to open the Core's Configurator to configure the core. For details, refer to the respective configuration user guides.

4.5.2 Instantiate

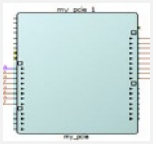
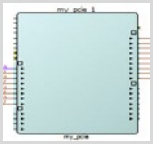
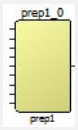
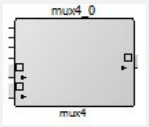
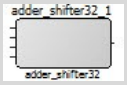
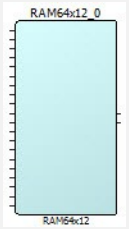
The SmartDesign canvas accepts the following component types for instantiation:

- Configured Microchip IP Cores
  - Drag and drop from the Catalog
  - IP cores must first be configured before they can be instantiated. If the IP core is not configured before instantiation, the drag and drop operation invokes the Core Configurator for the core to be configured.
- User-generated or third-party IP Cores
  - Drag and drop from the Catalog
- HDL design files
  - Drag and drop from the Design Hierarchy
- HDL Core design files (from the Design Hierarchy)
  - HDL core design files are parametrized HDL design files or HDL files with Buses attached
  - Drag and drop from the Design Hierarchy
- Basic macros
  - Drag and drop from Macro Library section in the Catalog
- Other SmartDesign components

  - These are `*.cxf` files generated from SmartDesign in the current Libero SoC project or imported from other Libero SoC projects.
  - Drag and drop from the Design Hierarchy
- Re-usable design blocks
  - These are `*.cxz` files published from Libero SoC and used as design blocks
  - Drag and drop from the Design Hierarchy

Each of these design components, after instantiation, is identified by different colors in the Design Canvas. When you hover the over a component, a tool-tip appears with information about that component.

Table 4-3. Component Types in the SmartDesign Canvas and Tool-Tip

Icon	Type of Design Components	Tool-tip Information
	Configured IP Core Component	Component: my_pcie Core: PF_PCIE 1.0.217
	IP Core directly instantiated from the Catalog	Core: PF_PCIE 1.0.217
	Block (`*.cxz`) file	Block: prep1
	SmartDesign component (`*.cxf`) file	SmartDesign: mytop
	HDL Core	HDL Core: mux4
	HDL	HDL:adder_shifter32
	Macro	Macro: RAM64x12

The tool-tip displays the following information about the component:

- Type of component
- Name of component

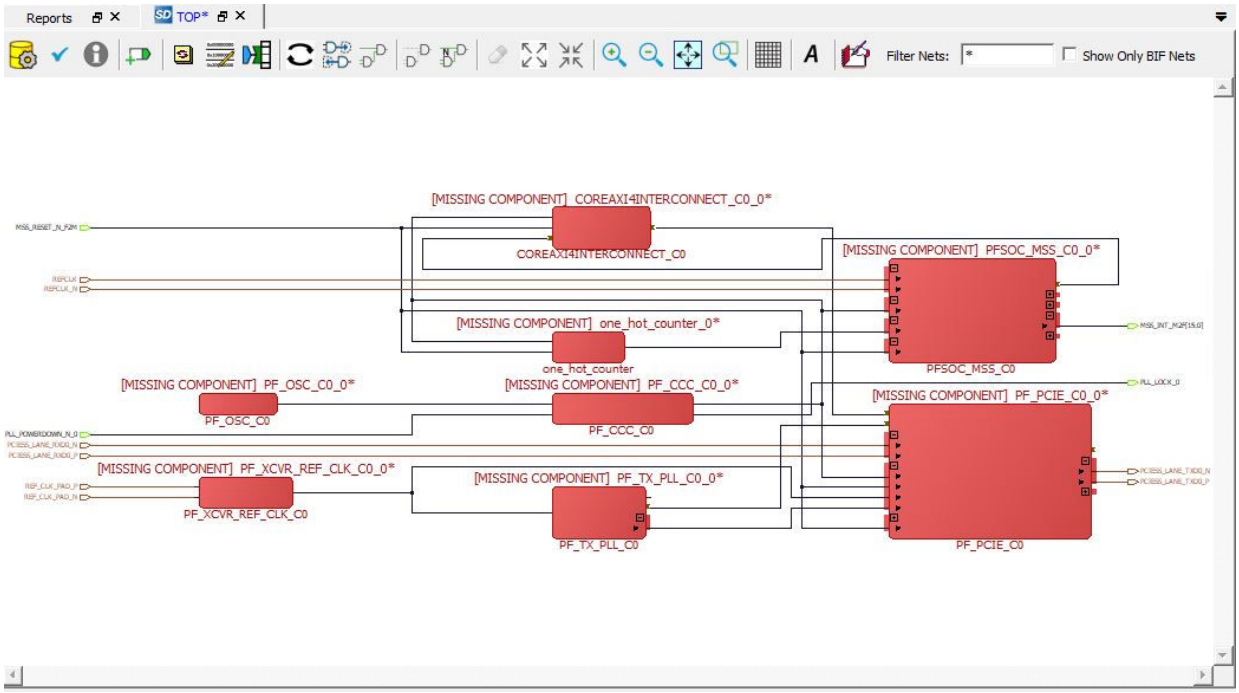
- Version of Core (for IP cores only)

The status icon is displayed at the top-right corner of the instance. Hovering over an instance, opens a tool-tip to display the information or message. For example, A new version is available.

4.5.3 Importance of .cxf Files in SmartDesign

SmartDesign components can be instantiated in another SmartDesign component by dragging and dropping them into the SmartDesign canvas. The low-level SmartDesign components in the hierarchy must be imported before instantiating in a new project. This is done by selecting **Import > Components** in the **File** menu. The HDL and corresponding cores associated with these components must also be imported and configured before instantiating in the new SmartDesign component. If you just import the `.cxf` file and do not import files corresponding to the low-level instances, you will see those instances highlighted in red and you will be informed of missing components. See the following example figure.

Figure 4-8. Errors While Importing SmartDesign Components with HDL Files and IP Cores



Using `.cxf` files is important in the following cases:

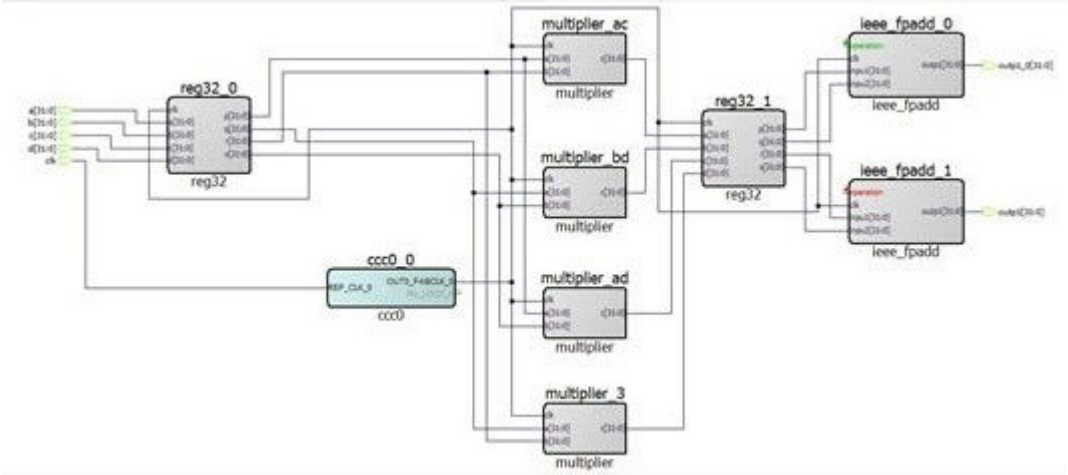
- When working on multiple designs with very few changes in the original design blocks.
- When dividing a large design into smaller designs with very few additional blocks.

Using `.cxf` files provides the following advantages:

- Significant time savings (decreased generation time)
- Minimizes errors in manual connections

See the following design example.

Figure 4-9. SmartDesign Example for Complex Multiplication



The example design above has clocking blocks, multiplier blocks, and adder blocks. You could separate this design into two separate designs— complex_real and complex_imaginary— in either of the following ways:

- Without using `.cxf` files— create two new projects, import and configure all necessary HDL files and IP cores, and make the connections manually.
- Using `.cxf` files—From the **Project** menu, save the original project with a new name using the **Save As** option. Make the necessary changes in the new project by deleting the blocks and ports you no longer need and adding additional blocks (if necessary), restoring the connections between existing blocks from original design. This saves time while dividing large designs into smaller designs, without the need to make all the connections manually.

To save the original project with a new name, from the **Project** menu, select the **Save As** option. Click **OK** after entering the new project name.

To change the name of the SmartDesign component, right click the component in the Design Hierarchy and choose **Rename Component**.

To create a SmartDesign component for calculating the real part of a complex multiplication, remove the blocks that are not necessary for calculating real part along with the unused ports. This eliminates many manual connections and reduces generation time. Real designs may not be as simple as this, but this type of dividing saves time while preserving the connections between existing blocks.

See the following example figures.

Figure 4-10. SmartDesign Component for Real Part Calculation of Complex Multiplication

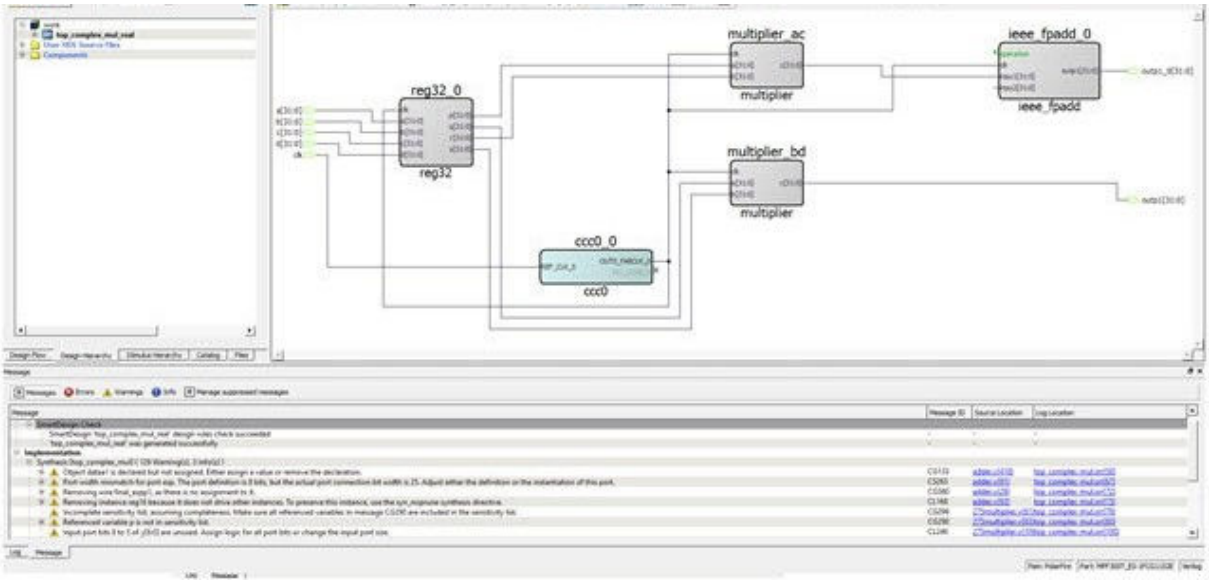
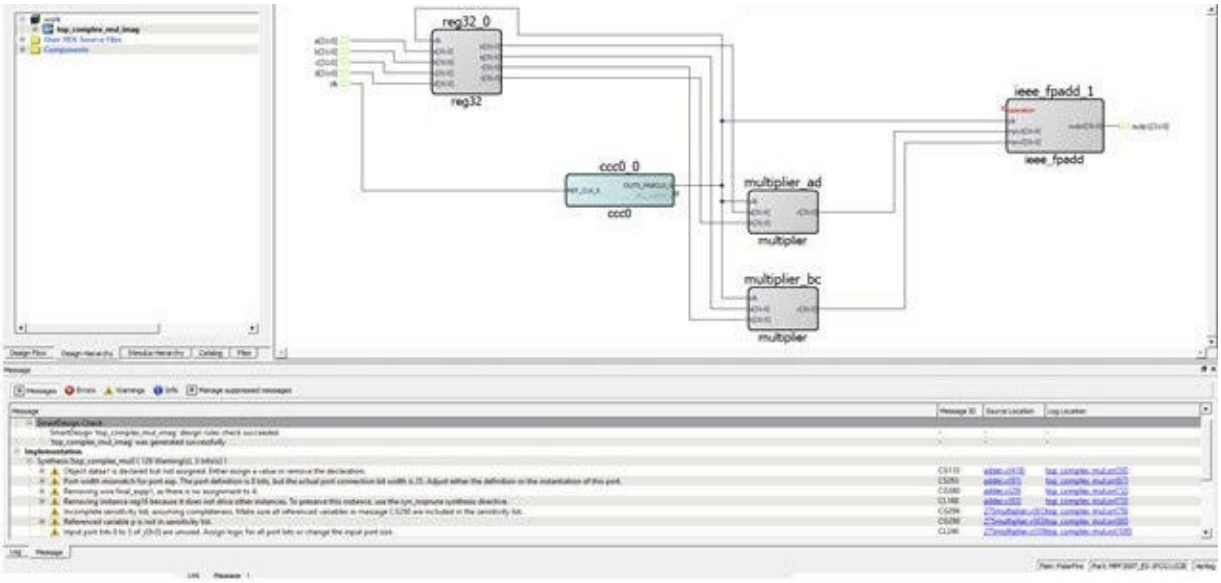


Figure 4-11. SmartDesign Component for Imaginary Part Calculation of Complex Multiplication



4.6 Make the Connections

There are several ways to make net connections in the SmartDesign Canvas.

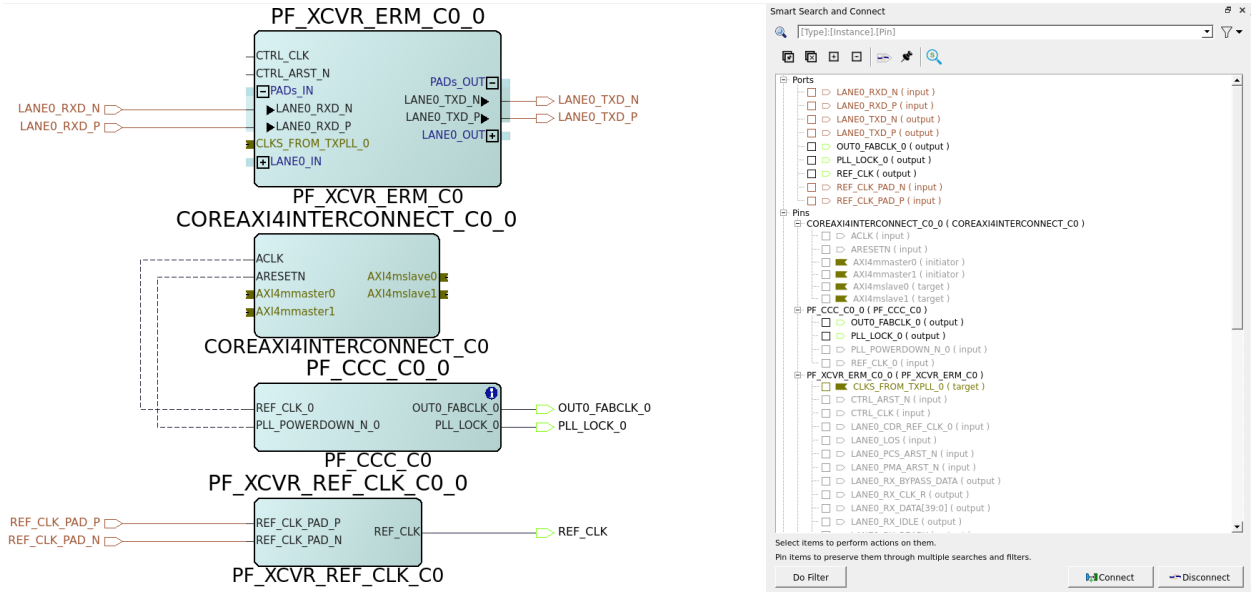
4.6.1 Smart Search and Connect

Smart Search and Connect tool is useful in SmartDesign, if there is a large design with multiple pins, ports, and nets to connect. Any object can be searched and connected easily without looking at the SmartDesign canvas. SmartDesign canvas reflects the connections as you make them. The log window displays the error messages if any error occurs.

The Smart Search and Connect tool is a resizable docking window. The window can be docked on the left, right, and lower sides of the canvas.

The Smart Search and Connect tool helps with complex search and in efficiently connecting multiple object (clocks, resets, and so on) at the same time. You can search items using keywords and filters, select, and then connect them using right click menu actions or by clicking the **Connect**, **Disconnect** buttons at the bottom. It is possible to pin the desired items and perform multiple searches. The pinned items will be available in search results, even if they do not match search patterns.

Figure 4-12. Canvas and Smart Search and Connect



The tool consist of the following items.

- Item tree
- Search bar
- Filter menu
- Action and toolbar
- Connectivity buttons
- Filtering toggle button

4.6.1.1 Item Tree

The item tree contains four top level items:

- **Ports:** This section contains all the top-level ports existing in the current SmartDesign canvas.
- **Pins:** This section contains all instance pins existing in the current SmartDesign canvas: grouped in sub-sections with instance names.
- **Instances:** This section contains all the instances existing in the current SmartDesign.
- **Nets:** This section contains all the nets existing in the current SmartDesign.

Right click menu contains appropriate actions for each type of objects.

4.6.1.2 Search Bar

In general search will follow this pattern: **[Type]:[Instance].[Name].**

User always can pin (check) items to keep them through multiple searches.

You can do a simple search when your search consists of only alphanumerical characters. All pins, ports, instances, and nets that satisfy the search pattern will appear. If the search pattern has the '.' separator symbol, SmartDesign treats the part before the separator as an instance name and the part after as a pin name. In this case, only pins and pinned items appear.

You can also search by the following keywords: "port:", "pin:", "instance:", "net:", and "*:". Alternatively, you can use their abbreviated versions. You must be specify keywords at the beginning of the search pattern.

4.6.1.3 Filter Menu

The Filter menu allows you to filter SmartDesign objects by their directions and their types. The selected filter is applied over the search results. The "Filter menu" icon shows whether a filter is selected.

 : No filter is selected

 : Filter is selected

4.6.1.4 Actions and Toolbar

Toolbar actions are the following:

Figure 4-13. Actions Toolbar

Table 4-4. Toolbar Actions

Action names	Description
Pin All	Sets pinned all visible items.
Unpin All	Unpins all pinned items.
Expand All	Expands all trees.
Collapse All	Collapses all trees.
Show Unconnected only	Filter action. Shows only unconnected pins/ports, if pressed. In this mode the instances and nets are not visible, even if they were pinned.
Show Pinned only	Filter action. Shows only pinned items, if pressed.
Zoom and Center	Checkable action. If pressed, after every selection the canvas zooms to the selected item.

4.6.1.5 Connection Buttons

Connectivity actions are going to be performed on selected objects by using "Connect" and "Disconnect".

4.6.1.6 Filtering SmartDesign Canvas

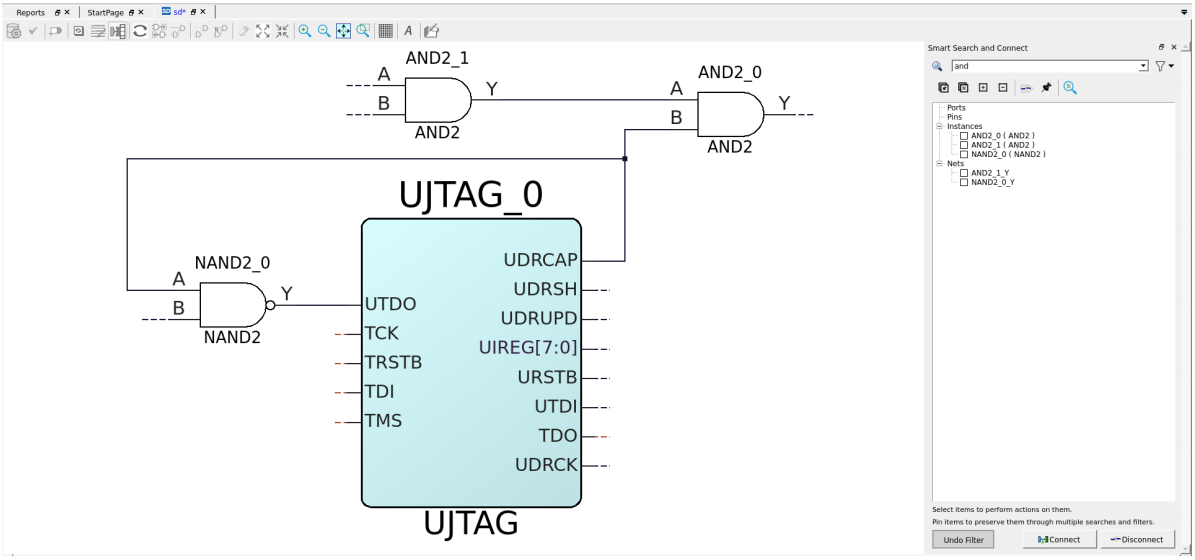
You can filter and display only a subset of the SmartDesign objects using the **Do Filter** toggle button of the **Smart Search and Connect** tool. This view is suitable to use with large designs to focus on a particular structure of the design, such as the clock or reset structure, or AMBA sub-systems for instance.

To create a filtered view of the SmartDesign canvas, first search the objects to be displayed in that view (perform multiple search and pin actions to define the list of objects) and then click the **Do Filter** toggle button on the **Smart Search and Connect** tool. After pressing it SmartDesign canvas will be recreated only with the object that are visible in the **Smart Search and Connect** search results tree.

Important: **Filtered SmartDesign Canvas** is read-only.

In the **Filtered Canvas**, all editorial actions and shortcuts are disabled, and only navigation actions are available. **Filtered Canvas** is created with a cone structure, to add new objects to the filtered canvas view by double clicking the dotted nets that expands the view by adding all objects connected to these nets. The net appears dotted if it is connected to an instance that is not included in the filtered view. You can double click the dotted net to load all the instances connected to that net.

Figure 4-14. Filtered SmartDesign Canvas

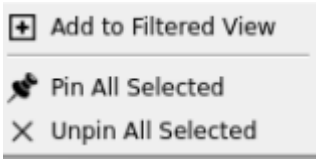


You can add new objects to the filtered view from the **Smart Search and Connect** search results tree by right clicking the object and selecting **Add to Filtered View**.

Adding a net to view using **Add to Filtered View** or double-clicking on it from the canvas adds the net itself and all the instances and ports to which the net is connected.

Adding pin/port to the filtered view will also add the net connected to it.

Figure 4-15. Add to Filtered View



You can exit the read-only filtered view to a normal SmartDesign canvas with the following options.

- Toggle the **Undo Filter** button
- Close the **Smart Search and Connect** window via **X** button
- Press **CTRL+Z** or **Undo** button

4.6.2 Control + Click Connection

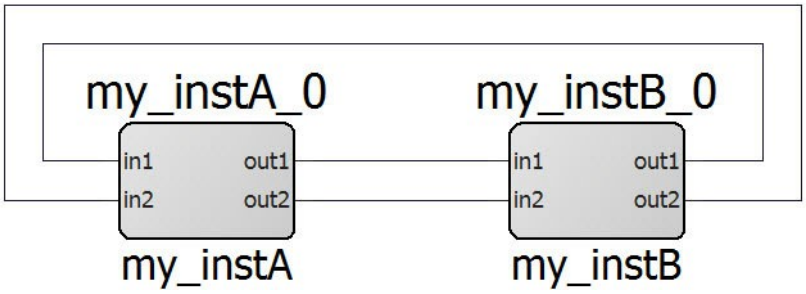
Use Control + Click to connect two pins on the canvas:

1. Left-click one pin.
2. Control and left-click another pin.
3. Right click the second pin and select **Connect**.

4.6.3 Modify Pin Order Before Connections

When two instances on the Canvas need to communicate with each other such that the output pins of one instance drive the input pins of another instance and vice versa, some of the nets between the two instances may have to go around the instance to make the connections.

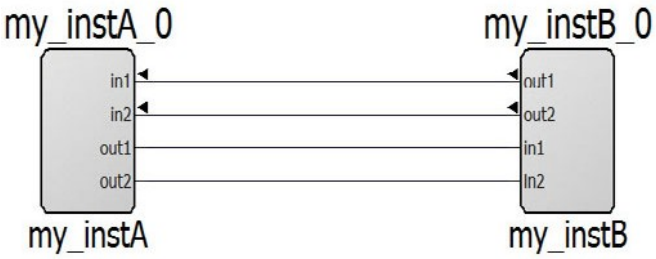
Figure 4-16. Connections between Two Instances with Regular Pin Order



However, if the pin order is modified such that the output pins of my_instance B are put on the left side and the input pins of Instance A are put on the right side of the instance, the net connection between the two instances are direct straight lines. The nets do not need to go around the instance.

See 3.2.9. Modify Pin Order for details on how to modify the pin order.

Figure 4-17. Connections between Two Instances with Modified Pin Order



After the pin order is modified, input pins are identified by inward-pointing arrowheads and output pins are identified by outward pointing arrowheads. The arrowhead helps you identify at a glance the direction of the pins (input/output) when they are not in the default locations. You can always hover the mouse over the pin to open the tool-tip message to see the direction.

Note: Inout pins, by default, are put on the right side of the instance. They do not have arrowheads when their location is modified. Hover the mouse over the pin to open the tool-tip message to see the direction of the input, output, and inout pins.

4.6.4 Splitting the Bus Before Connections

Before connections are made to a bus, the bus may need to be split for the following reasons:

- Different bits of the bus go to different parts of the design.
- Some bits of the bus need not to be connected and have attributes on them (output pins mark unused, tie to high/low or tie to constant).

The bus pin can be split into standard or custom slices:

- Standard slices are common, off-the-shelf slices available in the right click menu of a selected bus pin or port.
- Custom slices are various slice/width combinations that are possible for the given bus width but not available from the off-the-shelf listings in the right click drop-down menu. A special dialog box is available to customize the slices.

Refer to 3.3.11. Create Slices for details.

4.6.5 Search Design Objects to Connect

For a large design with many instances and pins, it may be difficult to find the pin/port/instance/net to make connections.

Three different ways are available for addressing this issue:

- Find window
- Net Filter in SmartDesign Canvas

- Smart Search and Connect

4.6.5.1 Find Window

The Find window is outside the SmartDesign canvas, but can be used to easily find design objects to make net connections.

1. Open the SmartDesign component in the canvas.
2. Click **Edit > Find** in the Libero SoC menu to open the Find window at the bottom of the Libero main window.
3. In the **Search** menu, select **Current Open SmartDesign**.
4. Enter the type of design objects (Instance/Net/Pin) from the **Type** menu.
5. Enter the string of characters in the **Find** box.
6. Click **Find All**.
7. If there are matches, click the item in the **Search Results**.

The SmartDesign canvas zooms in and highlights the design object. Zoom out far enough, with the design object still selected, to see the rest of the design and make the net connections.

4.6.5.2 Net Filter in SmartDesign Canvas

Use net filters in the SmartDesign Canvas to filter nets. Net filtering will filter out any nets that do not match the filter and make the SmartDesign Canvas less cluttered.

1. Open the SmartDesign component.
2. Enter a string in the **Filter Nets** field. By default, the filter field has the “* “character, which means all nets are shown (no filtering). Enter the net name or parts of the net name to filter the net you are interested in. To find all clock nets, you may want to put in *clk* in the field. Valid characters to enter in the field are:
   - “*” - a wild card that matches any number of characters
   - “?”- matches only one single character
   - [a-z, A-Z, 0-9] - matches any character inside the bracket
   - The comma “,” character or the space character is used to delimit multiple matches. A filter field with the entry “clk,reset” or “clk reset” matches any net names with the “clk” or “reset” string.

Note: For any term entered in the filter field that contains no “*” ,“?”, “[“, ”]”, the tool adds the wild-card match “*” before and after each term. “clk reset” and “*clk* *reset*” give the same matches. Net filtering is case-insensitive.

To narrow down the filter, click the **Show Only BIF Nets** check box. Only Bus Interface (BIF) nets that match the filter are shown. BIF nets that do not match the filter and non-BIF nets are hidden.

BIF pins are identified by the  icon on the instance. BIF nets are nets connected to BIF pins.

4.7 Add or Modify Top-Level Ports

You can add ports to the ports already in your SmartDesign and rename the ports.

4.7.1 Add Prefixes to Bus Interface and Group Names on Top-level Ports

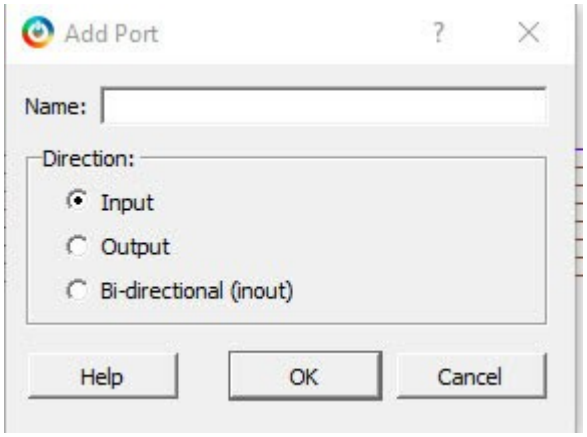
Bus Interfaces and Groups are comprised of other ports. On the top level, you can add prefixes to the group or bus interface port name to the sub-port names. To do so, right click the group or bus interface port and choose **Prefix <name> to Port Names**.

4.7.2 Adding and Removing Ports

To add ports:

1. From the **SmartDesign** menu, choose **Add Port**. The Add Port dialog box appears (as shown in the following figure).

Figure 4-18. Add New Port Dialog Box



2. Specify the name of the port you want to add. You can specify a bus port by indicating the bus width directly into the name using brackets [ ], such as mybus[3:0].
3. Select the direction of the port.
4. If the port name contains illegal characters or violates HDL naming rules, an error message will be displayed in the dialog box, and a new port will not be created.

To remove a port from the top level, right click the port and choose **Delete**.

4.7.3 Modify/Rename Port

To rename a top-level port, right click the top-level port and choose **Modify/Rename Port**. You can rename the port, change the bus width (if the port is a bus).

4.8 Invoke DRC on the Design

The DRC runs automatically when you generate your SmartDesign; the results appear in the **Reports** tab. You can also initiate a DRC by clicking on the **Design Rule Check** icon of the SmartDesign Canvas Icons.

For more information about running and understanding DRC results, see DRC Check.

4.9 Generate the Top-Level Component

The SmartDesign that has been created must now be generated. Generating a SmartDesign component may fail if there are any DRC errors. DRC errors must be corrected before you generate your SmartDesign top-level component.

If the ports of a sub-design have changed, the parent SmartDesign component will be annotated with the icon in the **Design Hierarchy** tab of the Design Explorer. This issue must also be corrected before you generate your SmartDesign top-level component.

Once there are no further DRC errors, the top-level component can be generated either recursively or non-recursively. Non-Recursive generation is enabled by default.

4.9.1 Recursive Generation

In recursive generation mode, the **Generate** button will try to generate all sub-design SmartDesigns, starting with depth. The parent SmartDesign will only be generated if all the sub-designs are generated successfully. To enable recursive generation, from the **Project** menu, choose **< Project > Preferences > Design Flow > Generate Recursively**.

4.9.2 Non-Recursive Generation

In the "non-recursive generation" mode, the **Generate** button will only attempt to generate the specified SmartDesign. This generation can be marked as successful even if a sub-design is ungenerated (either never attempted or

unsuccessfully attempted). An ungenerated component will be annotated with the ⓘ icon in the **Design Hierarchy** tab of the Design Explorer.

5. Design Navigation Features

The SmartDesign Canvas provides the following navigational features:

- Expand/Fold Instance
- Magnified window

5.1 Expand and Fold Instance

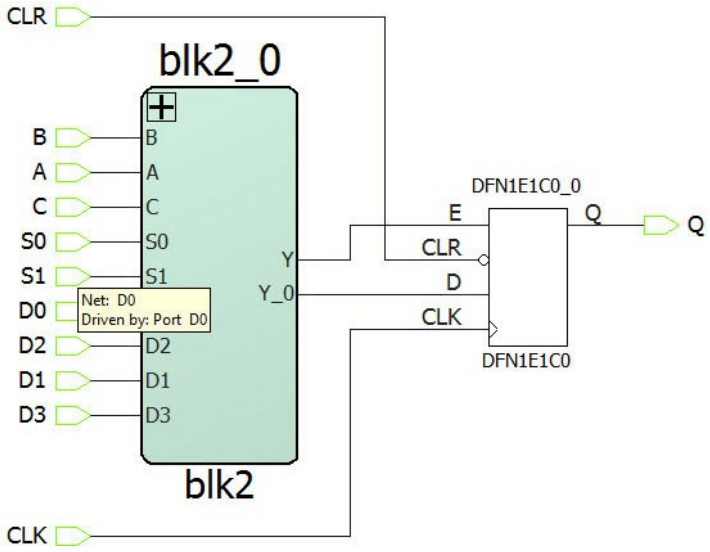
The Expand and Fold instance feature allows you to traverse up (Fold Instance) and down (Expand Instance) the design hierarchy of a SmartDesign component.

An instance of a SmartDesign component, which contains lower level hierarchies that can be expanded or folded in place. Expanded is traversing one level of hierarchy for viewing. Fold is the design that is collapsed to the next higher level. The expand or fold instance is a read-only view of the component.

The Expand and Fold actions are executed in place. The result of the Expand and Fold Instance appears in the same location, relative to the rest of the design in the same window. No new window is opened.

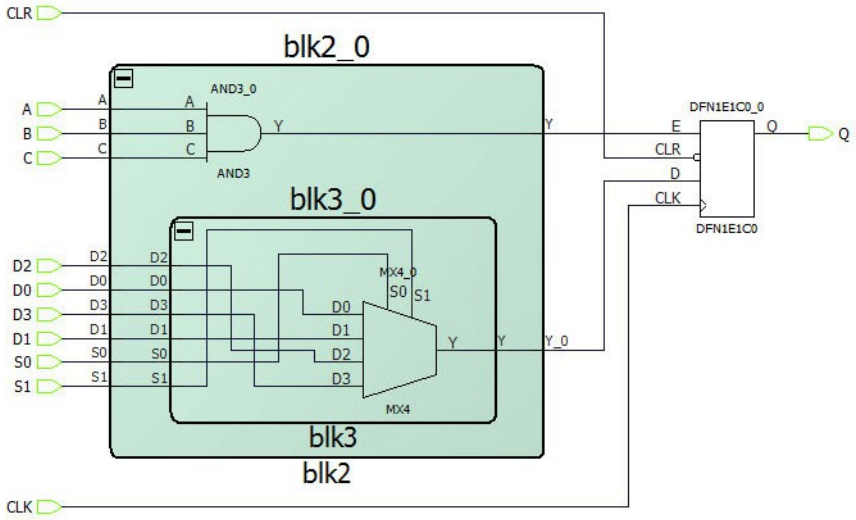
A folded design is indicated by a **+** sign at the top-left corner of the design. Clicking the **+** sign expands the folded design to the next lower levels of hierarchy. Alternatively, right click the instance and select **Expand Inplace**.

Figure 5-1. Top-Level Design — Folded



An expanded design is indicated by a **–** sign at the top-left corner of the design. Clicking the **–** sign collapses the design hierarchy to the next higher level of hierarchy. Alternatively, right click the instance and select **Fold Instance**.

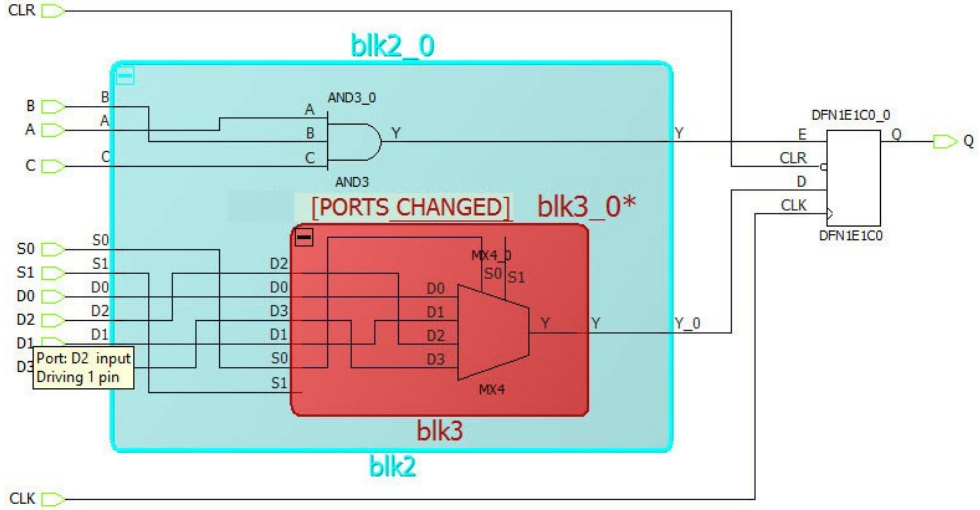
Figure 5-2. Top-Level Design — Expanded



When a lower level of the design hierarchy is modified, the parent block that instantiates the modified lower level is indicated by the asterisk (*) next to the name in the **SmartDesign Component Name** tab to indicate a change. If the modified block is two levels of hierarchy down, the design blocks of the next two higher levels have the asterisk (*) next to their names (in the **SmartDesign** tab) to indicate that the design component has changed. The modified block is highlighted in red and have status icon on the top-right side of the block.

Note: The red highlight and the warning icon appear only after the higher level block(s) is folded and expanded again to expose the changed lower level block.

Figure 5-3. Red Highlight and Changed — Module Identification



Note: Instead of ports changed, the error becomes **missing module** if any one of the following conditions occurs.

- A lower level SmartDesign component instantiated in a higher level module or block is deleted from the Project (Design Flow window > right click **SmartDesign Component** and select **Delete from Project**).
- An IP core instantiated in a higher level module or blocks is not found or has been removed from the vault.

If the changed or missing module/block is at the lowest level of hierarchy, the **Update Instance** and **Generate Components** steps must be repeated at every level of hierarchy above the changed module or block until the top-level hierarchy is reached, updated, and regenerated.

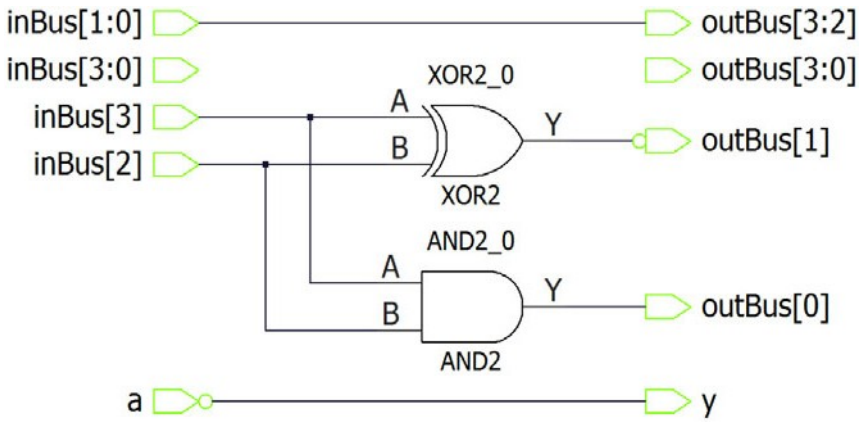
5.1.1 Expand Inplace and Low-Level Blocks

When a design component is expanded any place, SmartDesign reads in the current state of the low-level blocks after it expands. If changes are made to the low-level blocks (for example, name changes, connectivity changes, addition or deletion of instances, pin order changes), the Expand Inplace view must be folded and expanded again before the Expanded Inplace view shows the update.

The top-level ports in the low-level blocks are shown differently in the Expanded Inplace view if these top- level ports are:

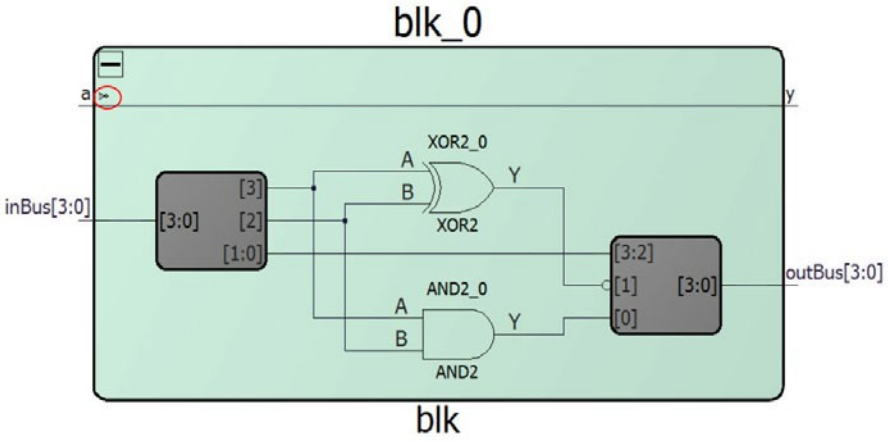
- Inverted
- Sliced

Figure 5-4. Low-Level Block View with Inverted Port and Sliced Port



At the Expanded Inplace view, for inverted ports, an inverter symbol is displayed next to the port (circled in the following figure). For the slice ports in this view, a slicer instance is inserted for each sliced bus.

Figure 5-5. Expanded Inplace View with Inverter Symbol and Slicer Ports



5.1.2 Component Regeneration

When the port list of the lower level block has changed, you need to:

1. Go to next higher level of the design hierarchy.
2. Right click the lower level component and select **Update Instance**.
3. Generate the higher level component.

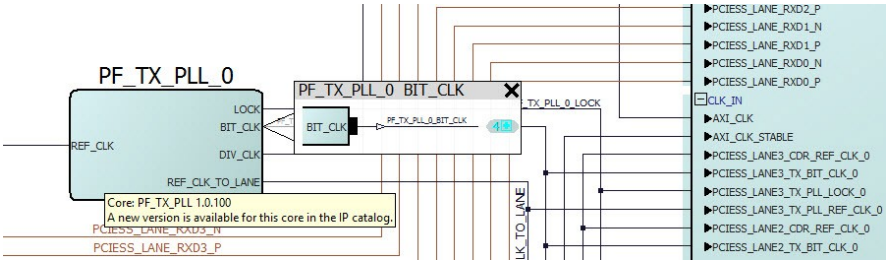
The red highlight and the **status icon** disappear when the component update is successful.

5.2 Magnify Pin

This option is available to pins and ports only. Double click a pin or a port or right click and select **Magnify Pin** to access this option. The Magnify Pin window shows the specified pin/port's connections.

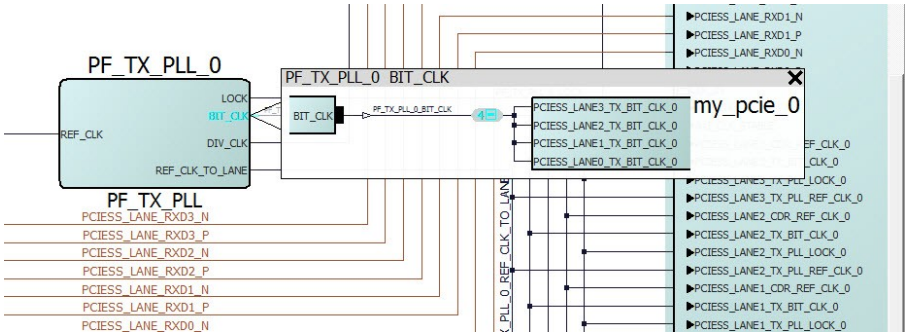
If the pin has a fanout of more than 1, the number 4 beside the + sign in the following figure shows the total fanout.

Figure 5-6. Magnify Pin Window



Click the + sign to see all the fanouts of the pin (see the following figure).

Figure 5-7. Magnify Pin Window with Fanout Expanded



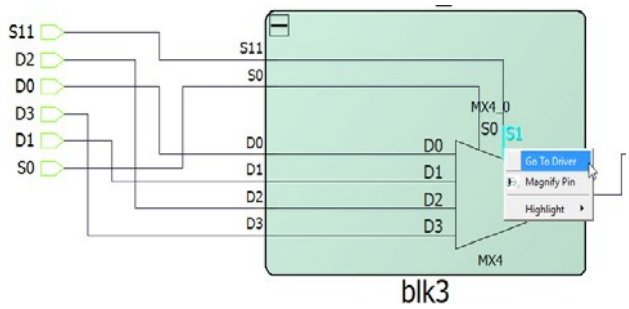
Double clicking the net/pin/port/instance inside the Magnify window zooms into and selects the item. This makes it easy to navigate inside large designs.

To close the Magnify window, click the **Delete** (**X**) button on the Magnify window or press ESC on the keyboard.

5.3 Go To Driver

Right click a net/pin/port and select **Go To Driver**. SmartDesign zooms in and selects the driver of the net/pin/port at the current level of hierarchy.

Figure 5-8. Go To Driver



6. Appendix A - Glossary

Table 6-1. SmartDesign Glossary

Term	Description
BIF	Abbreviation for bus interface. Logical grouping of ports or pins that represent a single functional purpose. May contain both input and output, scalars, or buses. A bus interface is a specific mapping of a bus definition onto a component instance.
Bus	An array of scalar ports or pins, where all scalars have a common base name and have unique indexes in the bus.
Bus Definition	Defines the signals that comprise a bus interface. Includes which signals are present on an initiator, target, or system interface, signal direction, width, default value, etc. A bus definition is not specific to a logic or design component but is a type or protocol.
Bus Interface Net	A connection between two or more compatible bus interfaces Canvas A visual representation of the canvas for placing components and stitching the components to create a working design.
Driver	A driver is the origin of a signal on a net. The input and target BIF ports of the top-level or the output and Initiator BIF ports from instances are drivers.
Instance	A block-like item with pins on either side of it. These are connected together to create designs. You may have multiple instances of a single component in your design. For each specific instance, you usually will have custom connections that differ from other instances of the same component.
Net	A wire that connects pins/ports in a design PAD The property of a port that must be connected to a design's top- level port. PAD ports will eventually be assigned to a package pin. In SmartDesign, these ports are automatically promoted to the top-level and cannot be modified.
Pins	Pins are the inputs/outputs/inouts of an instance that a net can be attached to for connection with other components in the design. By default, pins are placed on either the left (inputs) or the right side (outputs and inouts) of the instance. Pin order can be modified for a cleaner, less cluttered connection.
Port	A port is like a pin, but it is not attached to an instance. It acts as a way of letting a net connect to the outside world. A port has a direction (input, output, bidirectional) and may be referred to as a 'scalar port' to indicate that only a single unit-level signal is involved. In contrast, a bus interface on an instance may be considered as a non-scalar, composite port.
Macro	A type of very basic instance that typically has a special well- known shape associated with it. Inside of more complicated instances will be connected macros to do a more complicated function. Macros are specific to the technology family. Macros are listed in the Basic Macro group in the Catalog.
HDL File	A specially formatted text-file that describes the designs you create in a standard way.
Viewport	The rectangular view area of the canvas that is visible to you. You can move the viewport around on the canvas or zoom in/out to view your design. Showing the whole canvas would be too large in most cases.
Initiator BIF	Initiator Bus Interface. The bus interface that initiates a transaction (such as a read or write request) on a bus.
Target BIF	Target Bus Interface. The bus interface that responds to a transaction (such as a read or write request) on a bus.

.....continued

Term	Description
System Bus Interface	Interface that is neither initiator nor target; enables specialized connections to a bus.
Slice	A slice is created from a bus. It is a portion of the bus and it contains some but not all scalar members of the bus.
Top-Level Port	An external interface connection to the outside world. Scalar if a 1-bit port, bus if a multiple-bit port or a Bus Interface (BIF). These are connected to the pad/package pins of the FPGA device.
Pin Group	A grouping of pins (scalar or bus) you create for easy connection or identification.

7. Appendix B - DRC Check

When SmartDesign components are generated, the tool automatically enforces DRCs. The component is generated if the check passes.

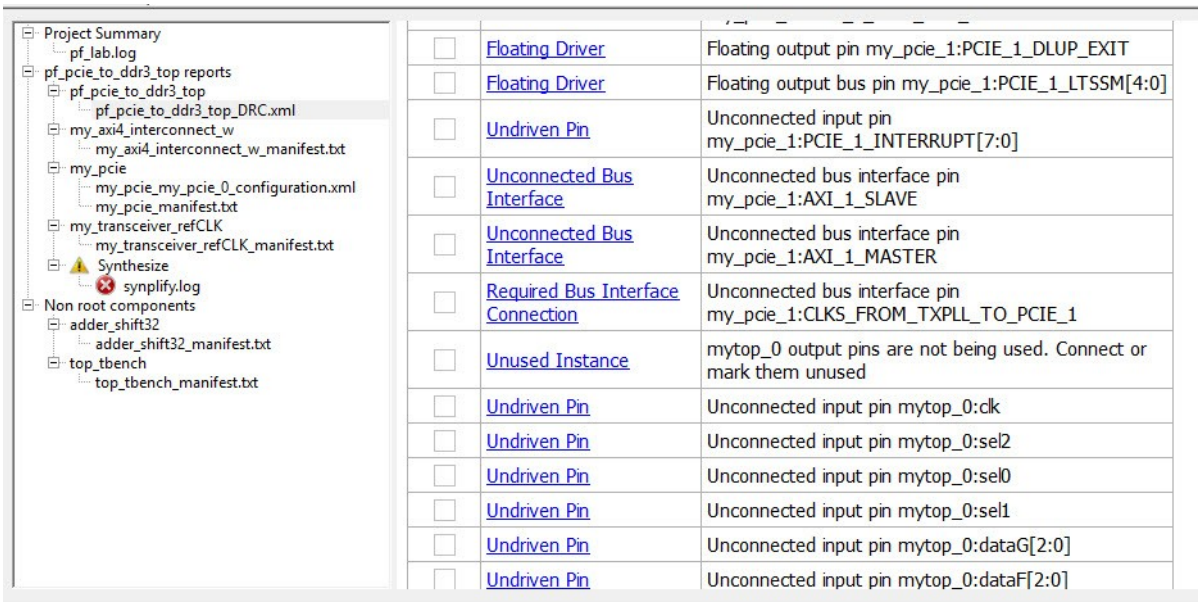
Alternatively, to invoke DRC checks without generating the component, click the **DRC check** icon in the toolbar.

To view the results of the DRC check, from the **Design** menu, choose **Reports**. The Report is named `<Design component>_DRC_xml` in the **Reports** tab. DRC errors are also reported in the Log/Message window.

Click the links on the DRC report. SmartDesign zooms in and highlights the design object that is the subject of the DRC violation.

You must correct all DRC errors before you can generate the SmartDesign component and continue with the design flow.

Figure 7-1. DRC Report



7.1 Message Types and Corrective Actions

The following are the more common DRC errors and the corrective actions you need to take:

Table 7-1. DRC Errors and Corrective Actions

DRC Error	Description
Unused Instance	You must remove this instance or connect at least one output pin to the rest of the design.
Out-of-date Instance	You must update the instance to reflect a change in the component referenced by this instance.
Undriven Pin	To correct the error, you must connect the pin to a driver or change the state, that is tie low (GND), tie high (VCC), tie to Constant or marked unused.
Floating Driver	You can mark the pin unused if it is not going to be used in the current design. Pins marked unused are ignored by the Design Rules Check.

.....continued

DRC Error	Description
Unconnected Bus Interface	You must connect this bus interface to a compatible port because it is a required connection.
Required Bus Interface Connection	You must connect this bus interface before you generate the design. These are typically silicon connection rules.
Exceeded Allowable Instances for Core	Some IP cores can only be instantiated a certain number of times for legal design. For example, there can only be one Arm® Cortex®-M1 or CoreMP7 in a design due to silicon limitations. You must remove the extra instances. This check is technology-dependent.
Incompatible Family Configuration	The instance is not configured to work with this project's Family setting. Either it is not supported by this family or you need to re-instantiate the core. This DRC check is family/ technology-dependent.
No RTL License, No Obfuscated License, No Evaluation License	You do not have the proper license to generate this core. Contact Microchip SoC to obtain the necessary license.
No Top level ports	There are no ports at the top-level. To auto-connect top-level ports, right click the Canvas and choose Auto-connect
Self-Instantiation	The component <component_name> corresponds to the current SmartDesign design. A component cannot instantiate itself. **Note:** This message is reported only in the Log Window.
Bus interface data width mismatch	There is a data width mismatch between MIV_RV32IMA_L1_AXI_C0_0:MMIO_MST_AXI4:MMIO_AXI_0_W_BITS_DATA[0-63] and COREAXI4INTERCONNECT_C0_0:AXI4mmaster1:MASTER1_WDATA[0-31], which may result in loss of data. To correct the error, make initiator (driver) BIF pin write port width less than or equal to target BIF pin write port width as per port name shown in the DRC message. Another way to correct the error is to make target BIF pin read port width less than or equal to initiator (driver) BIF pin read port width as per port name shown in the DRC message.
Bus interface ID width mismatch	There is an ID width mismatch between MIV_RV32IMA_L1_AXI_C0_0:MEM_MST_AXI4:MEM_AXI_0_AW_BITS_ID[0-3] and COREAXI4INTERCONNECT_C0_0:AXI4mmaster0:MASTER0_AWID[0-1], which may result in loss of data. To correct the error, make initiator (driver) BIF Pin AWID/WID/ARID port width less than or equal to target BIF pin AWID/WID/ARID port width as per port name shown in the DRC message. Another way to correct the error is to make target BIF pin RID/BID port width less than or equal to initiator (driver) BIF pin RID/BID port width as per port name shown in the DRC message.

8. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
F	08/2022	The following is a summary of the changes made in this revision. • Updated section Introduction. • Updated section 2.1. SmartDesign Actions. • Updated section 4.3. Flattening Hierarchical Smart Design. • Updated section 4.6.1. Smart Search and Connect. • Added section 4.6.1.6. Filtering SmartDesign Canvas. • Updated section 5.1. Expand and Fold Instance. • Removed section Appendix: FAQ.
E	04/2022	The following is a summary of the changes made in this revision. • Updated section 2.1. SmartDesign Actions. • Updated section 2.2. SmartDesign Hotkeys. • Updated section 3.3.3. Promote to Top-Level. • Updated section 3.3.7. Modify and Rename. • Updated section 3.5. View Memory Map. • Updated section 4.5.2. Instantiate. • Updated section 4.6.5.1. Find Window. • Updated section 5.1. Expand and Fold Instance.
D	12/2021	• Updated section 2.1. SmartDesign Actions. • Removed figures "Example of Zoom In" and "Example of Zoom Out." • Updated section 3.2.7. Replace Component. • Updated section 3.2.8. Update Component Version. • Updated screenshots Figure 3-22, Figure 3-23, Figure 3-24, Figure 3-28, and Figure 3-29 in the section 3.5. View Memory Map. • Added section 4.3. Flattening Hierarchical Smart Design. • Updated Table 7-1 in section 7.1. Message Types and Corrective Actions section.
C	08/2021	• Updated the following tables: – 2.1. SmartDesign Actions – 2.2. SmartDesign Hotkeys • Added note related to Port/Net/Instance naming rules in the 3. SmartDesign User Actions section. • Added 3.4. Copy, Cut, and Paste. • Added 4.2. Creating Hierarchical Smart Design. • Added 4.4. Manage Synthesis Attributes. • Added 4.6.1. Smart Search and Connect. • Updated "VHDL Construct Support in SmartDesign."

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Revision	Date	Description
B	04/2021	• Updated 3.5. View Memory Map by adding information related to Downgrade option in the Preferences window. • Updated 2.1. SmartDesign Actions section since Connection Mode icon is removed from the tool. • Updated 4.6. Make the Connections by removing Connection Mode details since it has been converted to inbuilt Connection Tool. • Updated "How do I make manual connections?" section with information related to the Connection Tool.
A	11/2020	Document converted to Microchip template. Initial Revision.

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