Chip Planner User Guide

Libero SoC v2025.2

Introduction (Ask a Question)

Chip Planner is a graphical interface tool that provides a Chip View and a Netlist View of your designs.

The Chip View allows you to create regions, edit regions, and make logic assignments to regions. It is a floorplanning tool used to improve the timing performance and routability of your design by providing maximum control over your design object placement.

The Netlist View provides a schematic view of the design that allows you to examine the routing of the nets and reveal any routing congestions.

You can also cross-probe from SmartTime into Chip Planner to browse your design and look into timing problems.

Use Chip Planner to:

- View macro assignments made during layout.
- Assign, unassign, or move macros.
- Lock macro assignments.
- View net connections.
- View architectural boundaries.
- View and edit silicon features, such as I/O banks.
- Create Regions and assign macros or nets to regions (floorplanning).
- View logic placement and net connections to investigate timing problems together with SmartTime's Cross-Probing feature.
- View the hierarchical netlist after Synthesis and the flattened netlist after Compile.
- Create logical cones for debugging and detailed analysis.

Run Synthesis and Compile Netlist on your design before invoking Chip Planner. You can invoke Chip Planner for floorplanning after running Place and Route to improve routability and remove congestion.

When floorplanning, analyze your design to see whether certain logic can be grouped within regions. Placement of regions are especially useful for hierarchical designs, with sufficient local connectivity within a block. If your timing analysis indicates several paths with negative slack, you can group the logic included in these paths into their own regions. This forces the placement of logic close together within the path and may improve timing performance of the design.

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1. About Chip Planner (Ask a Question)

1.1. Supported Families and Platforms (Ask a Question)

Chip Planner supports SmartFusion® 2, IGLOO® 2, RTG4™, PolarFire®, and PolarFire SoC devices and runs on Windows® and Linux® systems.

Important: Depending on the device selected, some UI elements such as icons, options, and dialog boxes may vary slightly in appearance and/or content. Basic Chip Planner functionality remains the same, regardless of the device chosen.

1.2. Invoking Chip Planner (Ask a Question)

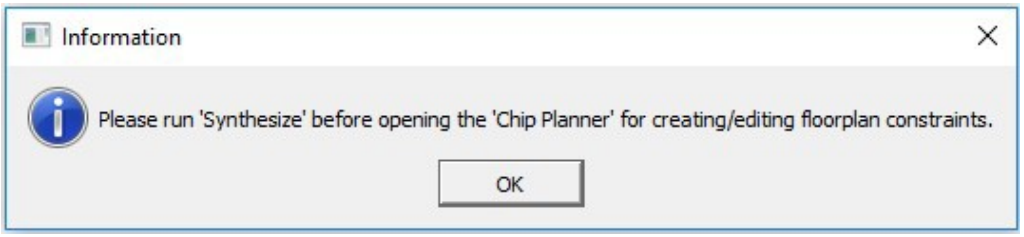
Invoke the Chip Planner as follows:

- **Design Flow window > Manage Constraints > Open Constraints Manager view > Constraint Manager > Floor Planner > Edit**

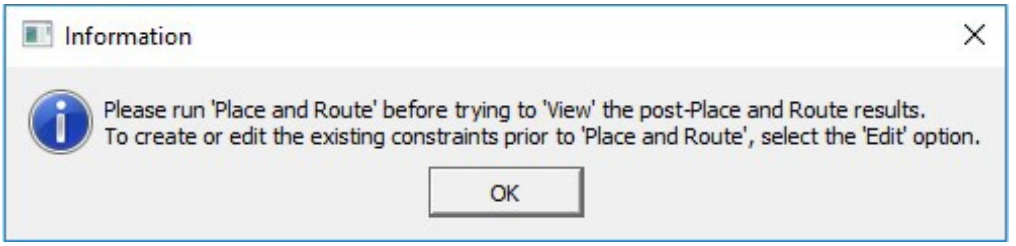
The **Edit** option in the Constraint Manager allows you to save or commit your changes to PDC files.

The **View** option shows the post-Place and Route design, including the final placement in read-only mode. The **View** option does not allow you to save or commit changes made in Chip Planner. However, you can export physical constraints with the **Edit** and **View** options, save them to disk, and use them later in your design as input files, depending on the design requirements.

Note: Complete the Synthesis step before invoking Chip Planner from the Constraint Manager using the **Edit** option. If you try to open Chip Planner before Synthesis, the following pop-up message appears.



Note: Complete the Synthesis step before invoking Chip Planner from the Constraint Manager using the **View** option. If you try to open Chip Planner using the **View** option before running Place and Route, the following pop-up message appears.



1.3. Chip Planner and PDC Commands/Files (Ask a Question)

When Chip Planner opens, only the PDC file(s) associated with Place and Route are loaded into Chip Planner for reading. PDC files in your project that are not associated with Place and Route are ignored.

When you make an I/O or floorplanning change in Chip Planner, commit and save. The change is saved to a `*.pdc` file that you set as a target in the Constraint Manager. If no PDC constraint file is set as target, the change is written to a new `user.pdc` file.

If the change is related to floorplanning, the `user.pdc` file appears in the **Floor Planner** tab. Interactive floorplanning actions in Chip Planner have corresponding PDC commands that can be made part of a constraint file for Place and Route.

If the change is related to I/Os, the `user.pdc` file appears in the **I/O Attributes** tab. The I/O PDC files are located in the `<proj>\constraints\io` folder.

The Floorplanning PDC files are located in the `<proj>\constraints\fp` folder.

For details about Libero® SoC PDC commands, see the PDC Commands User Guide for PolarFire FPGA or the PDC Commands User Guide for SmartFusion2, IGLOO2, and RTG4.

Chip Planner and I/O Editor can access and write to the same PDC file(s). If more than one of these tools are opened, making and saving changes from one tool is not allowed. This behavior prevents you from overwriting the constraints in the PDC file(s). A message alerts you to the modification conflict and identifies open tool(s) that must be closed.

To fix the modification conflict:

1. Close all tools except one.

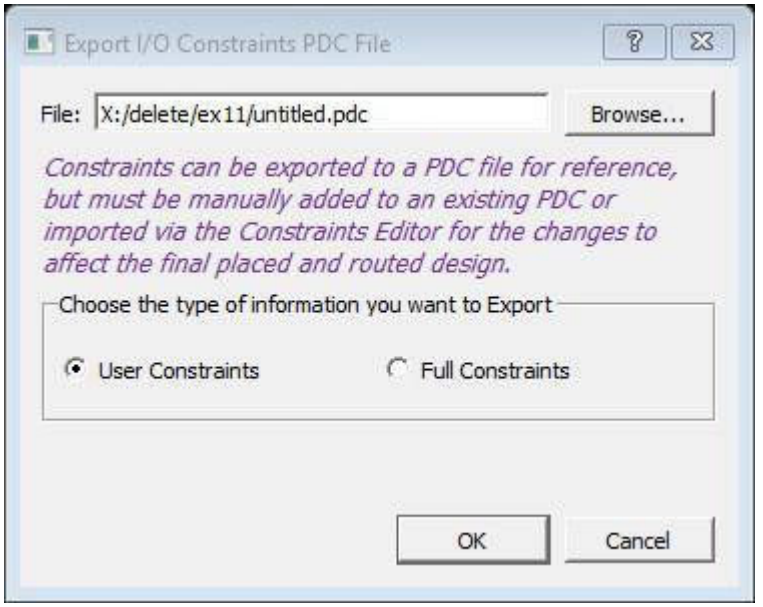
2. Make the changes in the tool, and then save them.

1.3.1. Export Physical Design Constraint (PDC) (Ask a Question)

Chip Planner allows you to export the physical design constraints (I/O Constraints and Floorplan Constraints) of the design to a PDC file saved to any location. Options allow you to:

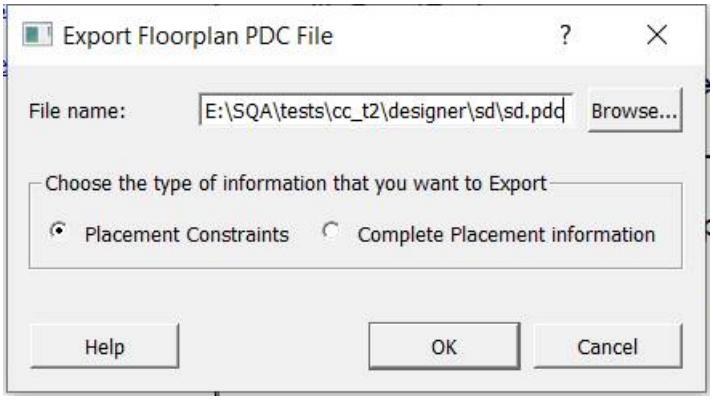
- Export the user constraints of the design.
- Export the full constraints of the design.
  The I/O PDC file can be exported using **File** > **Export** > **I/O Constraint PDC** as shown in the following figure.

Figure 1-1. Export I/O Constraints PDC File Dialog Box



The `<untitled>.pdc` file can be exported using: **File > Export > I/O Constraint (PDC) > Floorplan Constraints** as shown in the following figure.

Figure 1-2. Export Floorplan PDC File Dialog Box



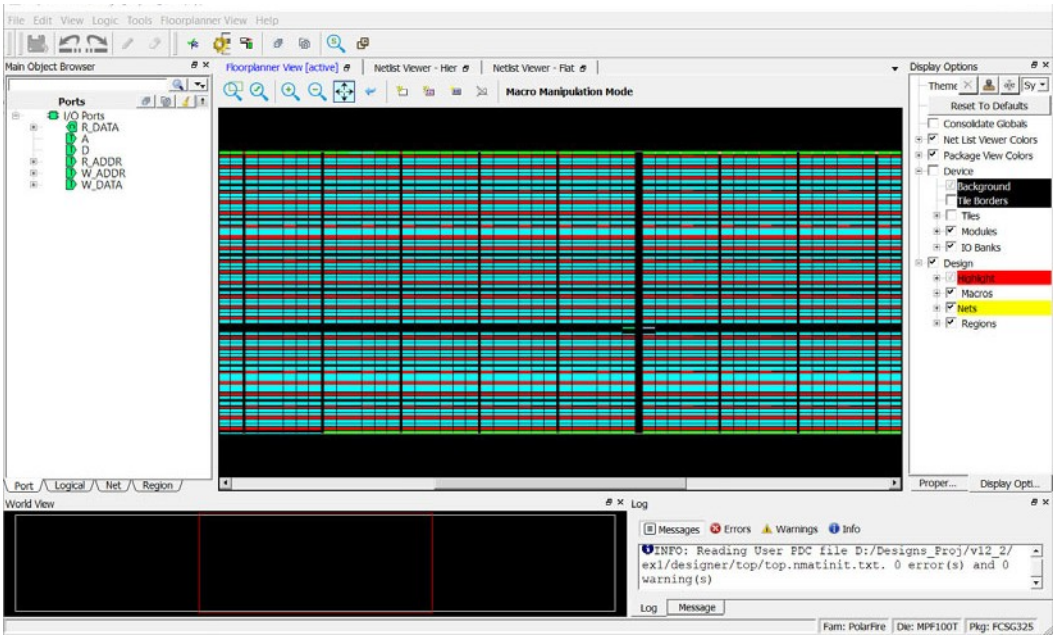
2. Chip Planner Views (Ask a Question)

When the Chip Planner launches, it opens the following windows:

- **Design View** window
- **Floorplanner View** window
- **Log** window
- **Display Options** window
- **Properties** window
- **World View** window

All windows can be docked or undocked (floating), turned on or off, resized, or moved to the right, left, top, or bottom of the Chip Planner application. Docked windows can be stacked horizontally or vertically.

Figure 2-1. Chip Planner



The **Design View** window provides the following view tabs for the design:

- Port
- Logical
- Net
- Region
- Block (only when the design instantiates a design block)

The following table lists the icons in the toolbar. Hover the mouse on the icon shown in the **Floorplanner View** to see the tooltip.

Table 2-1. Chip Planner Toolbar Icons

Icon	Name	Function
	Commit	Commit and Save behaves as follows: • Runs Chip Planner DRC before saving the changes. • Writes/updates PDC files.
	Undo	Reverses your last action.
	Redo	Reverses the action of your last Undo command.
	Highlight	Highlights a net, macro, or port.
	Unhighlight All	Unhighlights all highlighted selections (macro, net, or port).

Clone and Clear Options

The Clone and Clear options appear when you right click on the main object browser/design view window. The following table describes these options.

Table 2-2. Chip Planner Clone and Clear Options

Icon	Name	Function
	Clone new filter	Clones a Find window for a specific view (Logical/ Port/Net/Region/Block) depending on the view you are in when you click this icon or CTRL + F. Multiple Find windows may be cloned, each with a different set of filtering criteria, to provide multiple filtered views of design elements.
	Delete all filter browsers	Deletes all cloned Find windows.
	Delete all port filter browsers	Deletes all cloned port filter windows.
	Delete all net filter browsers	Deletes all cloned net filter windows.
	Delete all region filter browsers	Deletes all cloned region filter windows.
	Delete all block filter browsers	Deletes all cloned block filter windows.
	Rename	Renames the cloned window to a name other than the default name.

In addition, all five views share the following special icons:

- Port
- Logical
- Net Region
- Block

A tooltip is available for each icon. The following table lists these special icons.

Table 2-3. Special Icons in the Design View Window

Icon	Name	Function
	Reapply the Filter	Reapplies the filter and sort.
	Filter	Applies the filter to design object display.
	Collapse	Collapses the hierarchical display in the view.
	Expand	Expands the selected design object.
	Clear	Clears the Filter and refreshes the tree reflecting no filters applied.
	Change Sort Order and allow Additional Filtering	Changes sort order between ascending and descending, or applies additional filtering. Sort and Filter criteria vary with the view.
	Dock	Docks the cloned Find window. This option is available only in the cloned Find window.
	Maximize	Maximizes the cloned Find window. This option is available only in the cloned Find window.
	Restore	Restores back to the cloned Find window. This option is available only in the maximized clone Find window.

All Chip Planner windows can be docked or undocked.

Table 2-4. Window Management Icons

Icon	Name	Function
	Dock/Undock	Docks or undocks (floats) the window.
	Close	Closes the window.

Chip Planner provides the following special keys and hot keys.

Table 2-5. Special Keys and Hot Keys

Special Keys/Hot Keys	Function
CTRL + F	Find/Search function. Creates a cloned Find window.
CTRL + Z	Undoes the last action/command.
CTRL + S	Saves all changes.
CTRL + Y	Redoes last action/command.
Home	Scrolls to the first selected item in the view.
End	Scrolls to the last selected item in the view.
Tab	Scrolls to the next selected item in the view.

Table 2-5. Special Keys and Hot Keys (continued)

Special Keys/Hot Keys	Function
Shift + Tab	Scrolls to the previous selected item.
CTRL + Q	Exits Chip Planner.
CTRL + ++	Zooms in.
CTRL + --	Zooms out.
CTRL + 0	Zooms to fit.
CTRL + H	Locks all macros.
SHIFT + CTRL + H	Unlocks all macros.
Hold SHIFT + Left_Mouse Click	Selects multiple elements in Design View Windows. If you select two items, the items and all items between them are selected.
Hold CTRL + Left Mouse click	Selects multiple elements in Design View windows.
ESC	Unselects all selected items and removes any pop-up windows.
<Right Arrow key>	Selects the element at next level of hierarchy in the Design Flow window.
<Left Arrow key>	Selects the element at previous level of hierarchy in the Design Flow window.
<Down Arrow key>	Selects the next element at the same level of hierarchy in the Design Flow window.
<Up Arrow key>	Selects the previous element at the same level of hierarchy in the Design Flow window.

2.1. Design View Window and View Tabs (Ask a Question)

When Chip Planner opens, it presents a Design View window with five view tabs:

- Port
- Logical
- Net
- Region
- Block - only if user blocks (*.cxz files) exist in the design

Each of the view tabs displays a design view. A selection of a design element in one view is reflected in other views. For example, when you click and select a bus port in the Port View, the Logical View shows the OUTBUF/INBUF primitives (for the bus) selected and the Net View shows the net (connected to the INBUF/OUTBUF of the port) selected.

Similarly, when a user region is selected in the Region View, the selection is reflected in the Floorplanner View as well.

The Design View window can be docked and undocked.

2.2. Find Window (Ask a Question)

Chip Planner provides a Find window for each of the five design views to search for design elements. You can also use the CTRL + F Hot Key. Multiple Find windows can be created for the same design view (Port/Logical/Net/Region/Block).

When the Find window opens, it is associated with a specific design view. Only design elements specific to the particular view are displayed. The view name (Port/Logical/Net/Region/Block) is displayed across the top of the window.

You can create multiple cloned Find windows for each view. Cloned Find windows are floating when they are opened and can be resized, moved, docked, or undocked (floating).

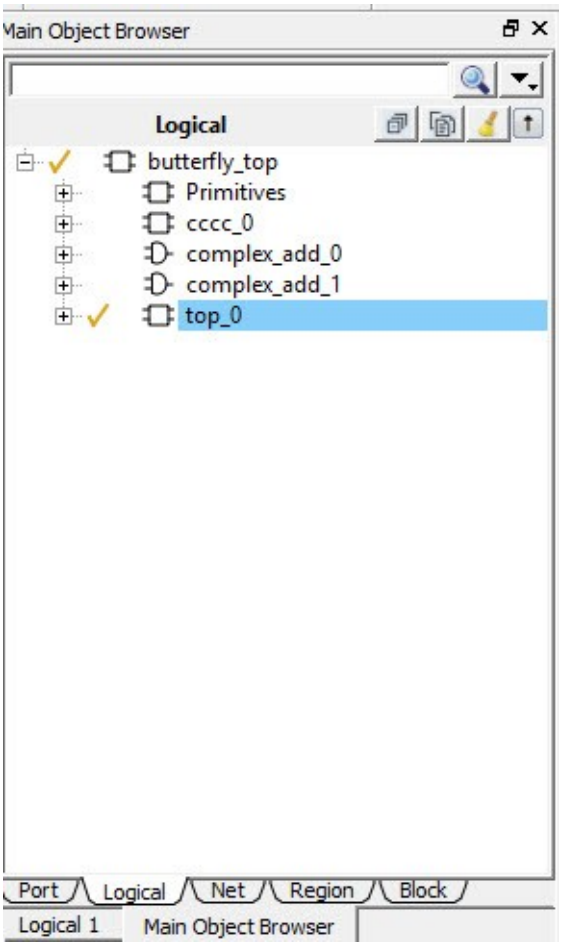
When the Find window is invoked in the Logical view, for example, the find window opens with the name Find (Logical) across the top of the window and the name Find # (Logical) across the top of the window when there are multiple cloned Find windows for the same View.

By default, each cloned Find window is named sequentially as Find 1 (<view_name>), Find 2 (<view_name>), Find 3 (<view_name>), and so on. The cloned Find windows can be renamed to a name different from the default.

A cloned Find window has the same features and functionality as the main view window. In addition, a cloned Find window has an additional icon called Rename Tree, which renames the cloned Find window to a name other than the default name.

Multiple Find windows are useful in floorplanning. For example, if your design has both a RAM and a MACC block, and want to filter, select both, and display them in the Floorplanner View, you need two Find windows for the logical view: one with the filter based on Macro type > RAM and the other with the filter based on Macro type > MACC.

Figure 2-2. Find (Logical View)



2.2.1. Search and Filter (Ask a Question)

Search and Filter operations are available for the five views (Port, Logical, Net, Region, and Block).

1. Open the Find windows and search for specific design elements.
2. Click the **Filter** icon ( ) in the Design View window or any cloned Find windows to search and filter the display. Three types of searches are available:
   - Wildcard Filter—such as "*" or "?" in the filter for wildcard matching. For example, when you type **FDDR*** in the filter, the FDDR component and all its lower level primitives are displayed.
   - Use Regular Match Filter.

- Regular Expressions—posix case insensitive regular expression search.

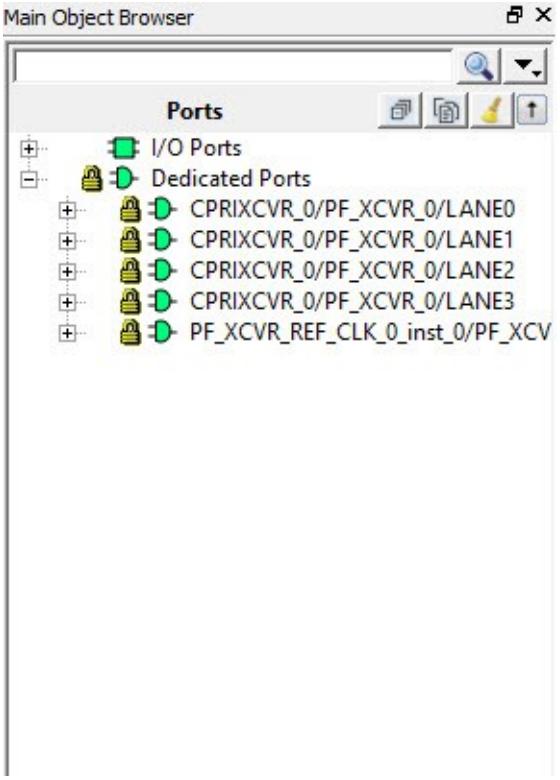
Note: All filtering is case-insensitive.

2.3. Port View (Ask a Question)

The Port View shows a hierarchical view of a design's Input, Output, and Inout ports. Regular I/Os and Dedicated I/Os are displayed as follows:

- Regular I/O ports—Input/Output/Inout ports that you can change or reassign. These appear under the **I/O Ports** tree.
- Dedicated I/Os—Special-purpose I/Os that cannot be changed or reassigned by you. These are shown under **the Dedicated Ports** tree.

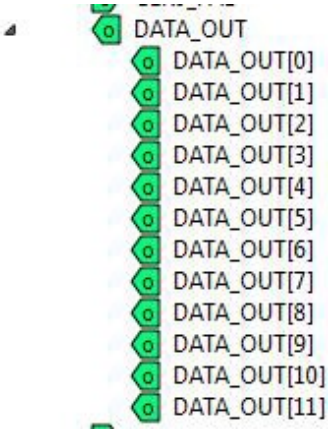
Figure 2-3. Port View (Dedicated Ports)



2.3.1. Port Buses (Ask a Question)

Scalar members of a bus port are grouped under the bus. All bus ports can be collapsed or expanded as shown in the following figure.

Figure 2-4. Bus Port DATA_OUT and Scalar Members



2.3.2. Port Properties (Ask a Question)

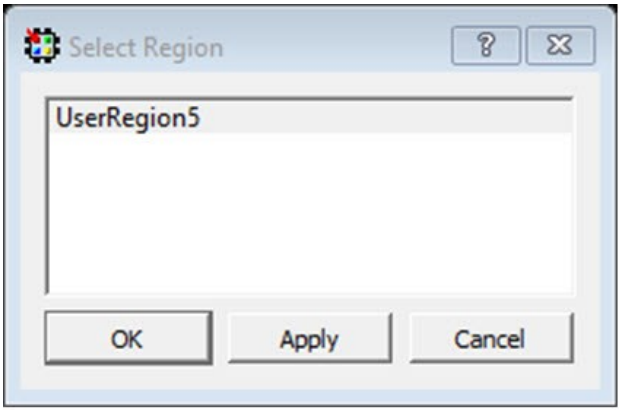
To see the properties of the port, select the port. The properties of the port you selected is displayed in the Properties Window. The selected port is also highlighted in the Floorplanner View and the World View.

2.3.3. User Actions in Port View (Ask a Question)

In the Port View, you can:

- Place ports to locations—Select a port, and then drag and drop it into the Floorplanner View at a valid resource location to assign the element to that location. All valid port locations are highlighted when you drag the selected element into the Floorplanner View.
- Unplace ports from locations—Right click the port and choose **Unplace From Location** to unassign a port.
- Lock Port to location—Right click the port and choose **Lock Placement** to lock selected port to the assigned location. This option is enabled only when the port is already placed in a location.
- Unlock Port from location—Right click the port and choose **Unlock Placement** to unassign the port. This option is enabled only when the port is already locked to a location.
- Region Assign—Right click a port and choose **Region Assign**. The Select Region dialog opens, and shows the regions available to assign that element. This dialog opens even if there are no User regions to which the selected item can be assigned. See the following figure.

Figure 2-5. Select Region Dialog Box



- Unassign Port from Region—Right click the port and choose **Unassign Macro to Region** to unassign a port macro from a region. This option is enabled only if the port is already assigned to a region.
- Unassign All—Right click the port and choose **Unassign All** to unassign all the ports that are assigned to regions.
- Unassign Selected Ports—Right click the port and choose **Unassign Selected Ports** to unassign all the selected ports that are assigned to regions.
- Check DRC rules of selected interface—For a selected interface, DRC rules can be verified by selecting this option. A message in the Log window informs you whether the DRC rule check is successful.

2.3.4. Port Sorting (Ask a Question)

Click the sort icon to sort the Ports by ascending or descending order, type, and port state:

2.3.5. Port Filtering (Ask a Question)

Either the traditional match filter or Regular Expression match filter is available. Enter a port name in the Filter text box to filter ports. Enable the **Use RegEx** check box to use Regular Expression match filtering.

2.3.5.1. Filter According to Port Types (Ask a Question)

The Port Filter list varies with the family and die.

2.3.5.2. Filter According to Port States (Ask a Question)

Port States filtering includes:

- Placeable—All I/Os that you can place.
- Unplaceable—All I/Os that you cannot place (for example, dedicated I/O).
- Assigned to location—All I/Os that can be assigned to a location.
- Not assigned to location—All I/Os that cannot be assigned to a location.
- Assigned to region—All I/Os that can be assigned to a region.
- Not assigned to region—All I/Os that cannot be assigned to a region.
- Locked—All I/Os that are locked.
- Unlocked—All I/Os that are not locked.

The following table lists the icons and the functions of the ports in the Port View.

Table 2-6. Ports and Icons

Icon	Name	Function
	Input Port	Represents an Input port.
	Output Port	Represents an Output port.
	Bidirectional Port	Represents a Bi-Directional port.
	White Background	Represents a port that is not placed.

Table 2-6. Ports and Icons (continued)

Icon	Name	Function
	Green Background	Represents a port that is placed.
	Blue Tick Mark	Represents an I/O that has been assigned to a region.
	Lock Icon	Represents an I/O that is fixed/locked to a location.

2.4. Logical View (Ask a Question)

The logical view is accessible from the Logical tab of the Design View window.

It displays a hierarchical view of all the logic inside the chip. The displayed Logic levels are:

- Component—Displays the logic at the component level. This represents the hierarchy in the design.
- Primitives—Displays the lowest level of the hierarchy (hard macro level). You can expand the hierarchy tree to see the lower level logic.

2.4.1. Logic Element Properties (Ask a Question)

Click the component/primitive to find out the properties of the logic element you have selected. The properties of the component/primitive are displayed in the Properties Window. The selected design element is also highlighted in the Floorplanner View and in the World View.

2.4.2. User Action in Logical View (Ask a Question)

Select a design element to:

- Assign elements to locations—Right click a design element and choose **Place to Location** to assign the element to that location. All valid resource locations are highlighted in the Floorplanner View when you drag the selected element into the Floorplanner View. Only a single element can be assigned at a time.
- Unassign element from location—Right click a design element and choose **Unplace from Location**. You can select multiple design elements/components and unassign them.
- Lock element to location—Right click a design element and choose **Lock Placement** to lock the selected element to an assigned location. This option is enabled only when the element is already placed in a location. You can select multiple design elements/components and lock them.
- Unlock element from location—Right click a design element and choose **Unlock Placement** to unlock or unfix a design element that is already locked to a location. This option is enabled when the element is already locked to a location. You can select multiple design elements/components and unlock them.
- Region assign—Right click a design element and choose **Region Assign**. A new Select Region dialog box provides you different regions available to assign that element. This dialog box appears even if there are no User regions to which the selected item can be assigned. You can also drag and drop the selected elements directly into a region in the Floorplanner View. If the selected elements are not compatible or over-booked for the desired region, the selection is not assigned to the region and invalid elements are shown in red in the Properties window.
- Unassign element from region—Right click a design element and choose **Unassign Macro from Region** to unassign a design element/macro from a region. This option is enabled only if the element is already assigned to a region. You can select multiple design elements/components and unassign them from a region.

- Unassign all—Right click the port and choose **Unassign All** to unassign all the elements that are assigned to regions.
- Unassign selected ports—Right click the port and choose **Unassign Selected Ports** to unassign all the selected elements that are assigned to regions.

2.4.3. Logical Filtering (Ask a Question)

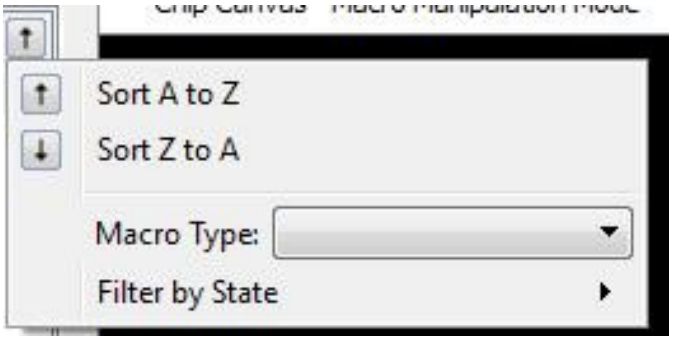
Enter a macro name in the Filter text box to filter the design elements. From the pull-down menu of the Sort icon, choose either the traditional match filtering, wildcard filtering, or Regular Expression match filtering.

2.4.4. Logical Sorting (Ask a Question)

Click the Sort icon:

to sort in ascending or descending order, the type (Filter by Macro Type), and state (Filter by State) of the logic element.

Figure 2-6. Macro Filter



2.4.5. Logical Filtering (Ask a Question)

Enter a macro name in the Filter text box to filter the design elements. From the pull-down menu of the Sort icon, choose either traditional match filtering, wildcard filtering, or Regular Expression match filtering.

2.4.5.1. Filtering by Macro Types (Ask a Question)

Available Macro types are family/die-dependent. For a list of Macro filters specific to the family/technology of your project, see Cross-Probing from SmartTime to Chip View/Netlist View.

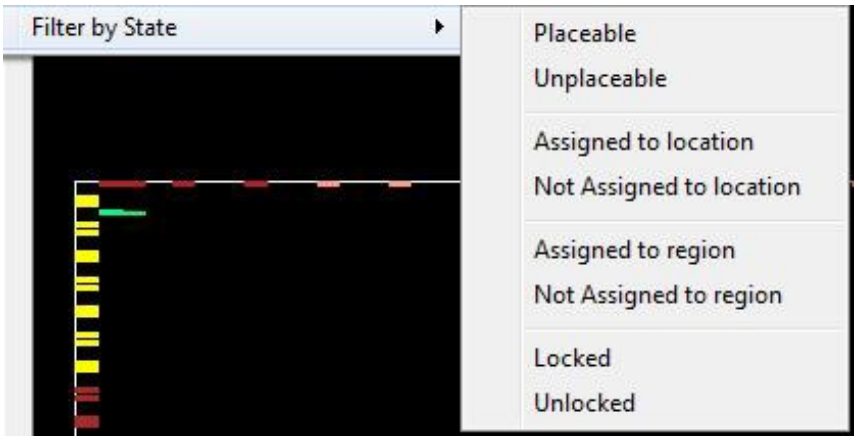
2.4.5.2. Filtering by Macro State (Ask a Question)

The Logical View displays the filter results based on the state of the Logical elements:

- Placeable—All macros that you can place. This option is mutually exclusive with the Unplaceable option.
- Unplaceable—All macros that you cannot placed. This option is mutually exclusive with the Placeable option.
- Assigned to Location—All macros that can be assigned to a location. This option is mutually exclusive with the Not assigned to Location option.
- Not assigned to Location—All macros that cannot be assigned to a location. This option is mutually exclusive with the Assigned to Location option.
- Assigned to Region—All macros that can be assigned to a region. This option is mutually exclusive with the Not assigned to Region option.

- Not assigned to Region—All macros that cannot be assigned to a region. This option is mutually exclusive with the Assigned to Region option.
- Locked—All macros that are locked. This option is mutually exclusive with the Unlocked option.
- Unlocked—All macros that are not locked. This option is mutually exclusive with the Locked option.

Figure 2-7. Macro State Filter



The following table lists the macros displayed in the Logical View.

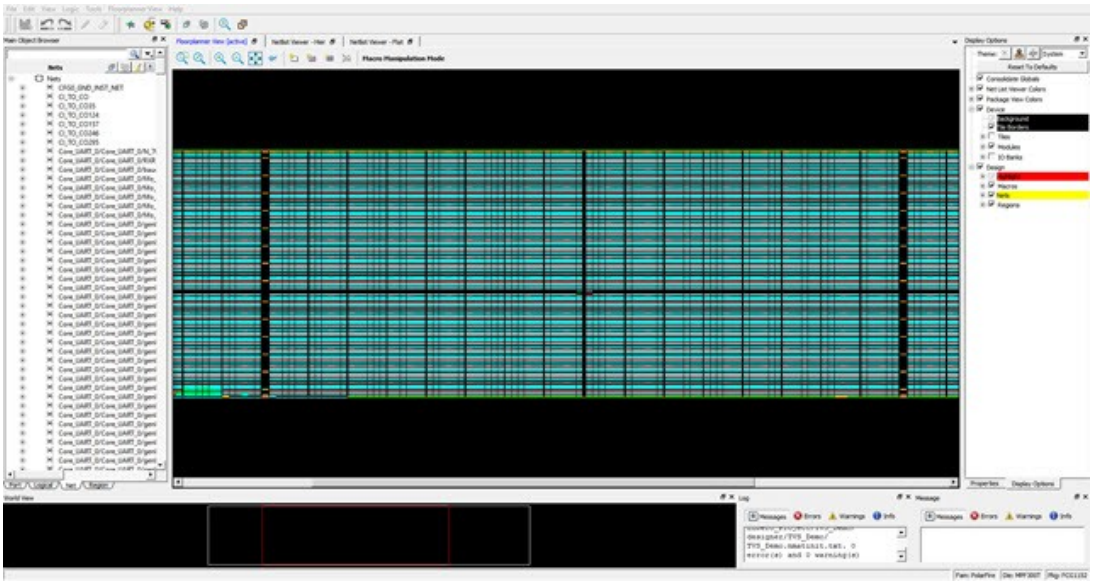
Table 2-7. Macros in Logical View

Icon	Name	Function
	Component/Top Level Macro	Represents a Design Component or Top level macro that has a lower level macro.
	Comb/Seq Element	Represents the lowest level element associated with a fabric resource.
	Input Port Macro	Represents a macro associated with an Input port.
	Output port macro	Represents a macro associated with an Output port.
	Bi-Directional port	Represents a macro associated with a Bi-Directional port.
	Global Resource	Represents a macro assigned to Global Resources/Row Global Resources.
	Block Element	Represents a design element associated with a block or an IP interface.
	White background	Represents a design element that is not placed.
	Green background	Represents a design element that is placed.
	Blue tick mark	Represents a design element that has been assigned to a region.
	Lock Icon	Represents a design element that is fixed/locked to a location.

2.5. Net View (Ask a Question)

The Net View displays a flattened net view of the design and all the nets associated with the design. In addition to showing each net, this view shows the pins connected to the net.

Figure 2-8. Net View



2.5.1. Net Properties (Ask a Question)

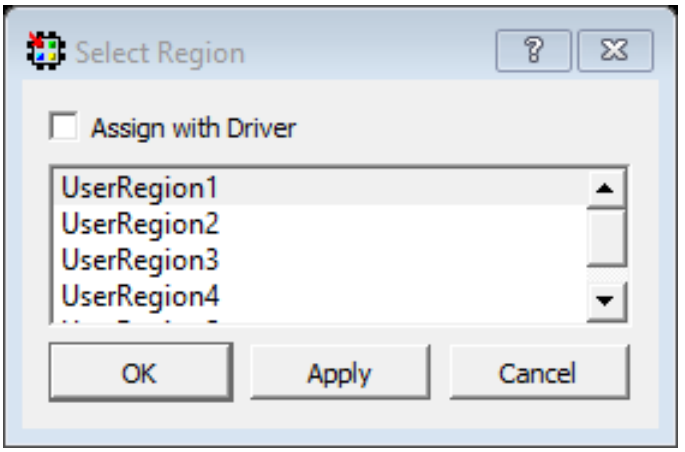
Click to select the net. The net properties are displayed in the Properties Window. The selected net is also highlighted in the Floorplanner View and the World View.

2.5.2. User Actions in Net View (Ask a Question)

From the Net view, you can:

- Change Net Color—Right click a net and choose **Net Color** to change the net color. This opens a color palette from which you can assign the desired color to the selected net.
- Region Assign—Right click a design element and choose **Region Assign**. The Select Region dialog opens, and shows the regions available to assign that element. This dialog box opens even if there are no User regions to which the selected item can be assigned. See the following example.

Figure 2-9. Select Region Dialog Box



- Check the **Assign with Driver** check box to assign all the net macros including driver macros to a region. This option is enabled if there is a valid Region created over the required resources. You can select multiple nets and assign them to a region.
- Unassign All—Right click the port and choose **Unassign All** to unassign all the nets that are assigned to regions.

- Unassign Selected Nets—Right click the port and choose **Unassign Selected Nets** to unassign all the selected nets that are assigned to regions.

2.5.3. Sorting (Ask a Question)

Sort the nets in ascending or descending order.

2.5.4. Filtering (Ask a Question)

Enter a net name in the Filter text box to filter net names. From the pull-down menu of the Sort icon, choose either traditional match filtering, wildcard filtering, or Regular Expression match filtering. You can also filter with criteria specific to nets, such as fanout values, net types, and routing status (routed or unrouted).

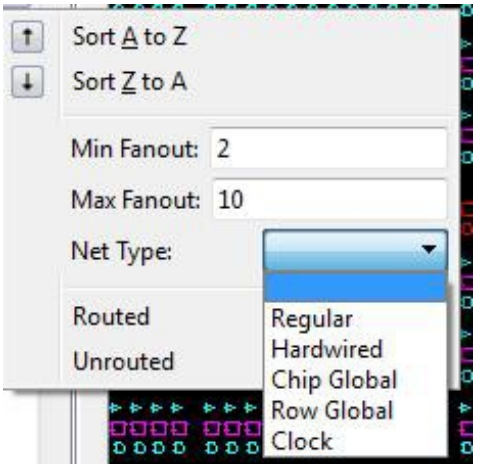
2.5.4.1. Filter Criteria Based on Fanout Value (Ask a Question)

Options are:

- Max Fanout—Enter a value to display nets with a maximum fanout value.
- Min Fanout—Enter a value to display nets with a minimum fanout value.

Note: Max Fanout and Min Fanout are logical ANDed together. If the Max Fanout has a value of 10 and the Min Fanout has a value of 2, the Net View displays only nets that meet both conditions. In this case, only nets with a fanout range of 2 to 10 are displayed.

Figure 2-10. Net Filter Options



The following table lists the icons specific to the Net View.

Table 2-8. List of Net Icons

Icon	Name	Function
	Regular/Hardwired Net	Represents a regular or hardwired net.
	Global Net	Represents a net that is routed through Chip Global/ Row global resources.
	Driven Macros	Represents a list of macros that are driven by this net.
	Driver Macros	Represents a macro that is driving this net.
	Blue tick mark	Represents a net that has been assigned to a region.

2.5.4.2. Filter Criteria Based on Net Type (Ask a Question)

The net type and the filter list is family/die-specific. For the list of net filters specific to the family/ technology of your project, see Cross-Probing from SmartTime to Chip View or Netlist Viewer.

2.5.4.3. Filter Criteria Based on Routing Status (Ask a Question)

Options are:

- Routed—Displays all routed nets.
- Unrouted—Displays all unrouted nets.

2.5.5. Global Nets (Ask a Question)

A global net is a net that uses global routing resources for routing a signal from source to destination logic clusters. These include Chip Globals Resources/Global Buffers (GB), Row global resources/row global buffers (RGB), and Half-Chip Globals (HGB for RTG4). Clocks, Async Reset, and nets with high fanout are typically routed through these global routing resources.

Global signals (G[n:0]) reach the logic clusters through row global signals (RG[7:0]) generated by an associated row global buffer (RGB). RGB are inferred by the layout tool. Depending on the placement of the design elements, it distributes the fanout of the global nets across multiple RGBs. The Net View shows this break-up for such global nets.

The following figure shows an example of Global Nets with different fanouts.

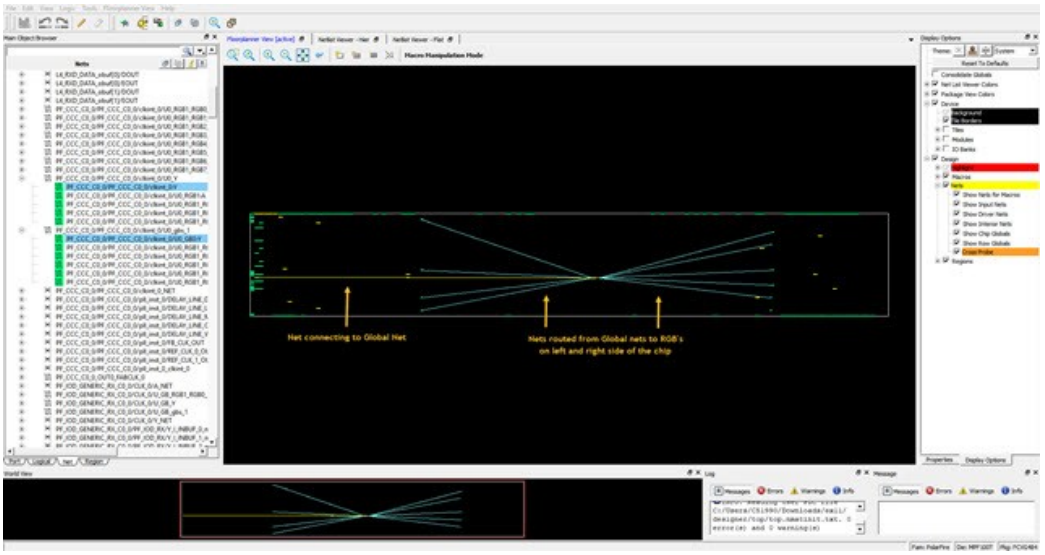
Figure 2-11. Global Nets Information with Different Fanouts Shown

Global Nets Information

	From	GB Location	Net Name	Fanout
1	PF_CCC_C0_0/PF_CCC_C0_0/clkint_0/U0	(864, 81)	PF_CCC_C0_0/PF_CCC_C0_0/clkint_0/U0_Y	24
2	PF_CCC_C0_0/PF_CCC_C0_0/clkint_0/U0_GB0	(876, 81)	PF_CCC_C0_0/PF_CCC_C0_0/clkint_0/U0_gbs_1	23
3	PF_IOD_GENERIC_RX_C0_0/CLK_0/U_GB	(865, 82)	PF_IOD_GENERIC_RX_C0_0/CLK_0/U_GB_Y	5
4	PF_IOD_GENERIC_RX_C0_0/CLK_0/U_GB_GB0	(877, 82)	PF_IOD_GENERIC_RX_C0_0/CLK_0/U_GB_gbs_1	1

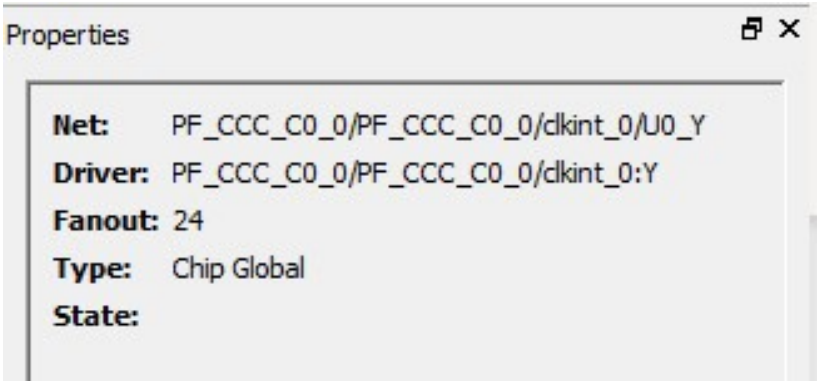
The following figure shows the Floorplanner View of the Global Net.

Figure 2-12. Floorplanner View of Global Nets



The following figure shows the Properties window of Global Nets, which appears at the right side of the Floorplanner View.

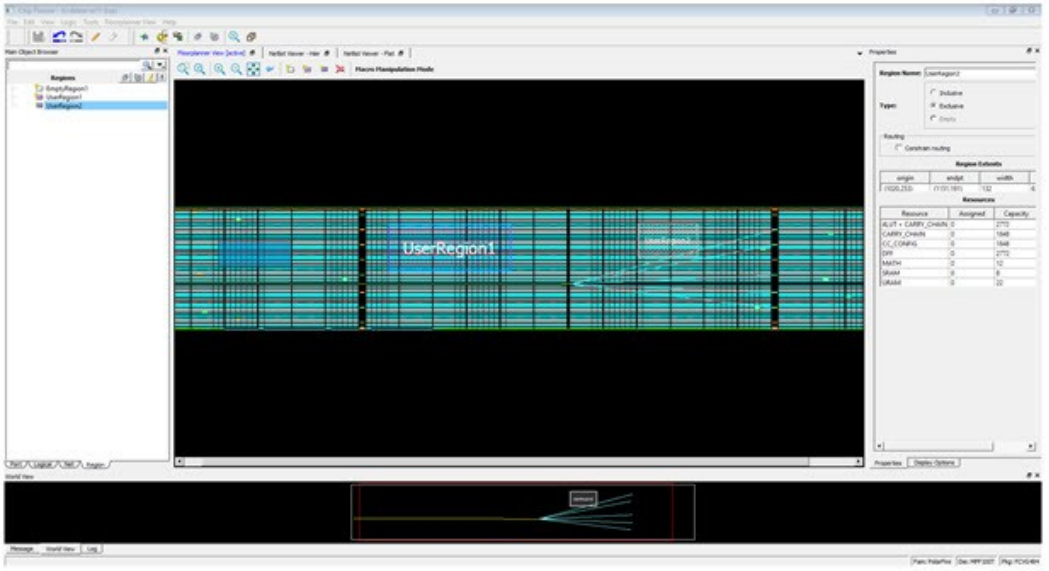
Figure 2-13. Properties Window View of Global Nets



2.6. Region View (Ask a Question)

The Region View displays the regions you have created and all Components, Macros, and Nets assigned to the region. When you create a region, by default the region is named UserRegion1, UserRegion2, and so on. When you select in the Region View, the properties of the Region you select are displayed in the Properties Window. When you select an item in the hierarchical tree display, all sub-items are selected.

Figure 2-14. Region View



2.6.1. User Regions and Region Types (Ask a Question)

Three types of regions are available for creation:

- Inclusive Region
- Exclusive Region
- Empty Region

You can select a region to perform the following activities:

- Delete—Deletes a selected region.
- Clone—Clones a selected region.
- Rename—Renames a selected region.
- Merge—Merges two or more regions. This option is enabled if there are more than two regions selected.
- Assign macros inside Region—Assigns macros that are part of a region area assigned to the selected region.
- Unplace From location—Unassigns all design elements that are part of a selected region from their placed locations.
- Lock Placement—Locks all macros that are part of a selected region.
- Unlock Placement—Unlocks all macros that are part of a selected region.
- Unassign All—Unassigns all the elements from a region.
- Unassign Selected Ports—Unassigns all the selected ports from a region.
- Unassign Selected Nets—Unassigns all the selected nets from a region.
- Unassign Selected Components—Unassigns all the selected components from a region.

2.6.2. User Actions on Regions in Floorplanner View (Ask a Question)

You can select a region in the Floorplanner View to perform the following activities:

- Delete—Deletes a selected region.
- Clone—Clones a selected region.
- Rename—Renames a selected region.

- Merge—Merges two or more regions. This option is enabled if there are more than two regions selected.
- Assign macros inside Region—Assigns macros that are part of a region area assigned to the selected region.
- Unplace From location—Unassigns all design elements that are part of a selected region from their placed locations.
- Lock Placement—Locks all macros that are part of a selected region.
- Unlock Placement—Unlocks all macros that are part of a selected region.
- Unassign All—Unassigns all the elements from a region.
- Unassign Selected Ports—Unassigns all the selected ports from a region.
- Unassign Selected Nets—Unassigns all the selected nets from a region.
- Unassign Selected Components—Unassigns all the selected components from a region.

2.6.3. Region Properties (Ask a Question)

Click the region in the Region View. The properties of the region you selected are displayed in the Properties Window. The selected region is also highlighted in the Floorplanner View and the World View.

2.6.4. Region Filtering (Ask a Question)

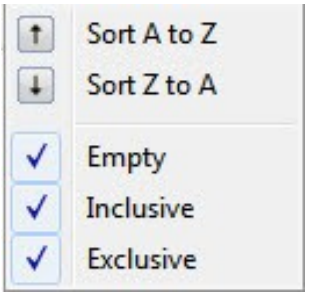
Enter a region name in the Filter text box. From the pull-down menu of the Sort icon, choose traditional match filtering, wildcard filtering, or Regular Expression match filtering.

2.6.5. Region Sorting (Ask a Question)

In addition to ascending or descending order display, a filter is available for the Region View to display user regions based on region types:

- Inclusive—Shows all inclusive regions.
- Exclusive—Shows all exclusive regions.
- Empty—Shows all empty regions.

Figure 2-15. Region View Filter



The following table lists the icons specific to the Region View Filter.

Table 2-9. Region Filter

Icon	Name	Function
	Inclusive	Represents an inclusive region.

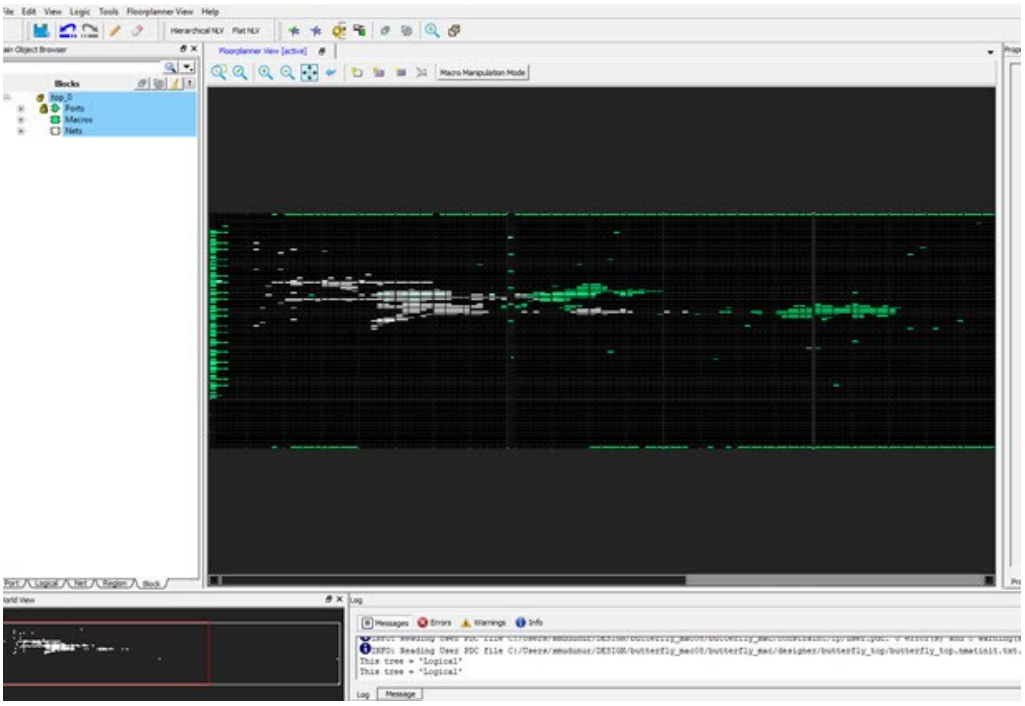
Table 2-9. Region Filter (continued)

Icon	Name	Function
	Exclusive Region	Represents an exclusive region.
	Empty Region	Represents an empty region.
	Nets	Represents a net associated with a region.
	Component/Top Level Macro	Represents a Design Component or Top level macro that have lower level macros.
	Comb / Seq Element	Represents the lowest level element associated with a fabric resource.
	Output port macro	Represents a macro associated with an output port.
	Input Port Macro	Represents a macro associated with an Input port.
	Green background	Represents a design element that is placed.
	Blue tick mark	Represents a design element that has been assigned to a region.
	Lock Icon	Represents a design element that is fixed/locked to a location.

2.7. Block View (Ask a Question)

The block view displays the low-level design blocks (*.cxz files) you have imported into the Libero SoC project. This tab appears only when design blocks exist in the project. These low-level design blocks may have completed the Place and Route step and met the timing and power requirements of the design block.

Figure 2-16. Block View Example



The Block View displays all the design blocks in the project and displays the following design elements for each design block:

- Macros
- Nets
- Ports

2.7.1. Block Properties (Ask a Question)

Click to select the block in the Block View and the properties of the block are displayed in the Properties Window. The selected block is also highlighted in the Floorplanner View and the World View.

2.7.2. Block Filtering (Ask a Question)

Enter a block name in the Filter text box to filter blocks. From the pull-down menu of the Sort icon, choose traditional regular match filtering, wildcard filtering or regular expression match filtering.

You can sort the blocks in ascending or descending order.

2.8. Properties Window (Ask a Question)

The Properties window displays the properties of the design elements. The items shown in the Properties window depends on what is selected in the design view.

2.8.1. Properties of Logical View Elements (Ask a Question)

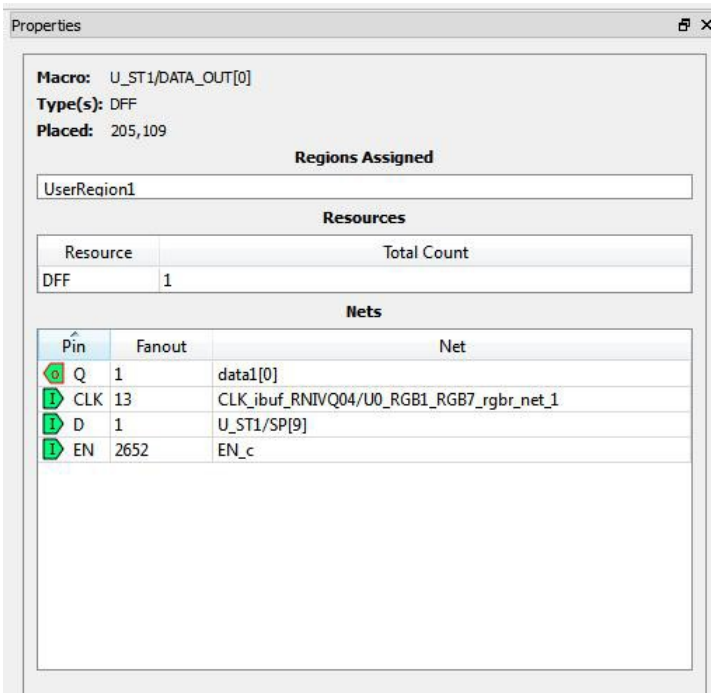
The Properties window displays the properties of a component or macro when it is selected in the Logical View. Properties displayed may include the following, depending on the type of design elements:

- Macro/Component Name—Full macro or component name based on selection in logical view.
- Cell Type—Resource type based on design element selection.
- Placed (Location)—X-Y coordinates where device element is placed.

- Resource Usage Table—Table showing resources based on component and macro selection.
- Region Attached Table—Table showing region to which selected macro/component is assigned.
- User region (if any) to which it is attached.
- Nets Table—Table showing pins and nets associated with the selected macro along with fanout value.
- Locked/Unlocked (Placement)—Selected port is locked or unlocked.
- Port—Port name to which the I/O macro is assigned (only shown for I/O port macros).
- I/O Technology Standard—I/O technology associated with the selected I/O macro (shown only for I/O port macros).
- I/O Bank—I/O bank to which the selected I/O macro is assigned (only shown for I/O port macros).
- Pin (Package Pin)—Pin to which the macro is assigned (shown only for I/O port macros).

Note: Not all properties in the list are displayed. The list of displayed properties varies with the type of design element selected in the Logical View.

Figure 2-17. Example of Properties Window (Logical View)



2.8.2. Properties of Port View Elements (Ask a Question)

When a design element (I/O Bus or Scalar I/O) is selected in the Port View, the Properties window displays the properties of a bus (for I/O bus) or a macro (for scalar I/Os).

For an I/O bus, the Properties window displays:

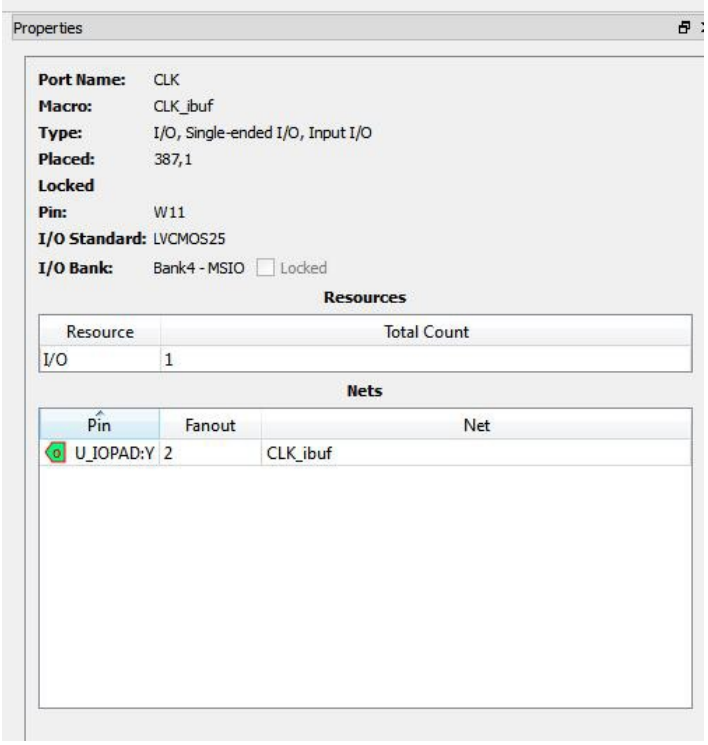
- Resource Usage Table—Shows all resources associated with the selection.
- Ports Table—Displays a table with I/O Bank, I/O Technology Standard, Package Pin, and Port Names of each individual member of the bus.

For scalar I/O ports, the Properties window displays the macro information:

- Port Name—Full Name of the selected port.
- Macro—Name of the macro associated with the selected port.

- Port Type of selected I/O.
- Placed (Location)—X-Y coordinates where device element is placed.
- Locked/Unlocked (Placement)—Selected port is locked or unlocked.
- Pin (Package Pin name)—Pin name to which selected port is assigned.
- I/O Technology Standard—I/O standard associated with the port.
- I/O Bank—I/O bank associated with the selected port.
- Resource Usage table.
- Nets Table—Table showing pins and nets associated with the selected port along with fanout value.

Figure 2-18. Example of Properties Window (Ports View)

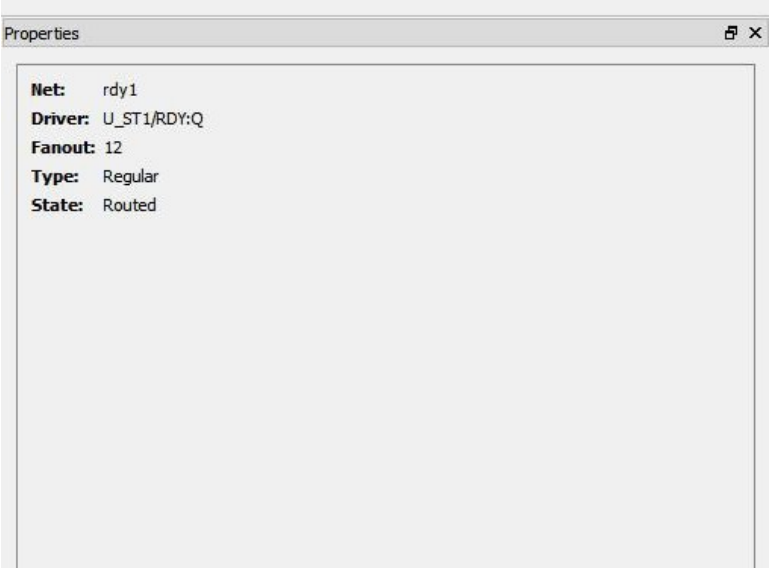


2.8.3. Properties of Nets (Ask a Question)

For nets selected in the Net view, the Properties window displays the following:

- Net Name—Full name of the selected net.
- Driver Name—Macro that is driving the selected net.
- Fanout—Fanout value of the selected net.
- Type—Regular, Hardwired, or Global for the selected net.
- State—Routed or Unrouted net.

Figure 2-19. Example of Properties Window (Net)



2.8.4. Properties of Region (Ask a Question)

Region properties are displayed in the Properties window when a user region is selected in the Floorplanner View or in the Region View.

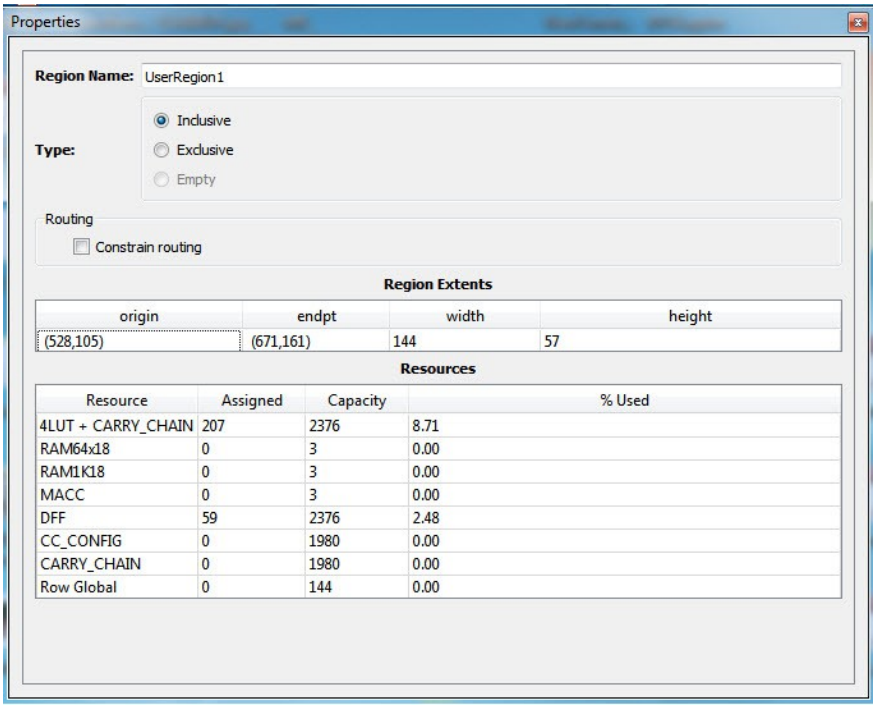
The properties window for a region displays the following:

- Region Name—By default, the regions are named UserRegion1, UserRegion2, and so on when first created. You can change the region name by editing the Region name text box in the Properties window.
- Type of Region—Inclusive, Exclusive, or Empty.
- Routing Requirements

Constrain routing—Instructs the Place and Route tool to apply routing restrictions, in addition to Placement restrictions, to the user regions.

- Region Extents—Displays the X-Y coordinates of the origin (lower left corner) and the endpoint (upper right corner) and the width and height of the region.
- Resources in the Region—Displays the logic resources in the region, including used (Assigned) resources and total available resources (Capacity) and a percentage of used resources (Assigned) relative to the total resources (Capacity). A percentage greater than 100 indicates resource overbooking, which is not allowed. The overbooked resource is highlighted in red.

Figure 2-20. Example of Properties Window (Region)



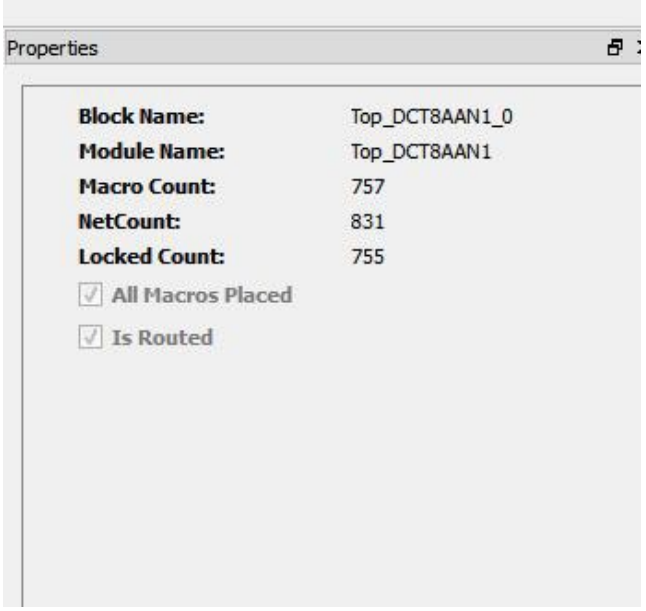
2.8.5. Properties of Blocks (Ask a Question)

When a block is selected in the Block View, the Properties window displays:

- Block Name—Name of the selected block.
- Module Name—Name of the block module.
- Macro Count—Total number of macros in the block.
- Net Count—Total number of nets in the block.
- Locked Count—Total number of locked macros.

In addition, it specifies whether all the macros are placed and/or routed.

Figure 2-21. Properties of Block



3. Display Options Window (Ask a Question)

The **Display Options** window allows you to customize the layout and the color settings for design elements on the **Floorplanner View** to meet your personal preferences.

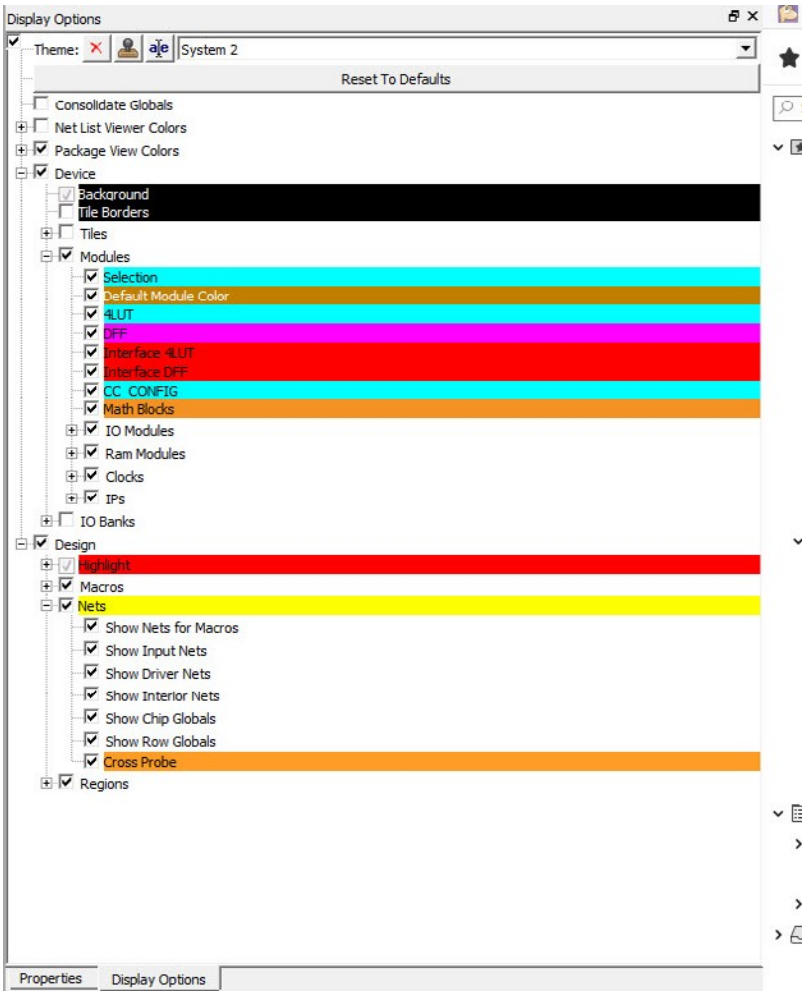
There are three default layers and colors settings group that are provided with Chip Planner:

- System
- Pin_Planner
- Grey_Scale

By default, Chip Planner launches with “System” layers and colors settings group for the **Device** (Silicon feature) and the **Design** elements. These are the System Default Settings.

The following figure shows the color setting for MPF300TS die (PolarFire).

Figure 3-1. Default Color Setting for Device (Silicon Hardware)



The device color setting is a hierarchical view. You may expand each group to see the lower level items and see the default color setting for each. The device cell types, I/O banks are die-dependent and reflects the available hardware components for the selected die.

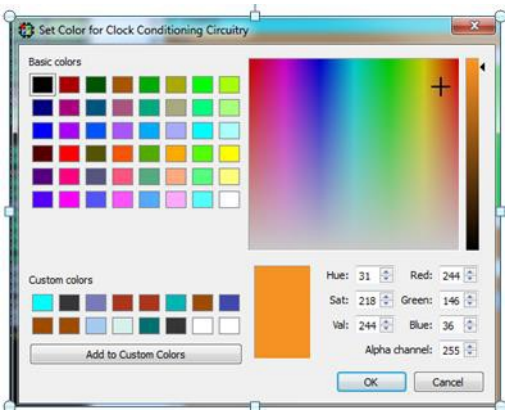
Similarly, the color settings for the **Design** elements are displayed in a hierarchical view. Expand the group to see the default color setting for each lower level **Design** element.

3.1. Changing Color Settings (Ask a Question)

To change the color setting for a device or design element from the default setting:

1. Right click the color for the element.
2. In the Set Color dialog box, move the Cross across the color spectrum to the color you prefer.
3. Click **OK**.

Figure 3-2. Set Color Dialog Box to Change Color



3.2. Displaying an Instance in the Floorplanner View Using the Display Options Window (Ask a Question)

You can use the check box provided against each menu item to select the elements you want to see in the Floorplanner View.

Some of the options in Display Options window cannot be unchecked, as these options are fixed for any design. Such options have check boxes grayed-out and are always enabled. However, you can still change the colors settings of these options.

Design Option in Display Options windows can be grouped according to Macro Type and State of Macro. The display of design elements in the Floorplanner View depends on both conditions met: the Macro Type and the State of macro. For example, if you want to see 4LUT elements of your design, you need to select both Movable and Placed Macro and 4LUT options.

The following table lists the icons specific to the Display Options window.

Table 3-1. Display Options Icons

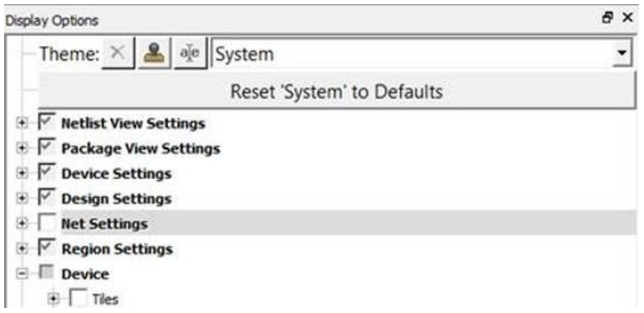
Icon	Name	Function
	Rename Settings	Renames user created layers and colors settings from the default name to a name you specify.
	Remove Settings	Removes the user defined Layers and colors settings.
	Clone Settings	Creates a clone of current Layers and Colors Settings.

3.3. Creating Personal Settings (Ask a Question)

You can create your display settings according to your preferences.

1. Create a clone from one of the selected settings (Grey Scale, Pin Planner, System) using **Clone Setting** icon in the Display Options window.

Figure 3-3. Clone Settings in Display Options Window



2. Accept the default name “Group #” for the settings name or rename it from the Display Options window.
3. Change color settings and/or select items to be displayed from the Display Options window.

The customized settings can be created and preserved on your system and will always be available in the drop-down group list in the Display Options window. The customized settings are available to you across different projects on the same machine.

3.4. Selection (Ask a Question)

Clicking an item selects that one object in the model. However, you can select multiple items:

- To select contiguous items, click the first item you want to select, and then hold down the Shift key and click the last item you want to select. All items between the two are selected automatically.
- To select items that are not contiguous. click the first item. Then hold down the Ctrl key and click each additional item you want to select.

If you selected multiple items and then change your mind about a selected item, you can deselect the item by holding down the Ctrl key and clicking the item.

Selections follow a symmetrical behavior: If you select a port, all macros attached to it are selected as well. Similarly, if you select a pin object, all corresponding macro objects are also selected.

For example, if you select a port, the macro is also shown as selected. However, the property page still points to the port. Pin selection follows the same behavior.

3.5. Highlighting (Ask a Question)

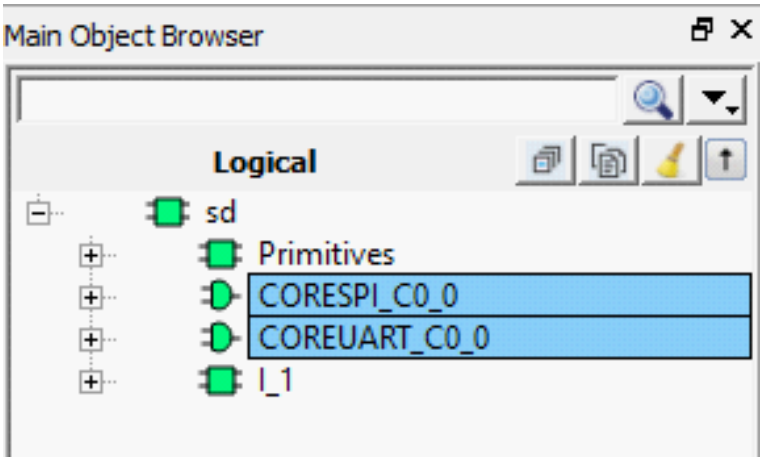
The Highlighting option allows you to set persistent colors on designated macros, nets, or both across the system.

To set a highlight, go to the **Logical Object Browser** or the **Net Object Browser**, select one or more macros and/or components, and click the pencil icon as shown in the following toolbar.

Figure 3-4. Pencil and Eraser Icons

When you set a highlight, all selected macros, ports, and/or nets in the design are marked with the selected color. The selected color appears in the left object browser tree. The following figure shows the left Main Object Browser with the logical tree displayed. To select both components, click one component, hold down the Ctrl key and click the other component.

Figure 3-5. Example of Highlighting Shown in the Object Browser Tree



The color remains until you select one of the two middle eraser icons:

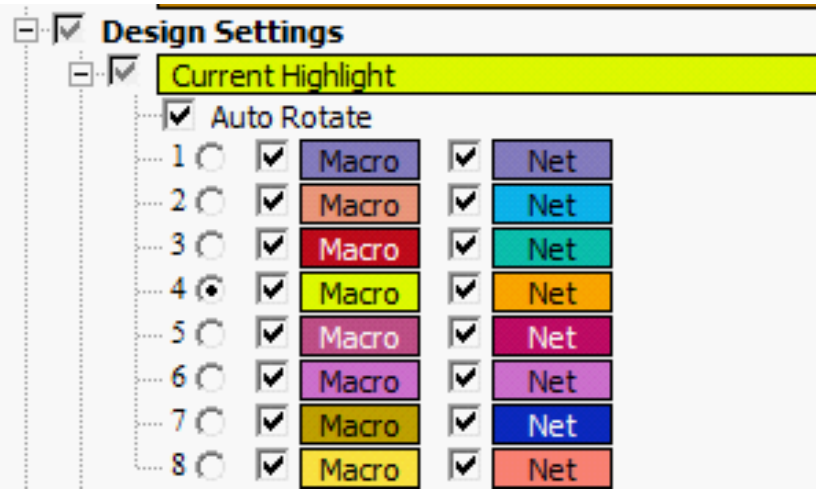
- The left eraser icon removes all highlights.
- The right eraser icon removes highlights only from selected items.

To set the highlights, use the **Current Highlight** check box from the **Design Settings** docking window. Below this check box are an **Auto Rotate** check box, along with eight **Highlight** check boxes and radio buttons.

- Use the **Highlight** check boxes to enable or disable a highlight. Separate check boxes are provided for macros and nets.
- Use the **Highlight** radio buttons to designate which highlight is active.

Note: You cannot disable the active highlight.

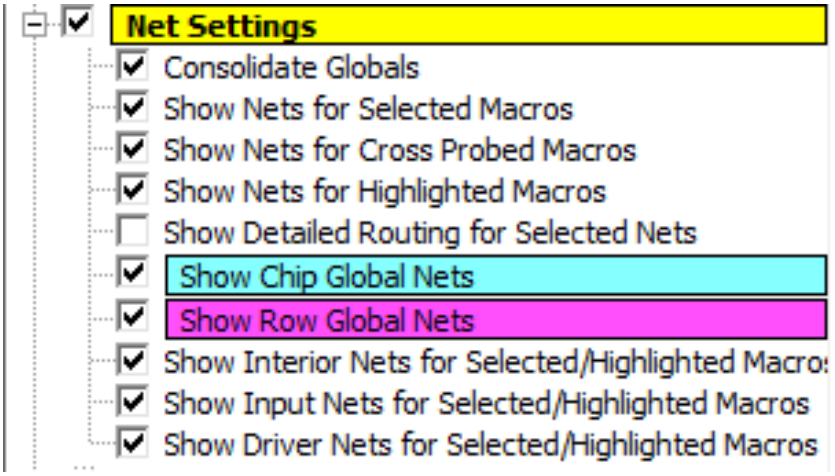
Figure 3-6. Design Settings Docking Window



Clicking the colored box next to each check box allows you to select a color for that macro or net.

The following figure shows an example of the results when all options under **Nets** are exposed.

Figure 3-7. Example of Exposing All Nets



If **Net Settings** is not checked, all nets in the system, except cross-probe nets, are disabled. All options subordinate to that option are marked with a gray box to show that the option is not used. If **Show Nets for Highlighted Macros** is not checked, all net options inside the currently highlighted net selections are disabled. To restore the color of these options, check the individual options. If you check **Show Nets for Highlighted Macros**, the individual settings in the highlight settings area determine whether nets will be drawn.
Note: If you enable **Auto Rotate** and **Net** under **Auto Rotate**, and then uncheck the check box in the **Net** color selection, the net color in the Net view is not consistent with that of the Planner.

The **Consolidate Globals** option converts the raw clock display with globals connected to locals as if the sum of the local nets and the global nets are the same net. This is for display purposes only. The bottom three options in the Design Settings docking window work with groups of macros and ports for which you consider net lines as a single entity:

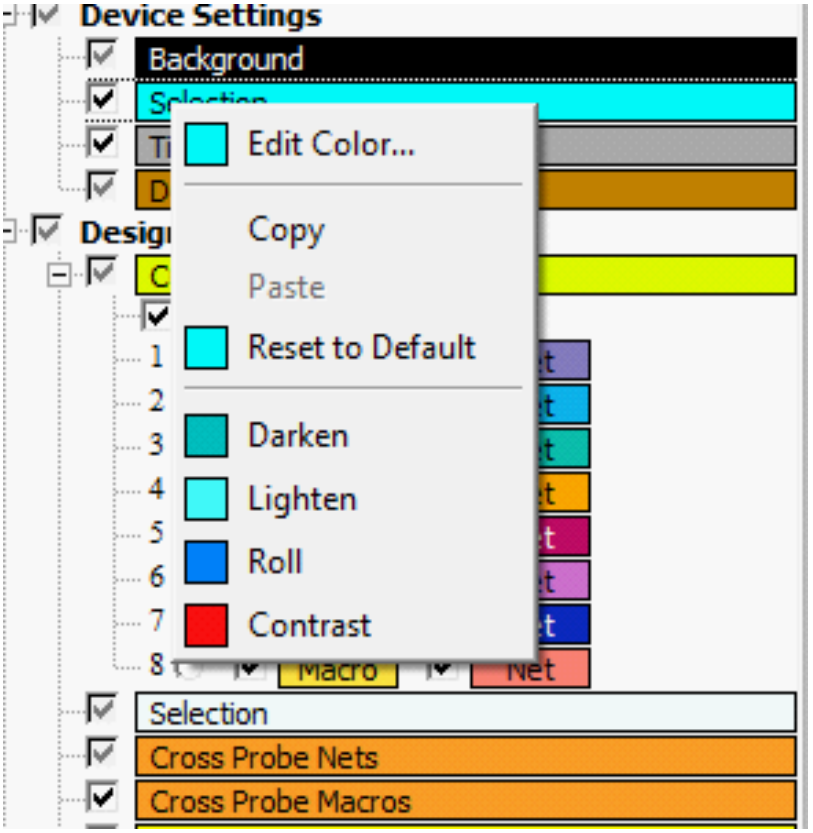
- **Show Interior Nets for Selected/Highlighted Macros** shows lines that connect two different macros in the group.
- **Show Input Nets for Selected/Highlighted Macros** shows lines that connect an output port of an exterior macro to one or more input pins in the group.
- **Show Driver Nets for Selected/Highlighted Macros** shows drivers in the group that connect with an exterior macro.

3.5.1. Changing an Option Color (Ask a Question)

To change the color associated with an option:

1. Right click the option under **Device Settings**.
   A right click menu similar to the following appears.

Figure 3-8. Right Click Menu



2. Select an option from the right click menu. The following table describes the options.

   Note: The **Darker** and **Lighter** work well with fully saturated colors, but not for extremes; however, you can use the **Set Color** dialog box to achieve the desired result. If you apply the **Contrast** option twice, you will get approximately the same color fully saturated.

Tip: You can also change option colors from one active element to another by selecting an active element under **Device Settings**, and then dragging the colored rectangle to the destination element.

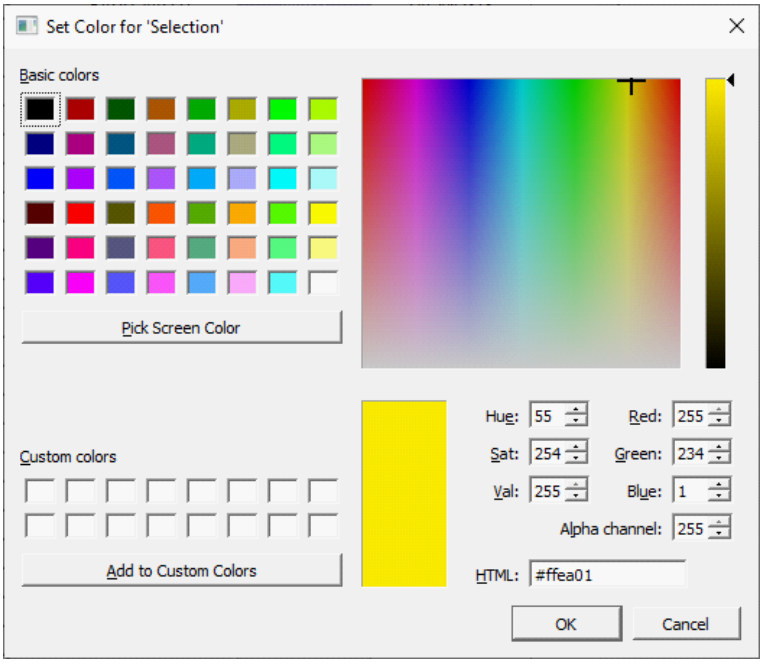
Table 3-2. Options from the Right Click Menu

Option	Description
Edit Color	Displays the Set Color dialog box as shown in the following figure. Use this dialog box to choose a color from a set of basic or custom color palettes. Alternatively, you can generate a color value by modifying the hue, saturation, luminosity (HSL) or red, green blue (RGB) color values. **Note:** Selecting fully or mostly transparent option colors can lead to unexpected results. For example, if you make a color fully transparent, you can have the option selected while rendering the color invisible.
Copy	Saves the color of the current option.
Paste	Makes the color of the option the same as the saved color.
Reset to Default	Resets the values for the selected option.
Darken	Creates a darker version of the color.
Lighten	Creates a lighter version of the color.

Table 3-2. Options from the Right Click Menu (continued)

Option	Description
Roll	Moves the hue 60 degrees around the hue, saturation, value (HSV) color wheel.
Contrast	Creates a fully saturated color, with the hue rotated 180 degrees.

Figure 3-9. Set Color Dialog Box

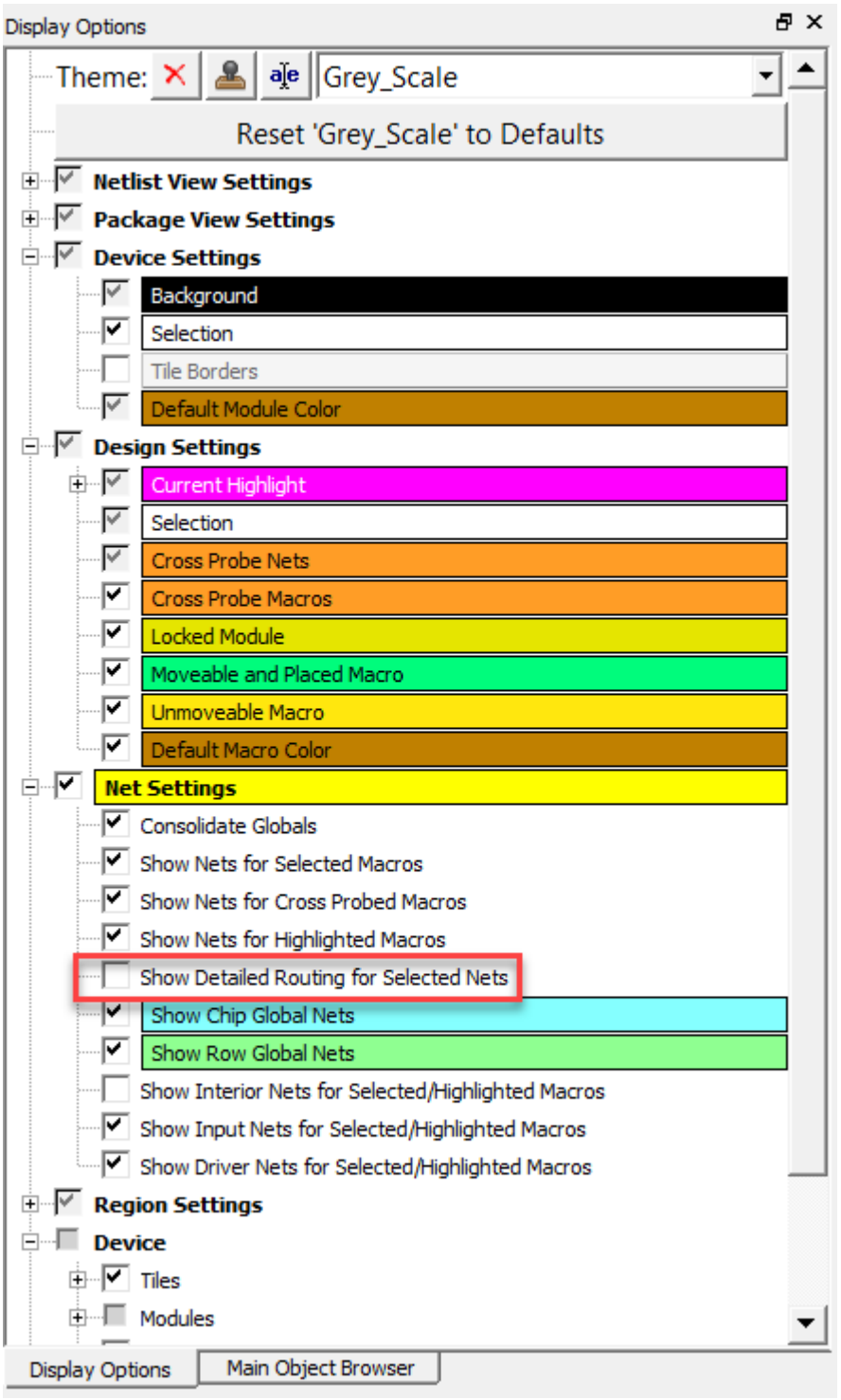


3.6. Displaying Routing Views (Ask a Question)

Chip Planner provides the **Show Detailed Routing for Selected Nets** option to PolarFire and PolarFire SoC users.

Checking this option displays detailed routing for selected nets. This is a global option, which means it applies to all Libero projects associated with the user when selected. By default, this option is not selected, which displays the net as rasnets.

Figure 3-10. Show Detailed Routing for Selected Nets



3.7. Cross Probing (Ask a Question)

When an external application performs a cross probe, the elements colored for cross probing and cross probe nets are always displayed. There are no options that allow cross probing to be disabled or turned off; however, you can change the cross probing color to transparent.

Any additional cross probes get added to the current ones. To clear a cross probe state, use the rightmost eraser icon in the following toolbar.

Figure 3-11. Pencil and Eraser Icons

3.8. Removing Custom Setting Group (Ask a Question)

To delete the custom setting group, select the custom setting group and click **Remove Setting icon** in Display Options window.

Note: The System setting is the default group and it cannot be removed. Only user-set custom settings can be removed.

3.9. Reset to System Default (Ask a Question)

Click **Reset <group_name> to Default** to reset the group's settings to the system default settings.

3.10. Consolidate Globals (Ask a Question)

When this box is checked, the Row Globals (RGB) are hidden from the Floorplanner View. RGBs do not exist in the user netlist. They are buffers inserted by Libero SoC after layout. When this option is turned on, the RGBs are removed from the display and the Chip Globals are shown as directly driving the macros and cells. This view makes it easy to determine the load of the Chip Globals, without having to track the load from the Chip Globals to the RGBs and then to the macros and cells.

3.11. Design Elements in Display Options Window (Ask a Question)

The design elements displayed in the Display Options window are family and die-dependent.

4. Floorplanner View Window (Ask a Question)

The **Floorplanner View** window displays all design elements in one window. The selections you make in the views are reflected in the **Floorplanner View**. The color scheme used in the canvas depends on the Layers and Colors you have selected in the **Display Options** window.

Figure 4-1. Floorplanner View

4.1. Operating Modes (Ask a Question)

The Floorplanner View has two modes of operation:

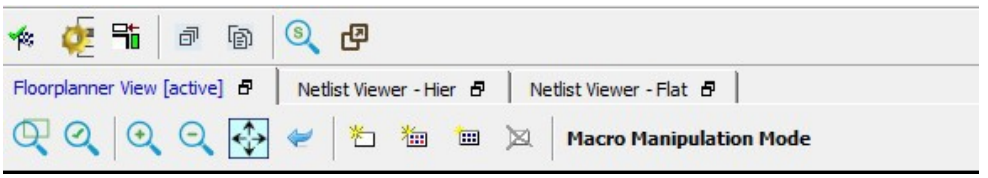
- Macro Manipulation Mode. Use this mode to work with macros, such as assigning macros to location or unassigning placed macros from locations. You can also view properties of selected macros in the Floorplanner View from the properties window. You can select multiple macros from the Floorplanner View by pressing the CTRL key and selecting required macros in the Floorplanner View.
- Region Manipulation Mode. Use this mode to work on regions such as resizing, renaming, or deleting regions, or assigning and unassigning macros or nets to regions.

Click the **Macro Manipulation Mode** or **Region Manipulation Mode** button to switch between modes.

4.2. Floorplanner View Icons (Ask a Question)

The icons available at the top of the Floorplanner View window allow you to zoom in, zoom out, assign I/ O banks, runs DRC checks, and create regions for placement.

Figure 4-2. Floorplanner View Icons

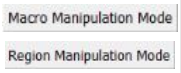


Note: If you have an IOD interface in your design, this icon also appears in the toolbar. The following table lists the functions of each icon.

Table 4-1. Floorplanner View Icons

Icon	Name	Function
	Rubber Band Zoom	Drags out an area to enlarge (zoom) into.
	Rubber Band Select	Zooms into an area. Click in the Floorplanner View and drag the mouse to delineate an area. Release the mouse and all macros inside the delineated area are selected. Works in the Macro Manipulation Mode.
	Zoom In	Zooms in to Floorplanner View.
	Zoom Out	Zooms out of Floorplanner View.
	Zoom to Fit	Zooms to fit the Floorplanner View.
	Zoom to Location	Zooms to a location specified by X-Y coordinates.
	Zoom to fit Selection	Zooms to fit selected macros and ports. When enabled, the view is centered on the selected and placed ports.
	Check Design Rules	Runs the Prelayout Checker, a preliminary check of the netlist for possible Place and Route issues.
	Check DRC Rules for Selected Interfaces	Run the Prelayout Checker for the selected interface, a preliminary check of the netlist for possible Place and Route issues.
	I/O Bank Settings	Sets the I/O bank to specific I/O Technology.
	Auto Assign I/O Bank	Runs the Auto I/O Bank and Globals Assigner. Assigns a voltage to every I/O Bank that does not have a voltage assigned to it and if required, a VREF pin.
	Create Empty	Creates an empty user region.
	Create Inclusive	Creates an inclusive user region.
	Create Exclusive	Creates an exclusive user region.

Table 4-1. Floorplanner View Icons (continued)

Icon	Name	Function
	Delete Region	Deletes the user-created region you selected.
	Use the Macro Manipulation Mode and Region Manipulation Mode buttons	Click the Macro Manipulation Mode and Region Manipulation Mode buttons to switch modes.
	Zoom Floorplanner View To Fit	Zooms to fit the Floorplanner View.
	Expand Floorplanner View To Minimum Zoom	Expands the floorplanner view to make devices visible.
	View Full Screen	Toggle button to view full screen and restore back.

4.3. Netlist Viewer in Floorplanner View Window (Ask a Question)

In addition to the Chip View, the Floorplanner View window displays the netlist views. See Netlist Views for details.

The Floorplanner View and the Netlist View feature different sets of icons specific to their views. There is also a Floorplanner View/Netlist Viewer menu that toggles between Floorplanner View and Netlist View based on the view that is active at the time. See the following figures.

Figure 4-3. Floorplanner Menu and Icons

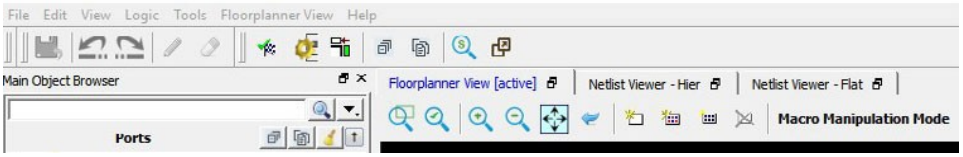
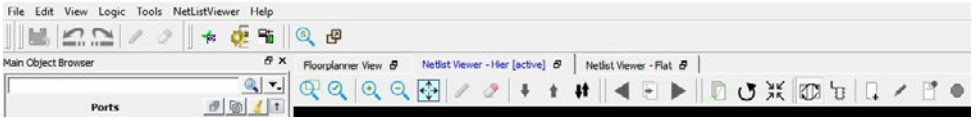


Figure 4-4. Netlist Viewer Menu and Icons

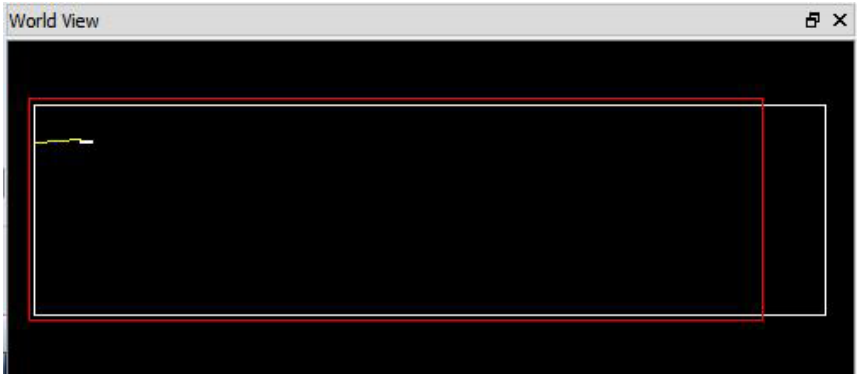


5. Other Chip Planner Windows (Ask a Question)

5.1. World View Window (Ask a Question)

The **World View** shows a red rectangle which reflects what is visible in the Floorplanner View in the context of the Chip. Changing what is visible in the canvas also changes the red rectangle. Changing the size or position of the red rectangle changes what is seen in the Floorplanner View.

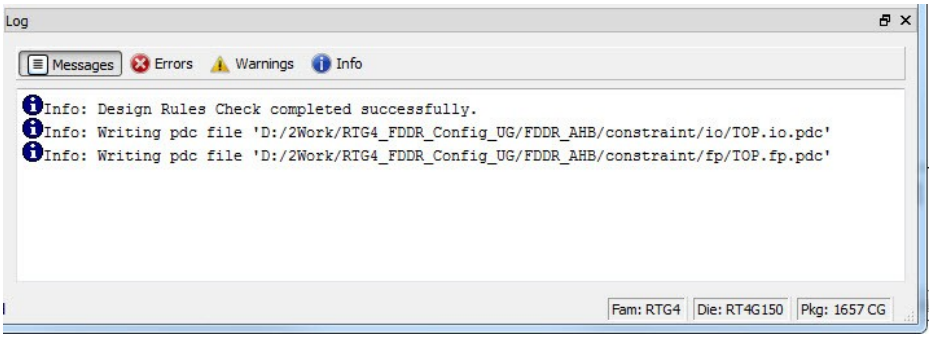
Figure 5-1. World View Window



5.2. Log Window (Ask a Question)

The Log window displays all messages generated by Chip Planner. You can filter the messages according to the type of message: Error, Warning, and Info. If you made and saved changes in Chip Planner, the Log window shows the name and location of the PDC file(s) that were edited to reflect the changes.

Figure 5-2. Log Window



6. Floorplanning Using Chip Planner (Ask a Question)

Floorplanning includes creating regions and making logic assignments to those regions. It is an optional methodology to improve the performance and routability of your design. The objective in floorplanning is to assign logic to specific regions on the chip to enhance performance and routability.

When floorplanning, you analyze your design to see if certain logic can be grouped within regions. Placement regions are especially useful for hierarchical designs with plenty of local connectivity within a block. If your timing analysis indicates several paths with negative slack, try grouping the logic included in these paths into their own regions. This forces the placement of logic within the path closer together and may improve timing performance of the design.

Use floorplanning to create Design Separation Regions for security-critical designs. For Microchip's Design Separation Methodology, all logic should be contained in a logic placement region with dedicated Place and Route resources. For details, see the Design Separation Methodology User Guide.

Use Chip Planner before and after running layout to help you floorplan. You can:

- Create Regions
- Move, resize, merge, or delete regions
- Assign logic to region
- Assign nets to regions

6.1. Types of Regions (Ask a Question)

Three region types can be created for floorplanning purposes:

- Inclusive region
- Exclusive region
- Empty region

6.1.1. Inclusive Region (Ask a Question)

In an inclusive region, the Place and Route tool places unassigned logic within its boundary. It can contain macros, both assigned and unassigned to region. Routing resources within an inclusive region are also not restricted. Logic that is placed prior to region creation is not unplaced from the region.

Use the **Create Inclusive Region** icon  to create an inclusive region.

When a region rectangle is created, you can assign logic macros, net macros, and port macros to it from the Design View window.

Figure 6-1. Inclusive Region Example

6.1.2. Exclusive Region (Ask a Question)

In an exclusive region, the Place and Route tool does not place unassigned logic within its boundary. It can contain only macros already assigned to the region before the region is created. However, routing resources within an exclusive region are not restricted.

Use the **Create Exclusive Region** icon to create an exclusive region: 

When a region rectangle is created, you can assign logic macros, net macros, and port macros to it from the Design View window.

If an exclusive region rectangle is created over placed macros, the locked macros already inside the exclusive region will not be unplaced. They are automatically assigned to the region. If the macro is placed but not locked, the macros will be unplaced from the locations and will not be assigned to the exclusive region.

Figure 6-2. Exclusive Region Example

6.1.3. Empty Region (Ask a Question)

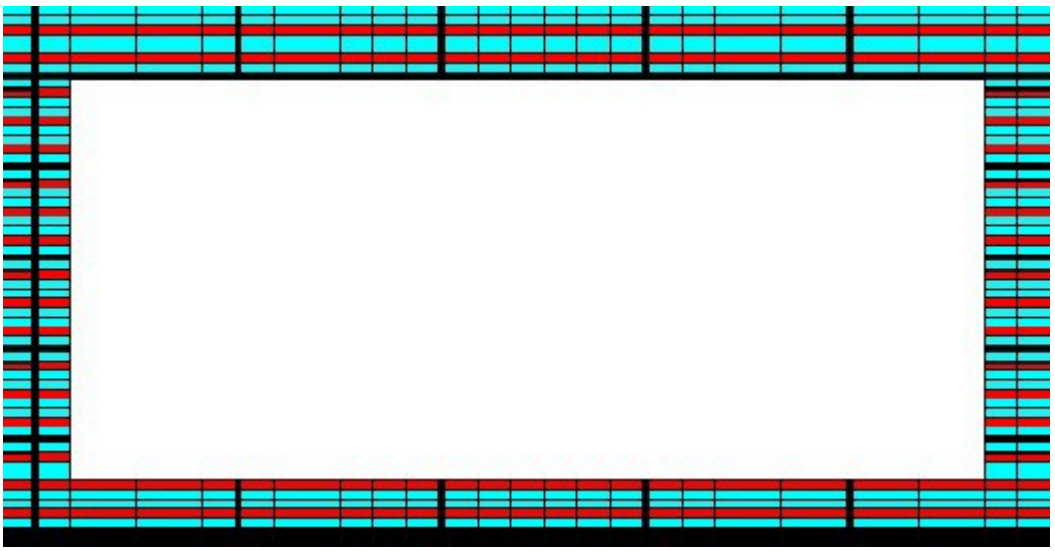
In an empty region, neither the user nor the Place and Route tool can place any logic within its boundary. However, routing resources within an empty region can be used by the Place and Route tool.

Use the **Create Empty Region** icon to create an empty region:

You cannot assign logic macros, net macros, or port macros to an empty region.

If an empty region rectangle is created over placed macros which are not locked, the macros will be unplaced from the locations. The creation of an empty region over locked macros is not allowed.

Figure 6-3. Empty Region Example (PolarFire)



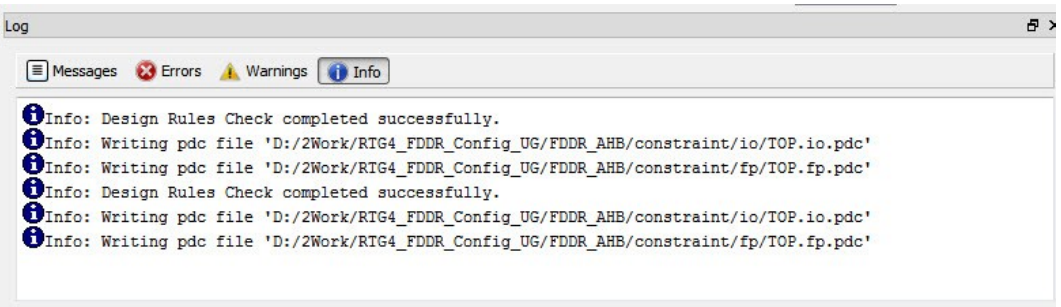
6.2. Creating Rectilinear Regions (Ask a Question)

To create a rectilinear region for floorplanning:

1. Click the region icon: Empty/Inclusive/Exclusive.
2. Go to the Floorplanner View and click at the location where you want to create a region.
3. Drag the mouse diagonally to draw a rectilinear shape for the size of the region you want. The region is named UserRegion1, 2, 3, and so on by default for Inclusive and Exclusive Regions, and EmptyRegion1, 2, 3, and so on by default for Empty Regions.
4. (Optional) Right click and select **Rename** to rename the region from the default name to a different name.
5. Click **Commit** to save the changes.

The Log window prints the message that PDC files are updated/written to reflect the changes you have made in Chip Planner.
Note: If a user region and its boundary fall on top of a cluster boundary, the tool extends the region to include the cluster in the region.

Figure 6-4. Log Window Messages



The `floorplan.pdc` file is updated with the “define_region” PDC command to reflect the new user region you create.

```
define_region -name EmptyRegion3 -type empty -color 2143322112 648 225 659 227
define_region -name UserRegion1 -type inclusive -color 2147442270 552 300 731 311
```

For details about PDC commands, see the PDC Commands User Guide (SmartFusion2, IGLOO2, RTG4 or the PDC Commands User Guide (PolarFire).

The Properties Window displays the properties of the region you created.

6.3. Creating Non-Rectilinear Regions (Ask a Question)

By default, a region is created with a rectangular area. However, you can also create a non-rectilinear region by merging two or more rectangular regions.

Notes:

- Use inclusive or exclusive region constraints if you intend to assign logic to a region. An inclusive region constraint with no macros assigned to it has no effect. An exclusive region constraint with no macros assigned to it is equivalent to an empty region.
- A user region in which there are macros assigned to it is identified by a vertical and horizontal checkered-board pattern:

- A user region without any logic assigned to it is identified by a diagonal hash line pattern:

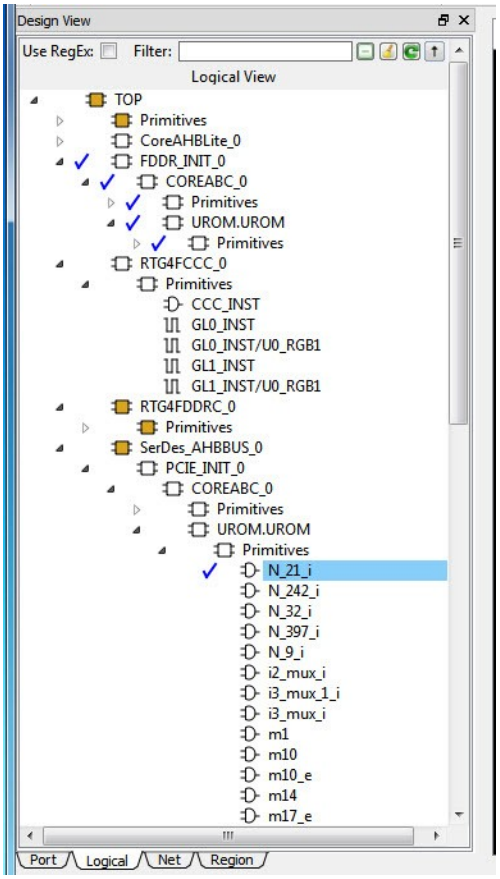
6.4. Assigning Components/Macros to Regions (Ask a Question)

To assign components or macros to a user region:

1. Right click the component or macro in the Logical View and choose **Region Assign**. A dialog box opens for you to select a user region.
2. Click **Commit** to save the changes.

   Alternatively, you can drag-drop the component or macro from the port, Logical View, or net onto a user region in the Floorplanner View.
   The component or macro assigned to the region is identified by a blue check mark:

Figure 6-5. Macro Assigned to a User Region



The Log window prints the message that PDC files are updated/written to reflect the changes you have made in Chip Planner.

The `floorplan.pdc` file is updated with the assign_region PDC command:

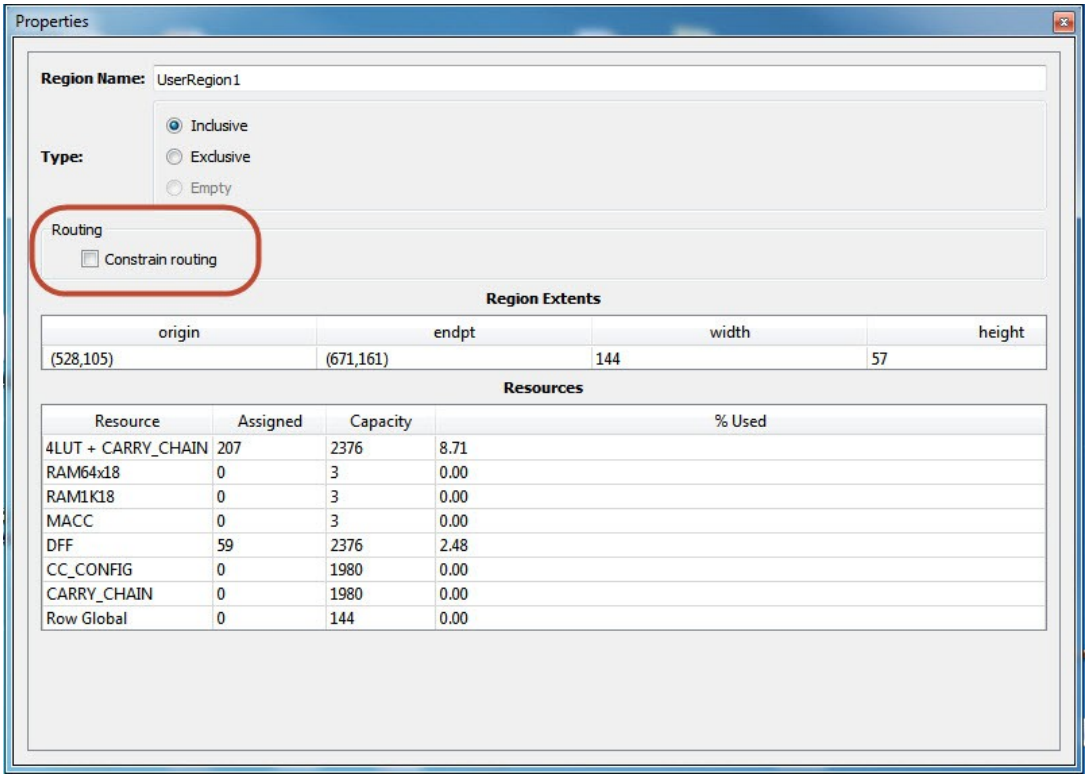
```
define_region -name UserRegion1 -type inclusive -color 2147442270 552 300 731 311
assign_region UserRegion1 FDDR_INIT_0
```

For details about PDC commands, see the PDC Commands User Guide for PolarFire FPGA and the PDC Commands User Guide for SmartFusion2, IGLOO2, and RTG4.

6.5. Routing Inside a Constrained Region (Ask a Question)

By default, when a region is first created, the region properties (Inclusive/Exclusive/Empty) apply to design resources (Placement) only. The Place and Route tool is free to use the routing resources inside the region. To further constrain the Place and Route tool on routing resources usage inside the region, click the **Constrain Routing** check box in the Properties window.

Figure 6-6. Constrain Routing Check Box inside Property Window



6.5.1. Constrain Routing (Ask a Question)

This option applies to all types of regions: inclusive, exclusive, and empty.

When this check box is checked, the region constraints are applied to routing, in addition to placement. The routing behavior is summarized in the following table for each type of user region.

Table 6-1. Routing Behavior Inside User Regions with Constrain Routing Enabled

Region Type	Routing Behavior
Inclusive	• For all nets internal to the region (the source and all destinations belong to the region), routing must be inside the region (that is, such nets cannot be assigned any routing resources that are outside the region or cross the region boundaries). • Nets not internal to the region can use routing resources within the region.
Exclusive	• For all nets internal to the region (the source and all destinations belong to the region), routing must be inside the region (that is, such nets cannot be assigned any routing resources that are outside the region or cross the region boundaries). • Nets without pins inside the region cannot be assigned any routing resources that are outside the region or cross region boundaries).
Empty	• No routing is allowed inside the Empty Region. • However, local clocks and globals can cross empty regions.

6.6. Empty Region General Guidelines (Ask a Question)

Empty regions allow you to create exclusive areas on the device where no logic placement can occur. Empty regions help guide the placer to pack your logic closer together and thereby use more local routing resources to connect it. You cannot create empty regions in areas that contain locked macros. Use the following guidelines for empty regions.

6.6.1. Use Empty Regions to Guide the Place and Route Process (Ask a Question)

If your design does not completely use up your target device (for example, 60% utilization or lower), use empty regions to cluster your logic placement into specific subareas of the chip. This helps when you have originally placed-and-routed the design into a smaller device but want to fit it to a larger part while still preserving the performance you have achieved in the smaller device.

6.6.2. Use Empty Regions to Reduce Routing Congestion (Ask a Question)

Creating empty regions next to the congested area(s) of your design helps reduce congestion. When you place an empty region next to congested logic blocks or regions, the placer cannot place any logic next to your region or logic block. Logic which would normally be placed there is forced to be placed somewhere else. Routing resources next to the congested area are freed up and provide the router more options to route signals into the congested block.

Before deciding to place empty region(s), analyze your design for congestion areas. To analyze the connectivity into and out of your logic blocks or regions, navigate to the **Region** tab and select the logical elements of your design. Create empty regions in these congested areas and see it if improves the routability of your logic.

6.6.3. Use Empty Regions to Reserve Device Resources (Ask a Question)

If you want to preserve the placement of your existing design but plan additional modifications in the future, create empty regions in the areas of the chip where you plan to add additional logic. As you add new logic, remove or resize your empty regions accordingly to fit your new logic. Empty regions placed over I/O pins reserve them for future use as the I/O needs of your design changes. There are some restrictions for using empty regions in this manner.

6.7. Overbooking of Regions (Ask a Question)

Overbooking of regions (assigning resources over 100% utilization) is not allowed. When you try to overbook a region, Chip Planner shows the overbooked resource type in the Properties Window of the Region and the resources are not assigned to the region. The overbooked resource is highlighted in red in the Region Properties window as shown in the following figure.

Figure 6-7. Overbooking of Region

6.8. User Action in Regions in the Floorplanner View (Ask a Question)

When you select a region on the Floorplanner View, you may see some of the following options:

- Rename Regions
- Delete Regions
- Merge Regions

- Unassign macros from Regions
- Assign Macros inside Region
- Clone Region
- Unassign All
- Unassign Selected Nets
- Unassign Selected Components
- Unassign Selected Ports

Floorplanner View has two operating modes:

- Macro Manipulation Mode
- Region Manipulation Mode

In Macro Manipulation Mode, before any region operations (resizing, renaming, deleting, or merging), you must first click the Region Manipulation Mode button to enter the Region Manipulation Mode.

Note: Any side-effects, such as unplacing or unassigning of a macro due to region creation or region resizing, are shown in the Log window.

7. Netlist Views (Ask a Question)

In addition to the chip view for floorplanning purposes, Chip Planner displays a schematic view of the design to make it easier to trace nets and debug the design.

Two netlist types can be displayed in the **Floorplanner View** window:

- Post-Synthesis Hierarchical View (**Netlist Viewer - Hier**)
- Post-compile flattened Netlist View (**Netlist Viewer - Flat**)

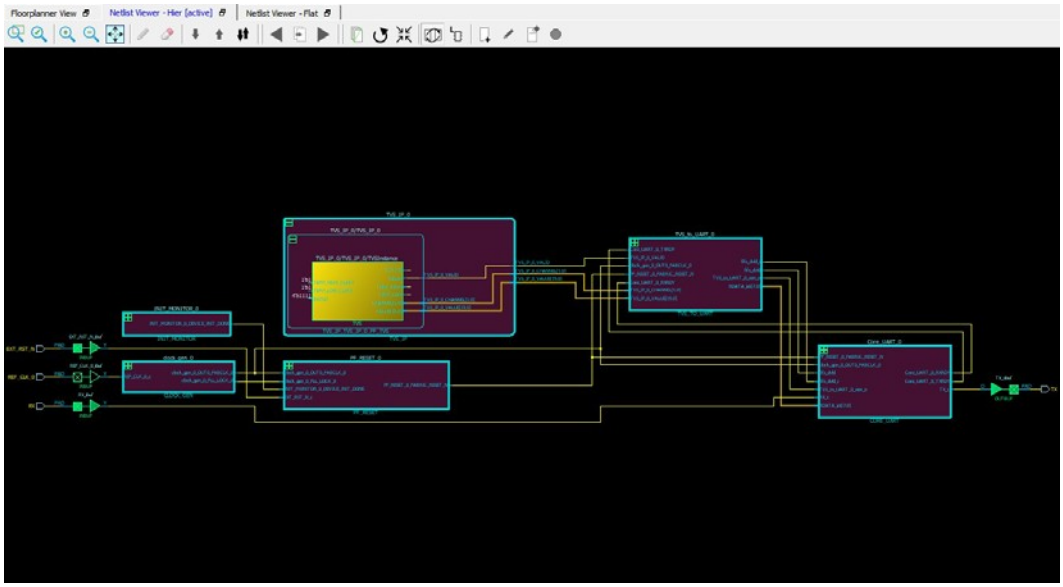
The **Floorplanner View** window and **Netlist Viewer - Hier** and **Netlist Viewer - Flat** tabs are present when Chip Planner is opened.

7.1. Netlist Viewer - Hier (Ask a Question)

The Post-Synthesis Hierarchical View (**Netlist Viewer - Hier**) is a hierarchical view of the netlist after synthesis and after technology mapping to the Microchip FPGA technology. Click the **Hierarchical View** window to display this view. The Chip Planner loads the netlist into the system memory and displays it in this window.

When the netlist loads into memory for the first time, a pop-up progress bar shows the progress of the loading process. Load times may incur a runtime penalty for large netlists.

Figure 7-1. Hierarchical NLV View

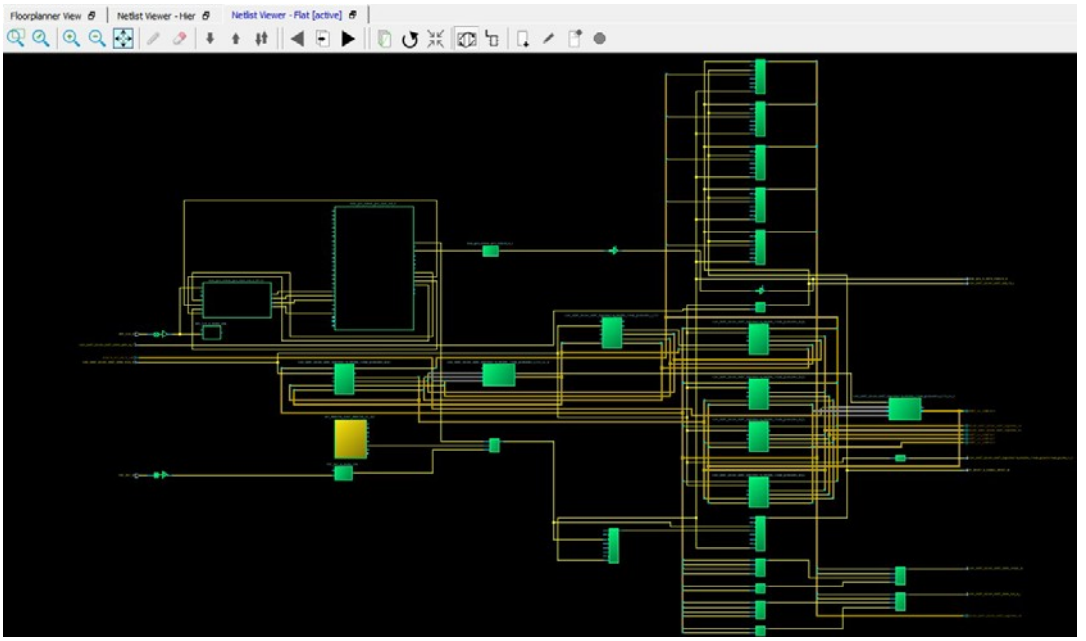


7.2. Netlist Viewer - Flat (Ask a Question)

The **Netlist Viewer - Flat** View is the flattened (non-hierarchical) netlist generated after synthesis, technology mapping, and further optimization based on the DRC rules of the device family and/or die. Click on the Canvas to load the 'Flat' view in the **Netlist Viewer - Flat** window to display this view. The Chip Planner loads the netlist into the system memory and displays it in this window, as shown in the following figure.

When the netlist loads into memory for the first time, a pop-up progress bar shows the progress of the loading process. Load times may incur a runtime penalty for large flattened netlists.

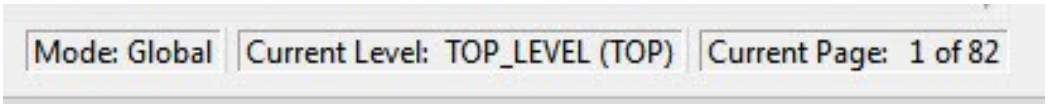
Figure 7-2. Flat NLV - Flattened Netlist



7.3. Display Across Multiple Pages (Ask a Question)

If a hierarchical or flattened netlist spans across multiple pages, the first page is displayed when it opens.

The current page number and the total number of pages are shown in the status bar at the lower right corner of the window.



Status Bar

To go to different pages of the Netlist view, use the left-pointing arrow:

or the right-pointing arrow:

.

7.4. Netlist Viewer Features (Ask a Question)

For information about the Netlist Viewer features, see the Netlist Viewer User Guide.

8. Cross-Probing from SmartTime to Chip View or Netlist Viewer (Ask a Question)

Cross-probing allows you to select a design object in one application and see the selection reflected in another application. When you cross-probe a design object from SmartTime to the Chip View/ Netlist View, you will better understand how the two applications interact with each other.

8.1. Cross-Probing from SmartTime to Chip View (Ask a Question)

With cross-probing, a timing path not meeting timing requirements may be fixed with relative ease when you see the less-than-optimal placement of the design object (in terms of timing requirement) in Chip Planner. Cross-probing from SmartTime to Chip Planner is available for the following design objects:

- Macros
- Ports
- Nets/Paths

Note: Cross-probing of design objects is available from SmartTime to Chip Planner but not vice versa. Before you can cross-probe from SmartTime to Chip Planner, you must:

1. Complete Place and Route on the design.
2. Open both SmartTime and Chip Planner.

8.1.1. Cross-Probing Examples (Ask a Question)

To cross-probe from SmartTime to Chip Planner, a design macro in the SmartTime is used as an example. You can download the example design files from the following location:

www.microchip.com/en-us/products/fpgas-and-plds/documentation

You can download the demo guide from the following location: www.microchip.com/en-us/application-notes/dg0852.html

8.1.1.1. Design Macro Example (Ask a Question)

1. Make sure that the design has successfully completed the Place and Route step.
2. Open SmartTime Maximum/Minimum Analysis view.
3. Open Chip Planner.
4. In the SmartTime Maximum Analysis view, right click the instance ending in data_out[5] in the Timing Path Graph and choose **Show in Chip Planner**. With cross-probing, that macro is selected in Chip Planner's Logical view (zoom in to see the selected item) and highlighted in white in the Floorplanner View. Zoom in to see the selected item. The Properties window in Chip Planner displays the properties of the macro ending in data_out[5].

   Note: The menu item **Show in Chip Planner** is grayed out if Chip Planner is not already open. You may need to zoom in to view the highlighted Q[2] macro in the Floorplanner View.

Figure 8-1. Cross-Probing the Macro Ending in data_out[5] in SmartTime View

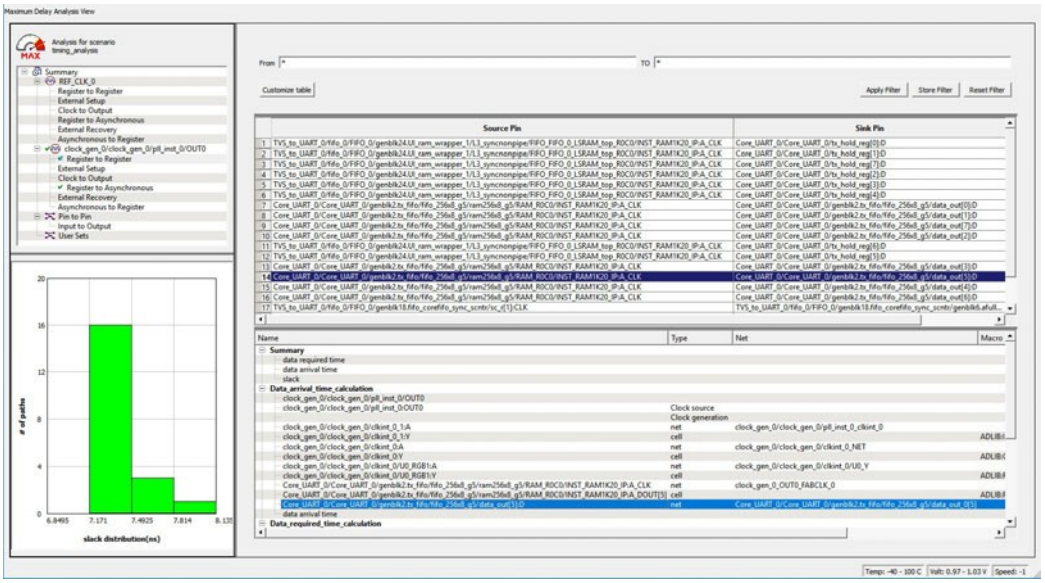
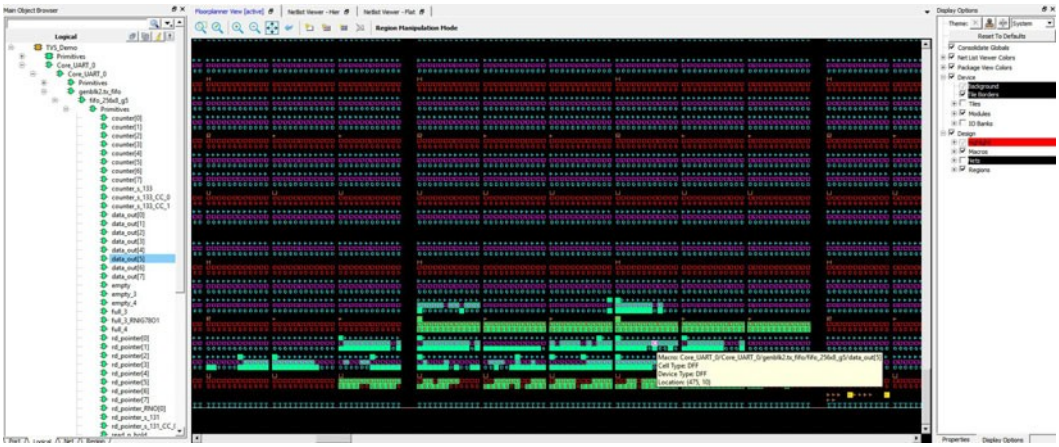


Figure 8-2. Cross-Probing the Macro Ending in data_out[5] in Floorplanner View



8.1.1.2. Timing Path Example (Ask a Question)

1. Make sure the design completed the Place and Route step successfully.
2. Open SmartTime Maximum/Minimum Analysis view.
3. Open Chip Planner.
4. In the SmartTime Maximum/Minimum Analysis view, right click the macro **Core_UART_0/Core_UART_0/tx_hold_reg[5]** in the table and choose **Show Path in Chip Planner**. There will be a net going from the macro ending in tx_hold_reg[5] to the other macros such as PF_RESET_0, RAM1K20 and RAM_R0C0 and local level global clock.

   Note: If Chip Planner is not already open, the menu item in **Show Path in Chip Planner** is grayed out.

Figure 8-3. Cross-Probing - Timing Path (SmartTime View)

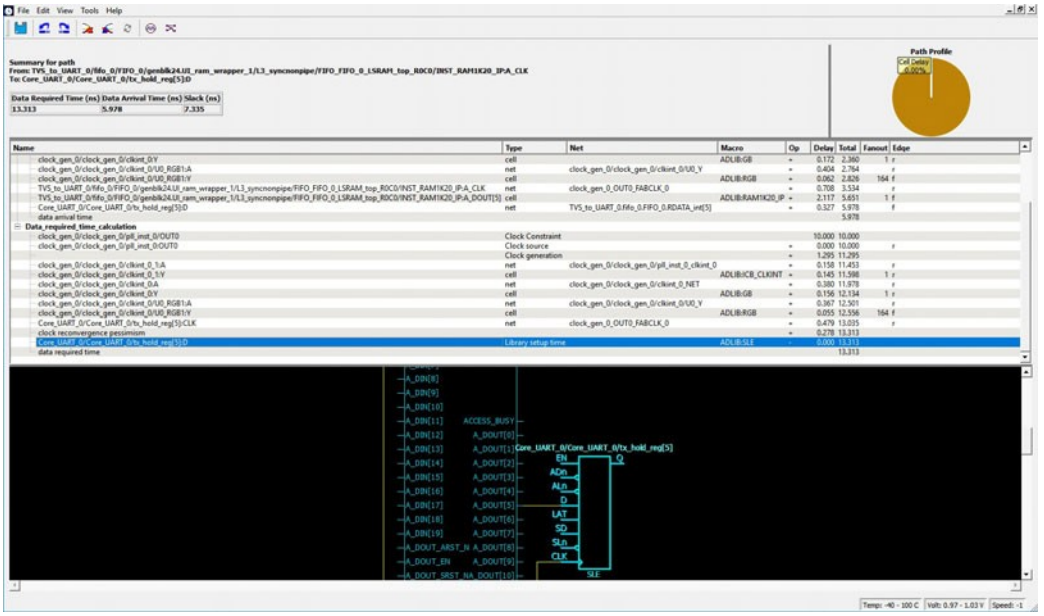
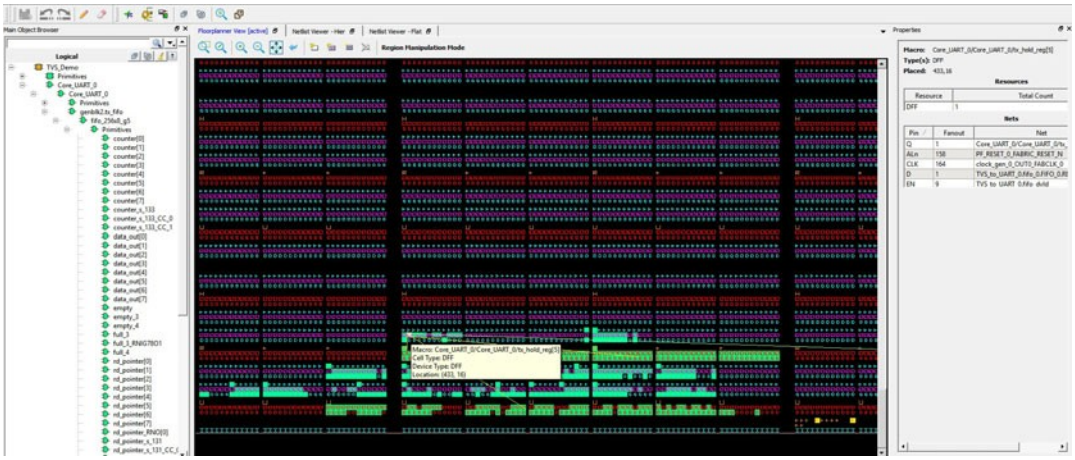


Figure 8-4. Cross-Probing - Timing Path (Floorplanner View)



8.1.1.3. Port Example (Ask a Question)

1. Make sure the design completed the Place and Route step successfully.
2. Open the SmartTime Maximum/Minimum Analysis view.
3. Open Chip Planner.
4. In the SmartTime Maximum/Minimum Analysis view, right click the port **TX** in the Path and choose **Show in Chip Planner**. Note that the port “TX” is selected and highlighted in Chip Planner's Port view.

Note: If Chip Planner is not already open, the menu item Show in Chip Planner is grayed out.

Figure 8-5. Cross-Probing - Port (SmartTime View)

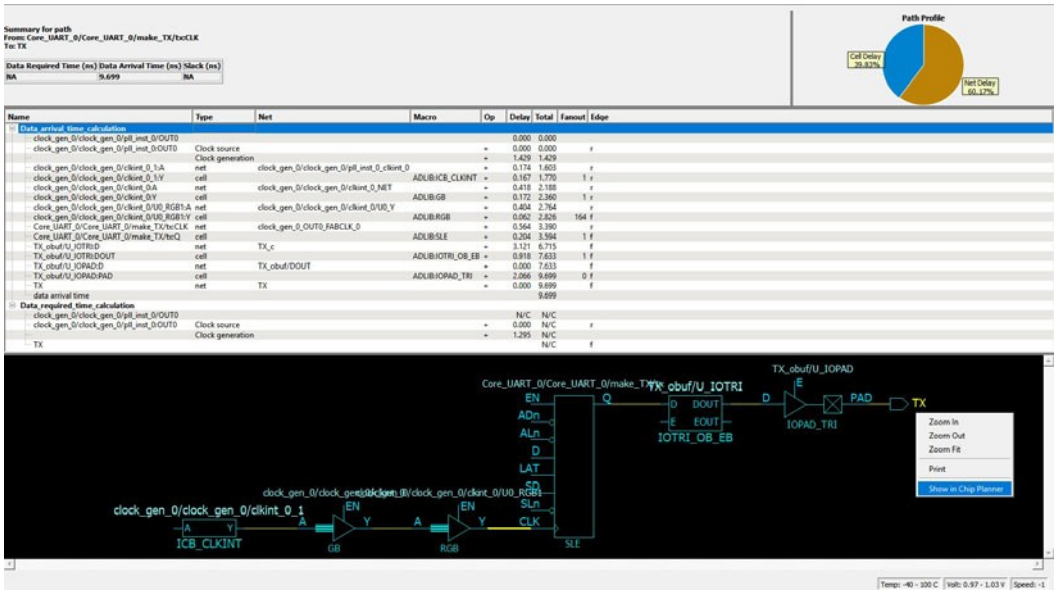
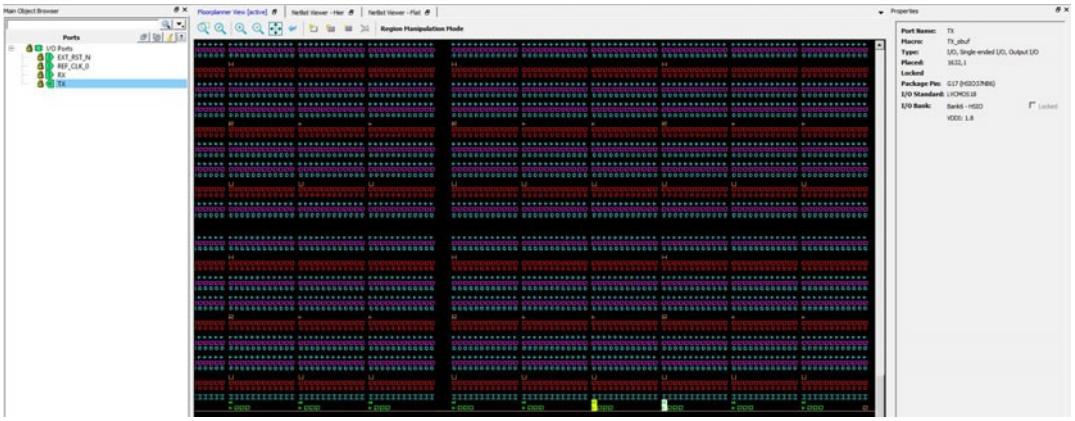


Figure 8-6. Cross-Probing - Port (Floorplanner View)



From the Properties View inside Chip Planner, you will find the following information about the Port “CLK” you are cross-probing:

- Port Type
- Port Placement Location (X-Y Coordinates)
- I/O Bank Number
- I/O Standard
- Pin Assignment

8.2. Cross-Probing from SmartTime to Netlist Viewer (Ask a Question)

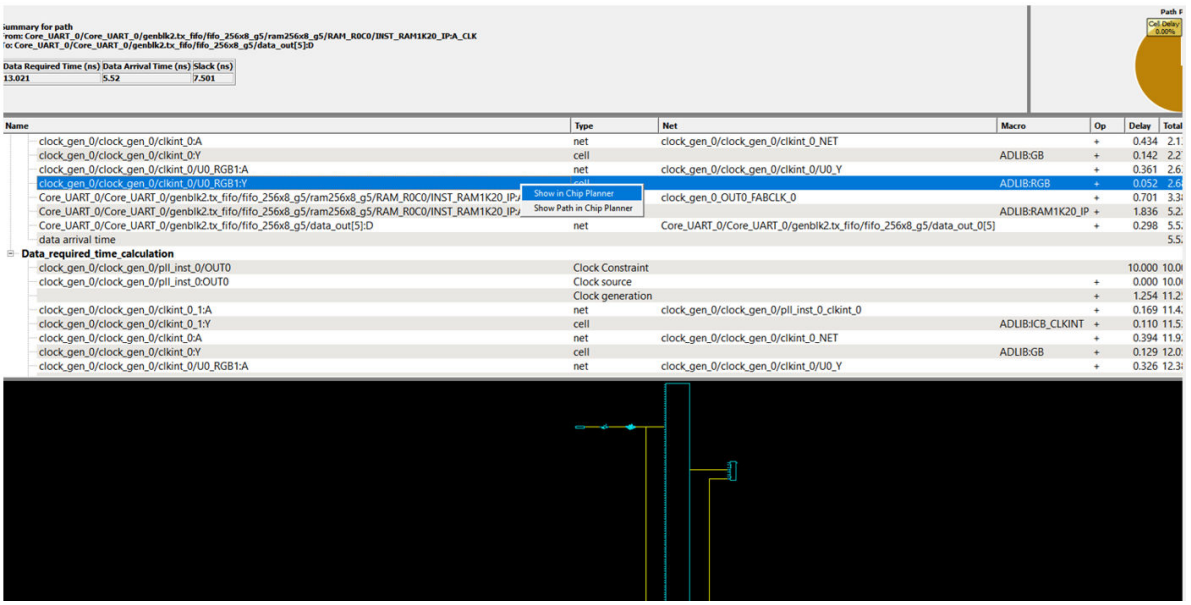
Cross-probing from SmartTime to Netlist Viewer allows you to examine and debug timing-critical paths as the first step toward timing closure. Timing paths with setup or hold time violations can be selected and cross-probed from SmartTime to Netlist Viewer to examine how the net is routed. Cross-probing can also reveal and identify routing congestion.

To cross-probe from SmartTime to Netlist Viewer, perform the following steps:

1. In Libero, complete the Place and Route step.

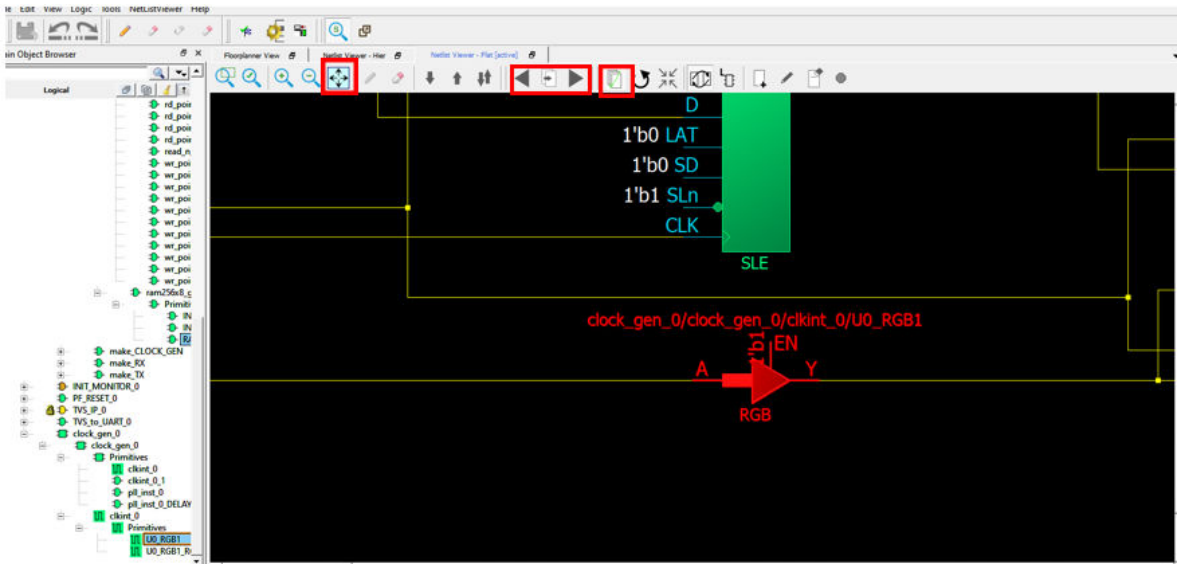
2. Invoke the Chip Planner.
3. In Chip Planner, select **Netlist Viewer - Flat**.
4. In the toolbar, turn on the zoom and center option:  .
5. In the Design Flow window, open SmartTime.
6. Open the Maximum/Minimum Delay Analysis view.
7. To open the Timing Path display in SmartTime, click on a timing path.
8. Right-click a cell in the timing path display or a timing path in the SmartTime table and select **Show in Chip Planner**.

Figure 8-7. Cross-Probe a Cell from SmartTime to Netlist Viewer



Netlist Viewer shows the selected item and highlights it.

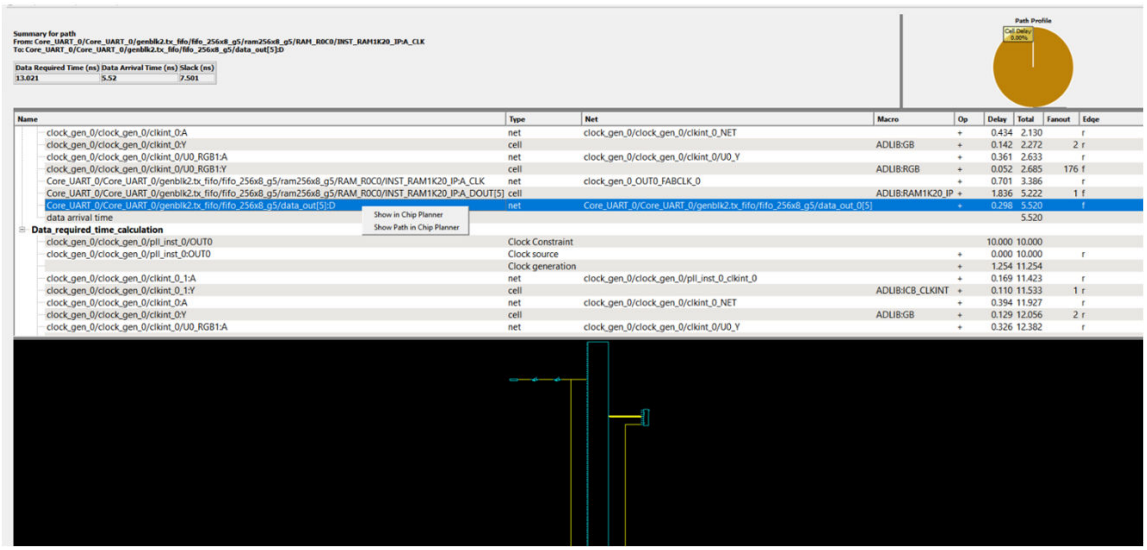
Figure 8-8. Cross-Probed Cell in Netlist Viewer View



Tip: Each time you click **Show In Chip Planner** action, the selected object is added to the list of objects previously selected on the Netlist Viewer canvas. To view all selected objects, click **Zoom to Fit** on the **Netlist Viewer** toolbar. In some cases, selected objects may be located on different pages of the canvas. To navigate between these pages, use the **Previous Page** and **Next Page** buttons. To view all selected objects on a single page, disable **Page Splitting**.

9. To view the objects in the path of the net, right-click a net in the timing path in the SmartTime table and select **Show Path in Chip Planner**.

Figure 8-9. Cross-Probe a Net from SmartTime to Netlist Viewer

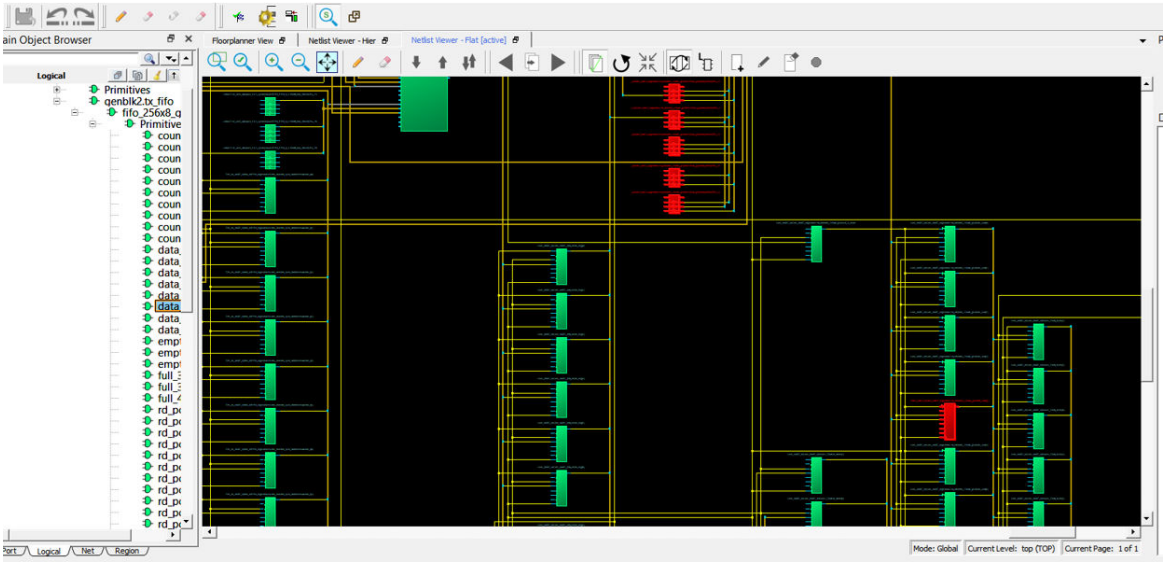


Attention: Cross-probing a net from the timing path display to Netlist Viewer is not supported.

Tip: You might want to **Disable Page Splitting** settings and click on **Zoom to Fit** to view all the selected items.

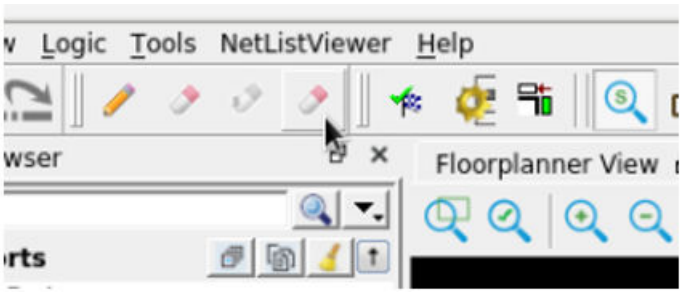
Netlist Viewer shows the objects in the selected net path and highlights them.

Figure 8-10. Cross-Probed Cell in the Path of the Net in Netlist Viewer View



10. If desirable, add the highlighted objects of interest in the Netlist view to a cone view, and add Drivers or Loads to the active cone view for debugging.

    To clear all cross-probe objects and paths, click **Clear Cross Probe** from the top toolbar of the window.



9. A - Limitations (Ask a Question)

This appendix lists Chip Planner limitations.

9.1. I/O Register Support (Ask a Question)

Every I/O has several embedded registers that you can use for faster clock-to-out timing, and to meet external hold and setup timing requirements. This feature uses input, output, or enable registers available in the I/O block.

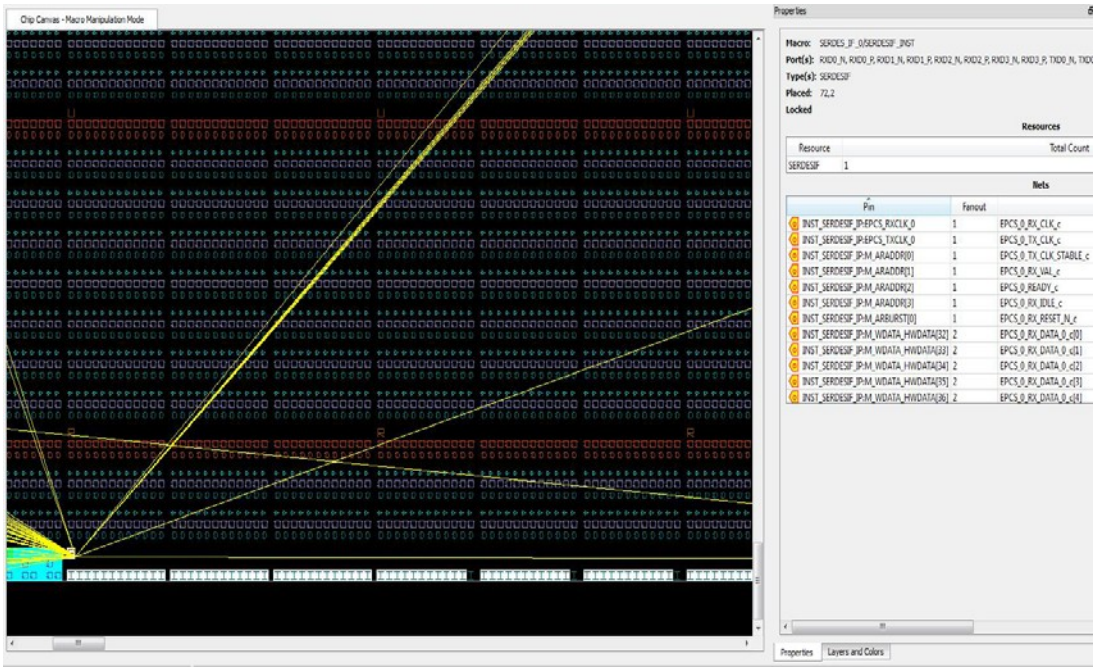
However, a register (if combined with an I/O register) is not shown in the Logical view as a separate element and is shown as part of a port.

Figure 9-1. Register Combined with Input Register of an I/O

9.2. Internal Elements of External IP Macros Displayed in a Single Connection (Ask a Question)

Some external IP, such as SerDes and FDDR, spans across multiple clusters and has its own dedicated ports. However, the net connected to these macro I/Os are shown to be connected from a single location. The following figure is an example of a SerDes macro that shows all the associated nets connected to a single macro.

Figure 9-2. SerDes Macro with Associated Nets in a Single Connection



9.2.1. Cross-Probing into SmartTime Not Supported (Ask a Question)

Cross-probing from the Chip View /Netlist View into SmartTime is not supported. Cross-probing is supported for SmartTime to Chip View and Netlist View, but not from Chip View or Netlist View to SmartTime.

10. Revision History (Ask a Question)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
N	12/2025	This document is released with Libero SoC Design Suite v2025.2 without changes from v2025.1.
M	05/2025	The following changes are made in this revision: • Deleted “Ratsnest view” from the fourth bullet in the Introduction section. • Updated the section Cross-Probing from SmartTime to Netlist Viewer.
L	08/2024	This document is released with Libero SoC Design Suite v2024.2 without changes from v2024.1.
K	02/2024	This document is released with Libero SoC Design Suite v2024.1 without changes from v2023.2.
J	08/2023	This document is released with Libero SoC Design Suite v2023.2 without changes from v2023.1.
H	04/2023	This document is released with Libero SoC Design Suite v2023.1 without changes from v2022.3.
G	12/2022	This document is released with Libero SoC Design Suite v2022.3 without changes from v2022.2.
F	08/2022	This document is released with Libero SoC Design Suite v2022.2 without changes from v2022.1.
E	04/2022	This document is released with Libero SoC Design Suite v2022.1 without changes from v2021.3.
D	12/2021	This document is released with Libero SoC Design Suite v2021.3 without changes from v2021.2.
C	08/2021	This document is released with Libero SoC Design Suite v2021.2 without changes from v2021.1.
B	04/2021	The following changes are made in this revision: • Highlighting: updated tools, Object Browser Tree, and design settings. Also, added a note about the net color in the Net view not being consistent with that of the Planner. • Changing an Option Color: updated options from the right click menu. • Displaying Routing Views: added this new topic. • Cross Probing: described how to change a cross probing color to transparent and how to clear a cross probe state.
A	11/2020	Document converted to Microchip template. Initial Revision.

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