
SmartFusion2

Dual-Port Large SRAM Configuration



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Introduction

A Dual-Port Large SRAM enables read and write access on both ports (Figure 1).

The core configurator automatically cascades Large SRAM blocks to create wider and deeper memories by choosing the most efficient aspect ratio. It also handles the grounding of unused bits. The core configurator supports the generation of memories that have different aspect ratios on each port.

Dual-Port Large SRAM is synchronous for memory write and read operations, setting up the addresses as well as writing and reading the data. The memory write and read operations will be triggered at the rising edge of the clock.

Optional pipeline registers are available at both the read data ports to improve the clock-to-out delay.

A feed-through write mode is also available to enable immediate access to the write data.

In this document, we describe how you can configure a Dual-Port Large SRAM instance and define how the signals are connected. For more details about the Dual-Port Large SRAM, please refer to the [SmartFusion2 User's Guide](#).

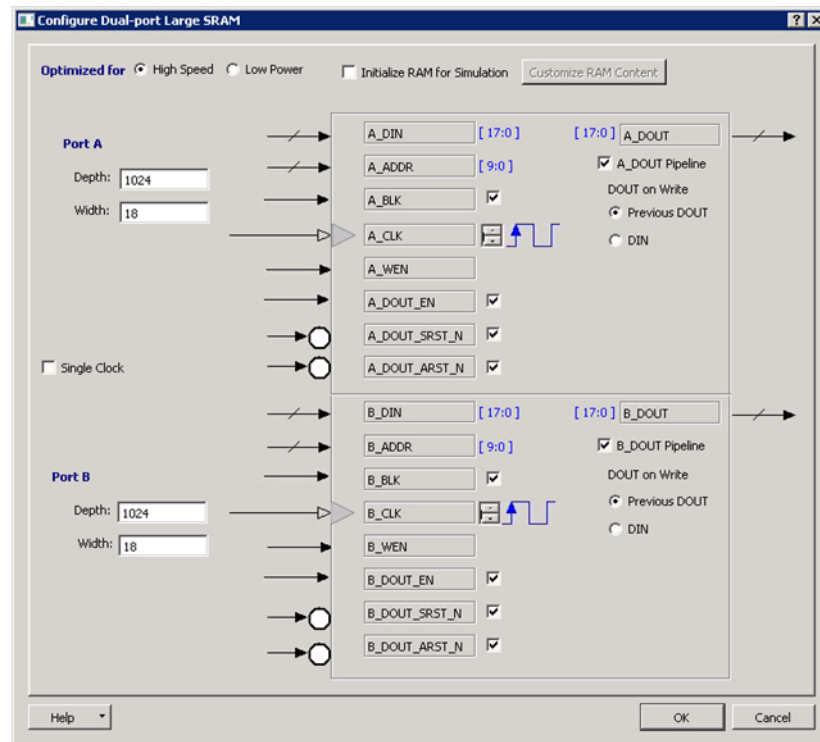


Figure 1 • Dual-Port Large SRAM Configurator

1 – Functionality

Optimization for High Speed or Low Power

Selecting High Speed results in a macro optimized for speed and area (width cascading).

Selecting Low Power results in a macro optimized for low power, but uses additional logic at the input and output (depth cascading). Performance for a low power optimized macro may be inferior to that of a macro optimized for speed.

Port A Depth/Width and Port B Depth/Width

The depth range for each port is 1-524288. The width range for each port is 1-1242.

The two ports can be independently configured for any depth and width. (Port A Depth * Port A Width) must equal (Port B Depth * Port B Width).

Single Clock (CLK) or Independent Port A and B Clocks (A_CLK, B_CLK)

The default configuration for Dual-Port Large SRAM is a Single clock (CLK) to drive both A and B ports with the same clock. Uncheck the Single clock checkbox to drive independent clocks - one for each port (A_CLK and B_CLK).

Click the waveform next to any of the clock signals to toggle its active edge.

Block Select (A_BLK, B_BLK) and Read/Write Control (A_WEN, B_WEN)

De-asserting A_BLK forces A_DOUT to zero. De-asserting B_BLK forces B_DOUT to zero.

Asserting A_BLK when A_WEN is low reads the RAM at the address A_ADDR onto the input of the A_DOUT register, on the next rising edge of A_CLK.

Asserting A_BLK when A_WEN is high writes the data A_DIN into the RAM at the address A_ADDR, on the next rising edge of A_CLK.

Asserting B_BLK when B_WEN is low, reads the RAM at the address B_ADDR onto the input of the B_DOUT register, on the next rising edge of B_CLK.

Asserting B_BLK when B_WEN is high, writes the data B_DIN into the RAM at the address B_ADDR, on the next edge of B_CLK.

The default configuration for A_BLK and B_BLK is unchecked, which ties the signal to the active state and removes it from the generated macro. Click the respective checkbox to insert that signal on the generated macro. Click the signal arrow (when available) to toggle its polarity.

Pipeline for Read Data Output of Port A and B

Click the Pipeline checkbox to enable pipelining of Read data (A_DOUT or B_DOUT). This is a static selection and cannot be changed dynamically by driving it with a signal.

Turning off pipelining of Read data of a port also disables the configuration options of the respective DOUT_EN, DOUT_SRST_N and DOUT_ARST_N signals.

DOUT on Write for Read Data Output of Port A and B

The default data on the Read Data output (A_DOUT or B_DOUT) during a write cycle is the DOUT data from the previous cycle. Click the DIN radio button to enable feed-through write mode on Read data output. This is a static selection and cannot be changed dynamically by driving it with a signal.

Register Enable (A_DOUT_EN and B_DOUT_EN)

The pipeline registers for ports A and B have active high, enable inputs. The default configuration is to tie these signals to the active state and remove them from the generated macro. Click each signal's checkbox to insert that signal on the generated macro.

Click the signal arrow (when available) to toggle its polarity.

Synchronous Reset (A_DOUT_SRST_N and B_DOUT_SRST_N)

The pipeline registers for ports A and B have active low, synchronous reset inputs. The default configuration is to tie these signals to the inactive state and remove them from the generated macro. Click each signal's checkbox to insert that signal on the generated macro.

Click the signal arrow (when available) to toggle its polarity.

Asynchronous Reset (A_DOUT_ARST_N and B_DOUT_ARST_N)

The pipeline registers for ports A and B have active low, asynchronous reset inputs. The default configuration is to tie these signals to the inactive state and remove them from the generated macro. Click each signal's checkbox to insert that signal on the generated macro.

Click the signal arrow (when available) to toggle its polarity.

DOUT Register Truth Table

Table 1-1 describes the functionality of the control signals on the A_DOUT and B_DOUT registers.

Table 1-1 • A_DOUT and B_DOUT Registers Truth Table

_ARST_N	Pipeline	_CLK	_EN	_SRST_N	d	q
0	x	x	x	x	x	0
1	T	Not rising	x	x	x	q
1	T	Rising	0	x	x	q
1	T	Rising	1	0	x	0
1	T	Rising	1	1	x	d
1	F	x	0	x	x	q
1	F	x	1	0	x	0
1	F	x	1	1	x	d

2 – Implementation Rules

Caveats for Dual-Port Large SRAM generation

- If a word width of 9 or 18 is used for one port, then the width of the other port cannot be 1, 2, or 4. Configurations that do not use the 9th bit (e.g., Port A width of 8192x4 and Port B width of 1024x32) are supported.
- The core configurator only supports depth cascading up to 32 blocks.
- The core configurator does not generate RAM based on a specific device. Refer to the [datasheet](#) to check for the available RAM1Kx18 modules in the device.
- The software returns a configuration error for unsupported configurations.

Note

- All unused inputs must be grounded.
- DOUT on Write selection is ignored during read operation.
- Writing different data to the same address using both ports in Dual-Port Large SRAM is undefined and should be avoided.
- Writing to and reading from the same address is undefined and should be avoided. There is no collision prevention or detection.
- Read from both ports at the same location is allowed.

3 – RAM Content Manager

The RAM Content Manager enables you to specify the contents of your memory so that you can avoid the simulation cycles required for initializing the memory, which reduces simulation runtime.

The RAM core generator takes away much of the complexity required in the generation of large memory that utilize one or more RAM blocks on the device. The configurator uses one or more memory blocks to generate a RAM matching your configuration. In addition, it also creates the surrounding cascading logic.

The configurator cascades RAM blocks in three different ways.

- Cascaded deep (e.g. 2 blocks of 16384x1 to create a 32768x1)
- Cascaded wide (e.g. 2 blocks of 16384x1 to create a 16384x2)
- Cascaded wide and deep (e.g. 4 blocks of 16384x1 to create a 32768x2, in a 2 blocks width-wise by 2 blocks depth-wise configuration)

Specify memory content in terms of your total memory size. The configurator must partition your memory file appropriately such that the right content goes to the right block RAM when multiple blocks are cascaded.

Supported Formats

The Microsemi implementation of these formats interprets data sets in bytes. This means that if the memory width is 7 bits, every 8th bit in the data set is ignored. Or, if the data width is 9, two bytes are assigned to each memory address and the upper 7 bits of each 2-byte pair are ignored.

The following examples illustrate how the data is interpreted for various word sizes:

For the given data: FF 11 EE 22 DD 33 CC 44 BB 55 (where 55 is the MSB and FF is the LSB)

For 32-bit word size:

```
0x22EE11FF (address 0)
0x44CC33DD (address 1)
0x000055BB (address 2)
```

For 16-bit word size:

```
0x11FF (address 0)
0x22EE (address 1)
0x33DD (address 2)
0x44CC (address 3)
0x55BB (address 4)
```

For 8-bit word size:

```
0xFF (address 0)
0x11 (address 1)
0xEE (address 2)
0x22 (address 3)
0xDD (address 4)
0x33 (address 5)
0xCC (address 6)
0x44 (address 7)
0xBB (address 8)
0x55 (address 9)
```

For 9-bit word size:

```
0x11FF -> 0x01FF (address 0)
0x22EE -> 0x00EE (address 1)
0x33DD -> 0x01DD (address 2)
0x44CC -> 0x00CC (address 3)
0x55BB -> 0x01BB (address 4)
```

Notice that for 9-bit, that the upper 7-bits of the 2-bytes are ignored.

INTEL-HEX

Industry standard file. Extensions are HEX and IHX. For example, file2.hex or file3.ihx.

A standard format created by Intel. Memory contents are stored in ASCII files using hexadecimal characters. Each file contains a series of records (lines of text) delimited by new line, '\n', characters and each record starts with a ':' character. For more information regarding this format, refer to the Intel-Hex Record Format Specification document available on the web (search Intel Hexadecimal Object File for several examples).

The Intel Hex Record is composed of five fields and arranged as follows:

```
:11aaaaatt[dd...]cc
```

Where:

- : is the start code of every Intel Hex record
- ll is the byte count of the data field
- aaaa is the 16-bit address of the beginning of the memory position for the data. Address is big endian.
- tt is record type, defines the data field:
 - 00 data record
 - 01 end of file record
 - 02 extended segment address record
 - 03 start segment address record (ignored by Microsemi SoC tools)
 - 04 extended linear address record
 - 05 start linear address record (ignored by Microsemi SoC tools)
- [dd...] is a sequence of n bytes of the data; n is equivalent to what was specified in the ll field
- cc is a checksum of count, address, and data

Example Intel Hex Record:

```
:0300300002337A1E
```

MOTOROLA S-record

Industry standard file. File extension is S, such as file4.s

This format uses ASCII files, hex characters, and records to specify memory content in much the same way that Intel-Hex does. Refer to the Motorola S-record description document for more information on this format (search Motorola S-record description for several examples). The RAM Content Manager uses only the S1 through S3 record types; the others are ignored.

The major difference between Intel-Hex and Motorola S-record is the record formats, and some extra error checking features that are incorporated into Motorola S.

In both formats, memory content is specified by providing a starting address and a data set. The upper bits of the data set are loaded into the starting address and leftovers overflow into the adjacent addresses until the entire data set has been used.

The Motorola S-record is composed of 6 fields and arranged as follows:

```
S t l l a a a a [ d d . . . ] c c
```

Where:

- S is the start code of every Motorola S-record
- t is record type, defines the data field
- ll is the byte count of the data field
- aaaa is a 16-bit address of the beginning of the memory position for the data. Address is big endian.

- [dd...] is a sequence of n bytes of the data; n is equivalent to what was specified in the ll field
- cc is the checksum of count, address, and data

Example Motorola S-Record:

S10a0000112233445566778899FFFA

RAM Content Manager Functionality

To open the RAM Content Manager, after specifying your RAM configurations (set your Read and Write Depth and Width), select the **Initialize RAM for Simulation** checkbox, and then click **Customize RAM Content**. The RAM Content Manager appears (Figure 3-1).

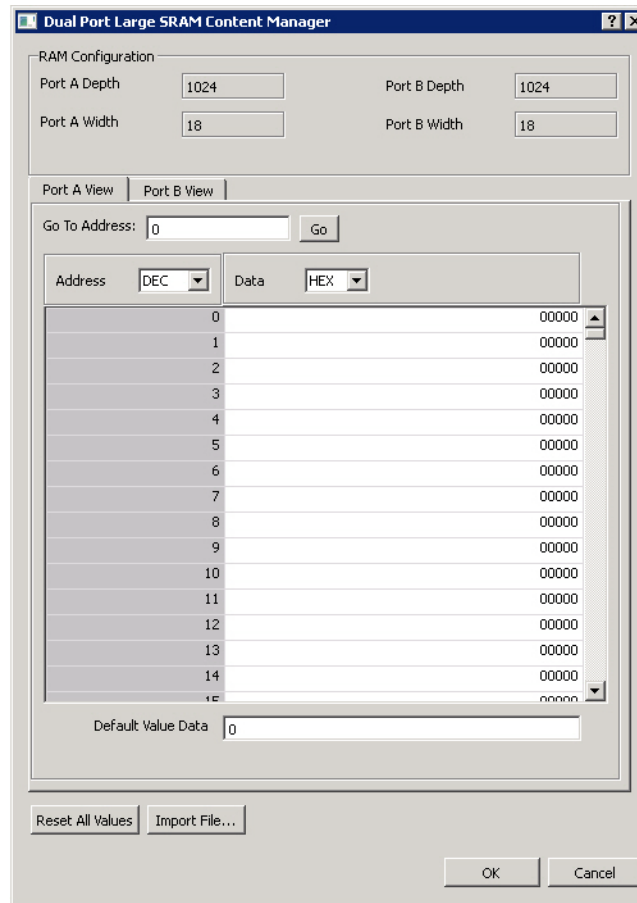


Figure 3-1 • Customize RAM Content for Simulation

RAM Configuration

Write Depth and Write Width - As specified in the RAM core generator dialog box (not editable).

Read Depth and Read Width - As specified in the RAM core generator dialog box (not editable).

Write Port View / Read Port View

Go To Address - Enables you to go to a specific address in the manager. Each memory block has many addresses; it is often difficult to scroll through and find a specific one. This task is simplified by enabling you to type in a specific address. The number display format (Hex, Bin, Dec) is controlled by the value you set in the drop-down menu above the Address column.

Address - The Address column lists the address of a memory location. The drop-down menu specifies the number format for your address list (hexadecimal, binary, or decimal).

Data - Enables you to control the data format and data value in the manager. Click the value to change it. Note that the dialogs show all data with the MSB down to LSB. For example, if the row showed 0xAABB for a 16-bit word size, the AA would be the MSB and BB would be LSB.

Default Data Value - The value given to memory addresses that have not been explicitly initialized (by importing content or editing manually). When changed, all default values in the manager are updated to match the new value. The number display format (Hex, Bin, Dec) is controlled by the value you set in the drop-down menu above the Data column.

Reset All Values - Resets the Data values.

Import File - Opens the Import Memory Content dialog box; enables you to select a memory content file (Intel-Hex) to load. File extensions are set to *.hex for Intel-Hex files during import.

OK - Closes the manager and saves all the changes made to the memory and its contents.

Cancel - Closes the manager, cancels all your changes in this instance of the manager, and returns the memory back to the state it held before the manager was opened.

MEMFILE (RAM Content Manager output file)

Transfer of RAM data (from the RAM Content Manager) to test equipment is accomplished via MEM files. The contents of your RAM is first organized into the logical layer and then reorganized to fit the hardware layer. Then it is stored in MEM files that are read by other systems and used for testing.

The MEM files are named according to the logical structure of RAM elements created by the configurator. In this scheme the highest order RAM blocks are named CORE_R0C0.mem, where "R" stands for row and "C" stands for column. For multiple RAM blocks, the naming continues with CORE_R0C1, CORE_R0C2, CORE_R1C0, etc.

The data intended for the RAM is stored as ASCII 1s and 0s within the file. Each memory address occupies one line. Words from logical layer blocks are concatenated or split in order to make them fit efficiently within the hardware blocks. If the logical layer width is less than the hardware layer, two or more logical layer words are concatenated to form one hardware layer word. In this case, the lowest bits of the hardware word are made up of the lower address data bits from the logical layer. If the logical layer width is more than the hardware layer, the words are split, placing the lower bits in lower addresses.

If the logical layer words do not fit cleanly into the hardware layer words, the most significant bit of the hardware layer words is not used and defaulted to zero. This is also done when the logical layer width is 1 in order to avoid having left over memory at the end of the hardware block.

4 – Port Description

Table 4-1 lists the Dual-Port Large SRAM signals in the generated macro.

Table 4-1 • Dual-Port Large SRAM Signals

Port	Direction	Polarity	Description
CLK	In	Rising edge	Single clock signal that drives all three ports with the same clock
A_DIN[]	In		Port A Write data
A_ADDR[]	In		Port A Read address
A_BLK	In	Active high	Port A Enable
A_CLK	In	Rising edge	Port A clock
A_WEN	In		Port A signal to switch between Read and Write modes: Low = Read; High = Write
A_DOUT[]	Out		Port A Read data
A_DOUT_EN	In	Active High	Port A Read data register Enable
A_DOUT_SRST_N	In	Active Low	Port A Read data register Synchronous reset
A_DOUT_ARST_N	In	Active Low	Port A Read data register Asynchronous reset
B_DIN[]	In		Port B Write data
B_ADDR[]	In		Port B address
B_BLK	In	Active High	Port B Enable
B_CLK	In	Rising edge	Port B clock
B_WEN	In		Port signal to switch between Read and Write modes: Low = Read; High = Write
B_DOUT[]	Out		Port B Read data
B_DOUT_EN	In	Active High	Port B Read data register Enable
B_DOUT_SRST_N	In	Active Low	Port B Read data register Synchronous reset
B_DOUT_ARST_N	iN	Active Low	Port B Read data register Asynchronous reset

5 – Parameters

Table 5-1 lists the Dual-Port Large SRAM parameters in the generated macro.

Table 5-1 • Dual-Port Large SRAM Parameters

GENFILE Parameter	Configurator Parameter	Valid Range	Default	Description
DESIGN				Name of the generated macro
FAM		SmartFusion2		Target family
OUTFORMAT		Verilog, VHDL		Netlist format
LPMTYPE		LPM_RAM		Macro category
DEVICE		500 - 5000	5000	Target device
PTYPE	PTYPE	2	2	2: Dual-port
INIT_RAM	INIT_RAM	F, T	F	Initialize RAM for simulation
CASCADE	CASCADE	0, 1	0	0: Cascading for WIDTH or Speed 1: Cascading for DEPTH or Power
CLKS	CLKS	1, 2	1	1: Single Read/Write Clock 2 : Independent Read and Write Clocks
WCLK_EDGE	CLK_EDGE	CLS=1 RISE, FALL	RISE	RISE: Rising edge Single clock FALL: Falling edge Single clock
WWIDTH	A_WIDTH	1-1242	18	Port A data width
WDEPTH	A_DEPTH	1-524288	1024	Port A address depth
RWIDTH	B_WIDTH	1-1242	18	Port B data width
RDEPTH	B_DEPTH	1- 524288	1024	Port B address depth
WE_POLARITY	A_BLK_POLARITY	0, 1, 2	2	0: Active-low Port A enable 1: Active-high Port A enable 2: Port A enable tied off to be always active
WCLK_EDGE	A_CLK_EDGE	CLKS=2 RISE, FALL	RISE	RISE: Rising edge Port A clock FALL: Falling edge Port A clock
PMODE1	A_PMODE	0, 1	0	0: Bypass Port A read data register 1: Pipeline Port A read data
WMODE1	A_WMODE	0, 1	0	0: Hold Port A read data 1: Feed through Port A write data to read data
A_DOUT_EN_POLARITY	A_DOUT_EN_POLARITY	PMODE1=1 0, 1, 2	2	0: Active-low Port A read data register enable 1: Active-high Port A read data register enable 2: Port A read data register enable tied off to be always active

Table 5-1 • Dual-Port Large SRAM Parameters

GENFILE Parameter	Configurator Parameter	Valid Range	Default	Description
A_DOUT_SRST_POLARITY	A_DOUT_SRST_POLARITY	PMODE1=1 0, 1, 2	2	0: Active-low Port A read data register Sync-reset 1: Active-high Port A read data register Sync-reset 2: Port A read data register Sync-reset tied off to be always inactive
A_DOUT_ARST_POLARITY	A_DOUT_ARST_POLARITY	PMODE1=1 0, 1, 2	2	0: Active-low Port A read data register Async-reset 1: Active-high Port A read data register Async-reset 2: Port A read data register Async-reset tied off to be always inactive
RE_POLARITY	B_BLK_POLARITY	0, 1, 2	2	0: Active-low Port B enable 1: Active-high Port B enable 2: Port B enable tied off to be always active
RCLK_EDGE	B_CLK_EDGE	CLKS=2 RISE, FALL	RISE	RISE: Rising edge Port B clock FALL: Falling edge Port B clock
PMODE2	B_PMODE	0, 1	0	0: Bypass Port B read data register 1: Pipeline Port B read data
WMODE2	B_WMODE	0, 1	0	0: Hold Port B read data 1: Feed through Port B write data to read data
B_DOUT_EN_POLARITY	B_DOUT_EN_POLARITY	PMODE2=1 0, 1, 2	2	0: Active-low Port B read data register enable 1: Active-high Port B read data register enable 2: Port B read data register enable tied off to be always active
B_DOUT_SRST_POLARITY	B_DOUT_SRST_POLARITY	PMODE2=1 0, 1, 2	2	0: Active-low Port B read data register Sync-reset 1: Active-high Port B read data register Sync-reset 2: Port B read data register Sync-reset tied off to be always inactive
B_DOUT_ARST_POLARITY	B_DOUT_ARST_POLARITY	PMODE2=1 0, 1, 2	2	0: Active-low Port B read data register Async-reset 1: Active-high Port B read data register Async-reset 2: Port B read data register Async-reset tied off to be always inactive
CLOCK_PN	CLOCK_PN	CLKS=1	CLK	Single clock Port name
DATAA_IN_PN	DATAA_IN_PN		A_DIN	Port A write data Port name
ADDRESSA_PN	ADDRESSA_PN		A_ADDR	Port A address Port name
BLKA_PN	BLKA_PN	A_BLK_POLARITY<2	A_BLK	Port A enable Port name
CLKA_PN	CLKA_PN	CLKS=2	A_CLK	Port A clock Port name
RWA_PN	RWA_PN		A_WEN	Port A Write enable Port name
DATAA_OUT_PN	DATAA_OUT_PN		A_DOUT	Port A read data Port name
A_DOUT_EN_PN	A_DOUT_EN_PN	PMODE1=1	A_DOUT_EN	Port A read data register enable Port name

Table 5-1 • Dual-Port Large SRAM Parameters

GENFILE Parameter	Configurator Parameter	Valid Range	Default	Description
A_DOUT_SRST_PN	A_DOUT_SRST_PN	PMODE1=1	A_DOUT_SRST_N	Port A read data register Sync-reset Port name
A_DOUT_ARST_PN	A_DOUT_ARST_PN	PMODE1=1	A_DOUT_ARST_N	Port A read data register Async-reset Port name
DATAB_IN_PN	DATAB_IN_PN		B_DIN	Port B write data Port name
ADDRESSB_PN	ADDRESSB_PN		B_ADDR	Port B address Port name
BLKB_PN	BLKB_PN	B_BLK_POLARITY<2	B_BLK	Port B enable Port name
CLKB_PN	CLKB_PN	CLKS=2	B_CLK	Port B clock Port name
RWB_PN	RWB_PN		B_WEN	Port B Write enable Port name
DATAB_OUT_PN	DATAB_OUT_PN		B_DOUT	Port B read data Port name
B_DOUT_EN_PN	B_DOUT_EN_PN	PMODE2=1	B_DOUT_EN	Port B read data register enable Port name
B_DOUT_SRST_PN	B_DOUT_SRST_PN	PMODE2=1	B_DOUT_SRST_N	Port B read data register Sync-reset Port name
B_DOUT_ARST_PN	B_DOUT_ARST_PN	PMODE2=1	B_DOUT_ARST_N	Port A read data register Async-reset Port name

A – Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call 800.262.1060

From the rest of the world, call 650.318.4460

Fax, from anywhere in the world, 408.643.6913

Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

Visit the Customer Support website (www.microsemi.com/soc/support/search/default.aspx) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the website.

Website

You can browse a variety of technical and non-technical information on the SoC home page, at www.microsemi.com/soc.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

My Cases

Microsemi SoC Products Group customers may submit and track technical cases online by going to [My Cases](#).

Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office. [Sales office listings](#) can be found at www.microsemi.com/soc/company/contact/default.aspx.

ITAR Technical Support

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech_itar@microsemi.com. Alternatively, within [My Cases](#), select **Yes** in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the [ITAR](#) web page.



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