# Table of Contents

Introduction ................................................................. 3

1 Functionality ............................................................. 5
   Identification .......................................................... 5
   Protocol Configuration ............................................... 5
   Protocol 1 and 2: Type, Number of Lanes, Speed ................. 6
   Lane Configuration ..................................................... 6
   XAUI Fabric SPLL Configuration .................................. 7
   EPCS Lane TX/RX Clock Selection ................................. 8
   Reference Clock Configuration ...................................... 8
   IO Standards ............................................................. 10
   Signal Integrity Options ............................................. 11
   High Speed Serial Interface Control Registers ................... 14
   SERDES (EPCS) High Speed Serial Interface Initialization .... 16
   Building EPCS Initialization Circuitry with EPCS_INIT Component ............................................. 17
   Interfacing SERDES (EPCS) with the Initialization Logic ....... 19

2 Port Description .......................................................... 21

3 Product Support .......................................................... 25
   Customer Service ...................................................... 25
   Customer Technical Support Center ............................... 25
   Technical Support ...................................................... 25
   Website ....................................................................... 25
   Contacting the Customer Technical Support Center ............ 25
   ITAR Technical Support ................................................ 26
Introduction

The RTG4 High Speed Serial Interface (EPCS and XAUI) core (NPSS_SERDES_IF) in the RTG4 family (Figure 1) supports the EPCS and XAUI protocol. NPSS means Non-PCIe High Speed Serial Interface.

Note: The RTG4 High Speed Serial Interface (EPCS and XAUI) core does not support the PCIe protocol.

For the PCIe protocol, use the RTG4 High Speed Serial Interface (PCIe, EPCS and XAUI) core.

The device may contain one or more High Speed Serial Interface blocks depending on its size. Refer to the RTG4 Datasheet or Product Brief for details.

As you make selections in the core configurator, it automatically narrows down the subsequent choices and defaults. Only the relevant ports appear in the generated macro.

In this document, we describe how you can configure a High Speed Serial Interface instance and define how the signals are connected.

To access the RTG4 High Speed Serial Interface (EPCS and XAUI) Configurator:

1. Instantiate the RTG4 High Speed Serial Interface (EPCS and XAUI) core from the Catalog into the SmartDesign Canvas, as shown in Figure 1.

2. Double-click the NPSS_SERDES block on the Canvas to open the Configurator.

Figure 1 • RTG4 High Speed Serial Interface (EPCS and XAUI) Block Instantiation on the SmartDesign Canvas
By default, SERDES_1 is checked when you open the Configurator.

Figure 2 • RTG4 High Speed Serial Interface (EPCS and XAUI) Configurator
1 – Functionality

Identification

RTG4 devices contain multiple High Speed Serial Interface blocks. The first row of checkboxes lets you identify which High Speed Serial Interface block (SERDES_1, SERDES_2, SERDES_3, SERDES_4) is being configured.

Note: The SERDES block names are dependent on the number of blocks present in the device. The SERDES blocks shown in Figure 2 are based on the RT4G150 device. Refer to the RTG4 device datasheet for a list of resources available on a device.

Protocol Configuration

RTG4 High Speed Serial Interface (EPCS and XAUI) block supports two protocols: Protocol 1 and Protocol 2. For each Protocol, you must configure the Type and Number of Lanes.

Protocol 1

Select your Protocol type from the drop-down menu:

- XAUI
- EPCS

Protocol 2

Select your Protocol type from the drop-down menu:

- EPCS (available only when XAUI is not selected for Protocol 1)

Notes:

- You must Configure Protocol 1 before configuring Protocol 2.
- Protocol 2 Types are context sensitive; they depend on the options you have selected in Protocol 1.
- Protocol 2 Type selection is disabled when you select XAUI in Protocol 1.

Number of Lanes

Select the number of lanes you wish to configure for Protocol 1 from the drop-down menu:

- X1 - Configure for 1 lane
- X2 - Configure for 2 lanes
- X4 - Configure for all 4 lanes

Note: Items in the drop-down list are context sensitive and depend on the Protocol Type. If Protocol Type is XAUI, all four lanes are selected by default.
Protocol 1 and 2: Type, Number of Lanes, Speed

Table 1-1 shows the protocol combinations that are feasible within a single High Speed Serial Interface block.

Table 1-1 • Available Protocols

<table>
<thead>
<tr>
<th>Protocol Type</th>
<th>Protocol #</th>
<th>Lane Width</th>
<th>Lane Assignment</th>
<th>Description</th>
<th>Speed Choices</th>
</tr>
</thead>
<tbody>
<tr>
<td>XAUI</td>
<td>Protocol 1</td>
<td>x4</td>
<td>Lane 0, Lane 1, Lane 2, Lane 3</td>
<td></td>
<td>3.125 Gpbs</td>
</tr>
<tr>
<td>EPCS</td>
<td>Protocol 1</td>
<td>x1</td>
<td>Users can select Lane 0, 1, 2 or 3</td>
<td>Lane 2 or 3 can be selected when Protocol 2 is not used.</td>
<td>Custom Speed</td>
</tr>
<tr>
<td></td>
<td>x2</td>
<td></td>
<td>Lane 0, Lane 1</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>x4</td>
<td></td>
<td>Lane 0, Lane 1, Lane 2, Lane 3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Protocol 2</td>
<td>x1</td>
<td></td>
<td>Users can select Lane 2 or 3</td>
<td>Not available when Protocol 1 is XAUI</td>
<td></td>
</tr>
<tr>
<td></td>
<td>x2</td>
<td></td>
<td>Lane 2, Lane 3</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Lane Configuration

Use Lane Configuration to configure up to four lanes for your SERDES. Refer to Table 1-1 on page 6 for lane configuration.

**Figure 1-1 • RTG4 High Speed Serial Interface (EPCS and XAUI) Configurator—Lane Configuration**

**Speed** - Available selections depend on your selected Protocol:

- 3.125 Gpbs for XAUI Protocol
- Custom Speed for EPCS Protocol

**Reference Clock Source** - Clock sources can be differential or single-ended. You can select one of the following options for Protocol 1 and Protocol 2:
- REFCLK (Differential)
- REFCLK0 (Voltage_Referenced)
- REFCLK1 (Voltage_Referenced)
- REFCLK0 (Single_Ended)
- REFCLK1 (Single_Ended)
- Fabric (Available only for EPCS Protocol)

Note: Lane 0 and Lane 1 share the same Reference Clock and Lane 2 and Lane 3 share the same Reference Clock. The selected Reference Clock is always available as REFCLK0_OUT or REFCLK1_OUT and can be used as clock source for logic inside Fabric.

PHY RefClk Frequency (MHz) - For EPCS Custom Speed, enter values between 100 and 160 MHz. For XAUI, the Frequency is fixed at 156.25 MHz.

Data Rate (Mbps) - Read-only fixed value for XAUI. For EPCS, select the data rate from the drop-down menu. Data Rates are computed based on the PHY RefClk Frequency.

Data Width - Read-only fixed value for XAUI. For EPCS, the data width varies with Data Rate (Mbps) as follows:
- 20 bit (for 5000 Mbps and 2500 Mbps)
- 16 bit (for 4000 Mbps or 2000 Mbps)
- 10 bit (2500 Mbps or 1250 Mbps)
- 8 bit (for 2000 Mbps or 1000 Mbps)
- 5 bit for 1250 Mbps
- 4 bit (for 1000 Mbps)

The displayed value is computed and updated based on your selected PHY RefClk Frequency and Data Rate.

FPGA Interface Frequency (MHz) - Read-only fixed value for XAUI. For EPCS Custom Speed, the displayed value is computed and updated based on the PHY RefClk Frequency and Data Rate you select.

VCO Rate (MHz) - Read-only fixed value for XAUI. For EPCS Custom Speed, the displayed value is computed and updated based on the PHY RefClk Frequency and Data Rate you select.

**XAUI Fabric SPLL Configuration**

The SPLL configuration field is relevant only for the XAUI protocol (Figure 1-2).

The CLK_BASE Frequency is read-only and fixed at 156.25 MHz.

---

**Figure 1-2 • XAUI Fabric SPLL Configuration**
EPCS Lane TX/RX Clock Selection

The EPCS Lane TX/RX Clock Selection option is only relevant when the Protocol selected is EPCS (Figure 1-3). It is not visible in other protocols. This option allows users to select the clocks to use for the TX/RX fabric interface and the logic in Fabric.

Reference Clock Configuration

This option allows you to configure the Multi-Standard User IO (MSIO) Reference Clock. Click the Configure Reference Clock Receiver button to open the Configuration Dialog Box (Figure 1-4).

Based on the PHY Reference Clock source selection, the supported IO standards and other options such as Impedance, Receiver settings, Weak Pull-Up/Pull-Down settings are shown. For example, when PHY Reference Clock source selection is REFCLK_Differential, only the differential IO standards supported are shown.

In general, if there are multiple options to select, the Combo-Box is enabled and you can change the default selection. Otherwise, it is grayed out.
Figure 1-5 shows how the REFCLK selection is used for each channel when REFCLK Clock Source is REFCLK_Differential.

![Reference Clock Receiver Function Configuration](image)

**Figure 1-5 • REFCLK Selection for Each Channel when REFCLK Clock Source is REFCLK_Differential**

Figure 1-6 shows how REFCLK selection is used for each channel when REFCLK Clock Source is REFCLK0_Voltage or REFCLK1_Voltage.
IO Standards

Note: The voltage for all SERDES block IOs must be the same.

The various differential IO standards supported are:
- LVDS33
- LVDS25
- RSDS
- MiniLVDS
- LVPECL33

The various voltage referenced IO standards supported are:
- SSTL25
- SSTL18
- HSTL18

The various single ended IO standards supported are:
- LVTTL33
- LVCMOS33
- LVCMOS25
• LVCMOS18

Note: The IO Standard voltage must be the same for both REFCLK_P(PAD_A) and REFCLK_N(PAD_B). When you make a change in IO Standard to REFCLK_P(PAD_A), the Configurator makes the same change to REFCLK_N(PAD_B), and vice versa.

**ODT Impedance Setting**

The various options supported (depending on the IO standard selected) are:

• Unterminated
• 50 Ohms
• 100 Ohms

Note: The LVDS33 I/O standard does not support On Die Termination (ODT).

**Schmitt Trigger**

The options supported are:

• On
• Off

**Weak Pull Mode**

The options supported are:

• On
• Off

**Signal Integrity Options**

Click the **Signal Integrity Options** button to open the Signal Integrity Configuration dialog box.

![Signal Integrity Options](image)

*Figure 1-7 • Signal Integrity Options*
The Signal Integrity Configuration dialog box gives you controls to maintain signal integrity and to mitigate signal integrity problems (Figure 1-8).

The values you enter are used to set register values related to signal integrity. Lanes which are not used are grayed-out in this dialog box.

**Transmit De-Emphasis**

Enter any value between 0.1 and 36.1 (in dB) in the *Required* edit box for both Pre-Transmit and Post-Transmit stage. Not all values are supported. Refer to Table 1-2 for all Actual values supported. The value you enter in the *Required* box will be matched to the closest valid Actual value and reported in the *Actual* box. The Configurator sets appropriate values for LANE<n>_TX_PRE_RATIO and LANE<n>_TX_PST_RATIO registers based on the Actual value.

LANE<n>_TX_PRE_RATIO and LANE<n>_TX_PST_RATIO registers are set based on the Actual value, as shown in Table 1-2. The default value for *Required* is 0 for Pre-Transmit, 3.5 for Post-Transmit. Lane<n>_TX_AMP_RATIO registers are always set to 0x80 for all lanes.
### Table 1-2 • EPCS Configuration for Different Data Width

<table>
<thead>
<tr>
<th>Feature</th>
<th>Control Registers</th>
<th>Actual Value=value programmed in register</th>
</tr>
</thead>
</table>
| De-Emphasis Pre       | LANE<n>_TX_PRE_RATIO | 0.1dB = 0x1  
                        |                                  | 0.3dB = 0x2  
                        |                                  | 0.4dB = 0x3  
                        |                                  | 0.5dB = 0x4  
                        |                                  | 0.7dB = 0x5  
                        |                                  | 0.9dB = 0x6  
                        |                                  | 1dB = 0x7    
                        |                                  | 1.2dB = 0x8   
                        |                                  | 1.3dB = 0x9   
                        |                                  | 1.5dB = 0xa   
                        |                                  | 1.6dB = 0xb   
                        |                                  | 1.8dB = 0xc   
                        |                                  | 2dB = 0xd     
                        |                                  | 2.1dB = 0xe    
                        |                                  | 2.3dB = 0xf    
                        |                                  | 2.5dB = 0x10   
                        |                                  | 2.7dB = 0x11   
                        |                                  | 2.9dB = 0x12   
                        |                                  | 3dB = 0x13     
                        |                                  | 3.3dB = 0x14    
                        |                                  | 3.5dB = 0x15    
                        |                                  | 3.7dB = 0x16    
                        |                                  | 3.9dB = 0x17    
                        |                                  | 4dB = 0x18      
                        |                                  | 4.3dB = 0x19     
                        |                                  | 4.5dB = 0x1a     
                        |                                  | 4.8dB = 0x1b     
                        |                                  | 5dB = 0x1c      
                        |                                  | 5.2dB = 0x1d     
                        |                                  | 5.5dB = 0x1e     
                        |                                  | 5.8dB = 0x1f     
                        |                                  | 6dB = 0x20      
                        |                                  | 6.3dB = 0x21     
                        |                                  | 6.5dB = 0x22     
                        |                                  | 7dB = 0x23      
                        |                                  | 7.2dB = 0x24     
                        |                                  | 7.5dB = 0x25     
                        |                                  | 7.8dB = 0x26     
                        |                                  | 8dB = 0x27      
                        |                                  | 8.5dB = 0x28     
                        |                                  | 9dB = 0x29      
                        |                                  | 9.3dB = 0x2a     
                        |                                  | 9.7dB = 0x2b     
                        |                                  | 10.1dB = 0x2c    
                        |                                  | 10.5dB = 0x2d    
                        |                                  | 11dB = 0x2e     
                        |                                  | 11.5dB = 0x2f    
                        |                                  | 12dB = 0x30     
                        |                                  | 12.6dB = 0x31    
                        |                                  | 13.2dB = 0x32    
                        |                                  | 13.8dB = 0x33    
                        |                                  | 14.5dB = 0x34    
                        |                                  | 15.2dB = 0x35    
                        |                                  | 16.1dB = 0x36    
                        |                                  | 17dB = 0x37     
                        |                                  | 18dB = 0x38     
                        |                                  | 19.2dB = 0x39    
                        |                                  | 20.5dB = 0x3a    
                        |                                  | 22.1dB = 0x3b    
                        |                                  | 24dB = 0x3c     
                        |                                  | 26.5dB = 0x3d    
                        |                                  | 30.1dB = 0x3e    
                        |                                  | 36.1dB = 0x3f    |
| De-Emphasis Post      | LANE<n>_TX_PST_RATIO |                                  |
**Note:** LANE<\(n\)> denotes the lane number where \(n\) can be 0, 1, 2 or 3.

For example, if you enter 2.4 dB in the **Required** box, 2.5dB (the closest match) is displayed in the **Actual** box and the registers are set as follows:

1. LANE<\(n\)>_TX_PRE_RATIO registers are set to 0x10.
2. LANE<\(n\)>_TX_PST_RATIO registers are set to 0x10.
3. LANE<\(n\)>_TX_AMP_RATIO registers are set to 0x80 for all lanes.

**Receive CTL Equalization**

There are 14 predefined settings available for user selection, in addition to the CTLE Disabled option (the default). Each predefined setting has the corresponding Cut-Off Frequency and Low Frequency Amplitude values preset and displayed when the predefined setting is selected. The impedance value for all predefined settings is 100 Ohms. Depending on the predefined setting, lane registers LANE<\(n\)>_RE_AMP_RATIO and LANE<\(n\)>_RE_CUT_RATIO are set to the values listed in Table 1-3.

---

**Table 1-3 • CTL Equalization Predefined Settings and Register Values**

<table>
<thead>
<tr>
<th>Pre-defined Setting #</th>
<th>Cut-Off Frequency (MHz)</th>
<th>Low Frequency Amplitude (dB)</th>
<th>LANE&lt;(n)&gt;_RE_AMP_RATIO (HEX)</th>
<th>LANE&lt;(n)&gt;_RE_CUT_RATIO (HEX)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTLE Disabled</td>
<td>N/A</td>
<td>N/A</td>
<td>0x00</td>
<td>0x00</td>
</tr>
<tr>
<td>1</td>
<td>400</td>
<td>10.88</td>
<td>0x77</td>
<td>0x20</td>
</tr>
<tr>
<td>2</td>
<td>500</td>
<td>13.06</td>
<td>0x5B</td>
<td>0x2A</td>
</tr>
<tr>
<td>3</td>
<td>600</td>
<td>13.98</td>
<td>0x51</td>
<td>0x2F</td>
</tr>
<tr>
<td>4</td>
<td>700</td>
<td>12.04</td>
<td>0x4A</td>
<td>0x32</td>
</tr>
<tr>
<td>5</td>
<td>800</td>
<td>13.38</td>
<td>0x3E</td>
<td>0x3C</td>
</tr>
<tr>
<td>6</td>
<td>900</td>
<td>13.98</td>
<td>0x39</td>
<td>0x40</td>
</tr>
<tr>
<td>7</td>
<td>1000</td>
<td>12.57</td>
<td>0x70</td>
<td>0x4F</td>
</tr>
<tr>
<td>8</td>
<td>1100</td>
<td>11.6</td>
<td>0x7D</td>
<td>0x58</td>
</tr>
<tr>
<td>9</td>
<td>1200</td>
<td>10.88</td>
<td>0x37</td>
<td>0xFE</td>
</tr>
<tr>
<td>10</td>
<td>1300</td>
<td>9.95</td>
<td>0x22</td>
<td>0xFC</td>
</tr>
<tr>
<td>11</td>
<td>1400</td>
<td>8.52</td>
<td>0x52</td>
<td>0xFE</td>
</tr>
<tr>
<td>12</td>
<td>1500</td>
<td>7.47</td>
<td>0x5B</td>
<td>0xFE</td>
</tr>
<tr>
<td>13</td>
<td>1600</td>
<td>7.04</td>
<td>0x73</td>
<td>0xFE</td>
</tr>
<tr>
<td>14</td>
<td>1700</td>
<td>6.66</td>
<td>0x78</td>
<td>0xFE</td>
</tr>
</tbody>
</table>

**Note:** LANE<\(n\)> denotes the lane number where \(n\) can be 0, 1, 2, or 3.

---

**Power Down Register Settings**

This controls the Physical Reset behavior of the EPCS SERDES when there is a lack of RX activity.

- Enabled (Physical Reset behavior is enabled)
- Disabled (Physical Reset behavior is disabled)

---

**High Speed Serial Interface Control Registers**

The High Speed Serial Interface has a set of registers that can be configured at runtime. The configuration values for these registers represent different parameters, refer to [UG:0567: RTG4 High Speed Serial Interfaces User Guide](#).

The majority of these registers are automatically populated by the selections made in the Configuration GUI. However, in some advanced configurations it may be necessary to modify these registers directly.
High Speed Serial Interface Registers Configuration

To enter the High Speed Serial Interface configuration values, specify the register values when you are configuring the High Speed Serial Interface. Click **Edit Registers** in the High Speed Serial Interface Configurator (Figure 2 on page 4) to open the Registers Configuration dialog box (Figure 1-9). Data entered in this configurator is written at power up in the High Speed Serial Interface registers.

Alternatively, you can click the Import Configuration button and import an existing configuration text file to configure the Registers.

The Registers Configuration dialog box enables you to enter High Speed Serial Interface register values using a graphical interface. The dialog box has the following features:

- **Registers Table** - Enter register values one-by-one using the Registers Table. To enter a register value, expand the register data tree (using the arrow or + sign), and click the **Actual Value** column to edit.

- **Import Configuration** - Import complete register configurations from text files. Register configuration syntax is shown below; Microsemi recommends using this method.
• **Export Configuration** - You can export the current register configuration data into a text file. The syntax of the exported file is the same as that of importable register configuration text files. For example:

```
LANE0_CR0                                 0x80
LANE0_ERRCNT_DEC                          0x20
LANE0_RXIDLE_MAX_ERRCNT_THR               0xF8
LANE0_IMPED_RATIO                         0x80
LANE0_PLL_F_PCLK_RATIO                    0x0
LANE0_PLL_M_N                              0x13
LANE0_CNT250NS_MAX                        0x20
LANE0_RE_amp_RATIO                        0x00
LANE0_RE_cut_RATIO                        0x00
LANE0_TX_amp_RATIO                        0x80
LANE0_TX_pst_RATIO                        0x0
LANE0_TX_pre_RATIO                        0x00
LANE0_ENDCALIB_MAX                        0x10
```

• **Reset Configuration** - Click Reset Configuration to undo any changes you have made to the register configuration. This deletes all register configuration data and you must either re-import or reenter this data. The data is reset to the hardware reset values.

• **Hide Read-Only Registers** - Enables you to show or hide the read-only registers in the Register Table. These registers are mostly status registers and do not contribute to the configuration.

When you generate your FPGA, the configuration register data entered in this configurator is used to initialize the High Speed Serial Interface.

**SERDES (EPCS) High Speed Serial Interface Initialization**

The EPCS SERDES Initialization solution requires that, in addition to specifying SERDES configuration register values, you need to build the configuration and initialization circuitry in SmartDesign for your EPCS SERDES. To help you build the initialization circuitry, Microsemi provides the EPCS_INIT component ready for import as a Block into your Libero SoC Project. The core is located in `<LiberoSoC_installation>/Designer/templates/rtg4/epcs_init.cxz`.

The EPCS_INIT component consists of

- CoreABC soft IP core
- CoreAPB3 bus soft IP core

---

![EPCS_INIT Block](image-url)
Building EPCS Initialization Circuitry with EPCS_INIT Component

After you have configured the High Speed Serial Interface for the EPCS Protocol, you need to build the initialization circuitry for the EPCS.

1. From the catalog, right-click the RTG4 High Speed Serial Interface (EPCS and XAUI)) and choose Configure Core.
2. Click OK to exit the Configurator when done. Your SERDES component is generated. Libero generates the CoreABC program in the `<project_folder>/component/work/<component_name>/ <component_name>_0/<SERDES_location_name>_init_abc.txt` file.
3. Drag and drop the generated SERDES (EPCS) component from the Design Hierarchy window into the SmartDesign canvas.
4. Import the EPCS_INIT component into your LiberoSoC project as a block (File > Import > Blocks).
5. Navigate to the `<LiberoSoC_Installation_folder>/Designer/templates/rtg4` folder and select epcs_init.cxz to import. The imported block appears as a component inside the Design Hierarchy window.
6. Drag and drop the imported EPCS_INIT component from the Design Hierarchy window into the same SmartDesign Canvas where you have instantiated the SERDES (EPCS) core.
7. Double-click the epcs_init component in the SmartDesign canvas to expose the CoreABC sub-component.
8. Double-click the CoreABC component to open the CoreABC Configurator.
9. The CoreABC component is already configured as shown in Figure 1-11. Make sure it has the following selections.
   – The data bus width is 32.
   – The maximum number of instructions is at least 256.
   – Instruction Store is Hard (FPGA Logic Elements).
   – Use IOWRT operation as optional instructions.
10. Copy the CoreABC program generated for your SERDES (EPCS) from the `<SERDES_location_name>_init_abc.txt` file created under the `<project_location>/component/work/<component_name>/<component_name_0>` folder and paste to the CoreABC Program tab. See Figure 1-12. The program code loads the EPCS SERDES Configuration Registers with the values you have configured for your EPCS SERDES and starts the initialization sequence. Depending on the number of instructions generated in the `<SERDES_location_name>_init_abc.txt` file, you may have to increase the maximum number of Instructions.
Interfacing SERDES (EPCS) with the Initialization Logic

To interface the NPSS_SERDES to the initialization logic block EPCS_INIT, make the necessary connections between the EPCS_INIT block and your NPSS_SERDES block in the SmartDesign canvas as follows.

**Figure 1-12 • CoreABC Program Code for EPCS SERDES**

```c
// CoreABC SERDES Initialization Sequence
//
// You must copy the CoreABC code from the
// <name>_init_abc.txt file generated for the SERDES
// component being initialized
//
// CoreABC SERDES Initialization Sequence
//
// Allow time for the APB interface to be ready after reset
NOP
NOP

// SYSTEM_CONFIG_PHV_MODE_1
APDMAT DAT 0x2e2e0 0x10
// LANE0_PHY_RESET_OVERRIDE
APDMAT DAT 0x01190 0x30
// LANE0_CRI
APDMAT DAT 0x01100 0x80
// LANE0_ERROR_DEC
APDMAT DAT 0x01010 0x20
// LANE0_RXCH_MAX_ERROR_THR
APDMAT DAT 0x01020 0x80
// LANE0_RXCH_RXED_RAT
APDMAT DAT 0x01030 0x10
// LANE0_CALIB_STABILITY_COUNT
APDMAT DAT 0x01040 0x20
// LANE0_RX_OFFSET_COUNT
APDMAT DAT 0x01050 0x20
// LANE0_PLL3_PLL_ECP
APDMAT DAT 0x01140 0x2
// LANE0_PLL3_PLL_ECP
APDMAT DAT 0x01100 0x22
// LANE0_PHY_RESET_OVERRIDE
APDMAT DAT 0x01190 0x0
// LANE0_UPDATE_SETTINGS
APDMAT DAT 0x01200 0x1
// SYSTEM_CONFIG_PHV_MODE_1
APDMAT DAT 0x2e2e0 0x20
// LANE0_PHY_RESET_OVERRIDE
APDMAT DAT 0x01190 0x30
```
When completed, click the Generate button in SmartDesign to generate the EPCS SERDES subsystem.

Configuration and initialization of your EPCS SERDES subsystem is complete.

Table 1-4 • Interface Connections Between epcs_init Block and NPSS_SERDES Block

<table>
<thead>
<tr>
<th>Port/Bus Interface (BIF) of SERDES Block</th>
<th>Port/Bus Interface (BIF) of Initialization Logic Block EPCS_INIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>APB_SLAVE</td>
<td>INIT_APB</td>
</tr>
<tr>
<td>APB_S_PCLK</td>
<td>INIT_CLK</td>
</tr>
<tr>
<td>APB_S_PRESET_N</td>
<td>INIT_RESET_N</td>
</tr>
<tr>
<td>EPCS_0_RESET_N</td>
<td>INIT_DONE</td>
</tr>
</tbody>
</table>

Figure 1-13 • SERDES (EPCS) Subsystem Initialization Circuity
# Port Description

## Table 2-1 • APB Ports

<table>
<thead>
<tr>
<th>Port</th>
<th>Direction</th>
<th>Port Group</th>
</tr>
</thead>
<tbody>
<tr>
<td>APB_S_PRDATA[31:0]</td>
<td>OUT</td>
<td>APB_SLAVE</td>
</tr>
<tr>
<td>APB_S_PREADY</td>
<td>OUT</td>
<td></td>
</tr>
<tr>
<td>APB_S_PSLVERR</td>
<td>OUT</td>
<td></td>
</tr>
<tr>
<td>APB_S_PADDR[13:2]</td>
<td>IN</td>
<td></td>
</tr>
<tr>
<td>APB_S_PENABLE</td>
<td>IN</td>
<td></td>
</tr>
<tr>
<td>APB_S_PSEL</td>
<td>IN</td>
<td></td>
</tr>
<tr>
<td>APB_S_PWDATA[31:0]</td>
<td>IN</td>
<td></td>
</tr>
<tr>
<td>APB_S_PWRITE</td>
<td>IN</td>
<td></td>
</tr>
<tr>
<td>APB_S_PCLK</td>
<td>IN</td>
<td></td>
</tr>
<tr>
<td>APB_S_PRESET_N</td>
<td>IN</td>
<td></td>
</tr>
</tbody>
</table>

## Table 2-2 • XAUI Control Ports

<table>
<thead>
<tr>
<th>Port</th>
<th>Direction</th>
</tr>
</thead>
<tbody>
<tr>
<td>CORE_RESET_N</td>
<td>IN</td>
</tr>
<tr>
<td>PHY_RESET_N</td>
<td>IN</td>
</tr>
<tr>
<td>SPLL_LOCK</td>
<td>OUT</td>
</tr>
<tr>
<td>PLL_LOCK_INT</td>
<td>OUT</td>
</tr>
<tr>
<td>PLL_LOCKLOST_INT</td>
<td>OUT</td>
</tr>
</tbody>
</table>

## Table 2-3 • XAUI Ports

<table>
<thead>
<tr>
<th>Port</th>
<th>Direction</th>
</tr>
</thead>
<tbody>
<tr>
<td>XAUI_RXD[63:0]</td>
<td>OUT</td>
</tr>
<tr>
<td>XAUI_RXC[7:0]</td>
<td>OUT</td>
</tr>
<tr>
<td>XAUI_VNDRESLO[7:0]</td>
<td>OUT</td>
</tr>
<tr>
<td>XAUI_VNDRESHI[7:0]</td>
<td>OUT</td>
</tr>
<tr>
<td>XAUI_MMD_MDC</td>
<td>IN</td>
</tr>
<tr>
<td>XAUI_MMD_MDI</td>
<td>IN</td>
</tr>
<tr>
<td>XAUI_MMD_MDI_EXT</td>
<td>IN</td>
</tr>
<tr>
<td>XAUI_MMD_MDOE_IN</td>
<td>IN</td>
</tr>
<tr>
<td>XAUI_MMD_PRTAD[4:0]</td>
<td>IN</td>
</tr>
</tbody>
</table>
### Table 2-3 • XAUI Ports (continued)

<table>
<thead>
<tr>
<th>Port</th>
<th>Direction</th>
</tr>
</thead>
<tbody>
<tr>
<td>XAUI_MMD_DEVID[4:0]</td>
<td>IN</td>
</tr>
<tr>
<td>XAUI_LOOPBACK_IN</td>
<td>IN</td>
</tr>
<tr>
<td>XAUI_MDC_RESET</td>
<td>IN</td>
</tr>
<tr>
<td>XAUI_TX_RESET</td>
<td>IN</td>
</tr>
<tr>
<td>XAUI_RX_RESET</td>
<td>IN</td>
</tr>
<tr>
<td>XAUI_TXD[63:0]</td>
<td>IN</td>
</tr>
<tr>
<td>XAUI_TXC[7:0]</td>
<td>IN</td>
</tr>
<tr>
<td>XAUI_MMD_MDO</td>
<td>OUT</td>
</tr>
<tr>
<td>XAUI_MMD_MDOE</td>
<td>OUT</td>
</tr>
<tr>
<td>XAUI_LOWPOWER</td>
<td>OUT</td>
</tr>
<tr>
<td>XAUI_LOOPBACK_OUT</td>
<td>OUT</td>
</tr>
<tr>
<td>XAUI_TX_CLK_OUT</td>
<td>OUT</td>
</tr>
<tr>
<td>XAUI_RX_CLK_OUT</td>
<td>OUT</td>
</tr>
<tr>
<td>XAUI_PHY_NOT_READY</td>
<td>OUT</td>
</tr>
<tr>
<td>XAUI_RX_CLK_IN</td>
<td>IN</td>
</tr>
<tr>
<td>XAUI_FB_CLK</td>
<td>IN</td>
</tr>
<tr>
<td>XAUI_LANE01_RX_ERR</td>
<td>IN</td>
</tr>
<tr>
<td>XAUI_LANE23_RX_ERR</td>
<td>IN</td>
</tr>
<tr>
<td>XAUI_PWRDN</td>
<td>IN</td>
</tr>
</tbody>
</table>

**Note:** When this input is driven high it powers down the XAUI Core. Tie Low for normal operation.

| XAUI_TX_OOB               | IN        |

**Note:** Unused for XAUI. Tie Low for normal operation.
### Table 2-4 • EPCS Ports per Lane

<table>
<thead>
<tr>
<th>Port</th>
<th>Direction</th>
<th>Ports Group</th>
</tr>
</thead>
<tbody>
<tr>
<td>EPCS_&lt;n&gt;_PWRDN</td>
<td>IN</td>
<td>EPCS_&lt;n&gt;_IN</td>
</tr>
<tr>
<td>EPCS_&lt;n&gt;_TX_VAL</td>
<td>IN</td>
<td></td>
</tr>
<tr>
<td>EPCS_&lt;n&gt;_TX_OOB</td>
<td>IN</td>
<td></td>
</tr>
<tr>
<td>EPCS_&lt;n&gt;_RX_ERR</td>
<td>IN</td>
<td></td>
</tr>
<tr>
<td>EPCS_&lt;n&gt;_RESET_N</td>
<td>IN</td>
<td></td>
</tr>
<tr>
<td>EPCS_&lt;n&gt;_TX_DATA[&lt;wd&gt;:0]</td>
<td>IN</td>
<td></td>
</tr>
<tr>
<td>EPCS_&lt;n&gt;_ARXSKIPBIT</td>
<td>IN</td>
<td></td>
</tr>
<tr>
<td>EPCS_&lt;n&gt;_RXFWF_RCLK</td>
<td>IN</td>
<td></td>
</tr>
<tr>
<td>EPCS_&lt;n&gt;_TXFWF_WCLK</td>
<td>IN</td>
<td></td>
</tr>
<tr>
<td>EPCS_FAB_REF_CLK</td>
<td>IN</td>
<td>EPCS_&lt;n&gt;_OUT</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EPCS_&lt;n&gt;_READY</td>
<td>OUT</td>
<td>EPCS_&lt;n&gt;_OUT</td>
</tr>
<tr>
<td>EPCS_&lt;n&gt;_TX_CLK_STABLE</td>
<td>OUT</td>
<td></td>
</tr>
<tr>
<td>EPCS_&lt;n&gt;_TX_CLK</td>
<td>OUT</td>
<td></td>
</tr>
<tr>
<td>EPCS_&lt;n&gt;_RX_CLK</td>
<td>OUT</td>
<td></td>
</tr>
<tr>
<td>EPCS_&lt;n&gt;_RX_VAL</td>
<td>OUT</td>
<td></td>
</tr>
<tr>
<td>EPCS_&lt;n&gt;_RX_IDLE</td>
<td>OUT</td>
<td></td>
</tr>
<tr>
<td>EPCS_&lt;n&gt;_RX_RESET_N</td>
<td>OUT</td>
<td></td>
</tr>
<tr>
<td>EPCS_&lt;n&gt;_TX_RESET_N</td>
<td>OUT</td>
<td></td>
</tr>
<tr>
<td>EPCS_&lt;n&gt;_RX_DATA[&lt;wd&gt;:0]</td>
<td>OUT</td>
<td></td>
</tr>
<tr>
<td>GLOBAL_0_OUT</td>
<td>OUT</td>
<td></td>
</tr>
<tr>
<td>GLOBAL_1_OUT</td>
<td>OUT</td>
<td></td>
</tr>
</tbody>
</table>

**Note:**

1. `<n>` indicates the lane on which EPCS is configured.
   `<wd>` Valid values are 19, 15, 9, 7, 4, and 3.
2. GLOBAL_0_OUT and GLOBAL_1_OUT ports are available only if they have been configured in the configurator. See "EPCS Lane TX/RX Clock Selection" on page 8 for more information.
### Table 2-5 • PAD Ports

<table>
<thead>
<tr>
<th>Ports</th>
<th>Direction</th>
<th>Ports Group</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RXD0_P, RXD0_N</td>
<td>IN</td>
<td>PADs_IN</td>
<td>Differential input pair for lane 0 (Rx data)</td>
</tr>
<tr>
<td>RXD1_P, RXD1_N</td>
<td>IN</td>
<td>PADs_IN</td>
<td>Differential input pair for lane 1 (Rx data)</td>
</tr>
<tr>
<td>RXD2_P, RXD2_N</td>
<td>IN</td>
<td>PADs_IN</td>
<td>Differential input pair for lane 2 (Rx data)</td>
</tr>
<tr>
<td>RXD3_P, RXD3_N</td>
<td>IN</td>
<td>PADs_IN</td>
<td>Differential input pair for lane 3 (Rx data)</td>
</tr>
<tr>
<td>REFCLK_P, REFCLK_N</td>
<td>IN</td>
<td></td>
<td>Differential input reference clock pair.</td>
</tr>
<tr>
<td>TXD0_P, TXD0_N</td>
<td>OUT</td>
<td>PADs_OUT</td>
<td>Differential output pair for lane 0 (Tx data)</td>
</tr>
<tr>
<td>TXD1_P, TXD1_N</td>
<td>OUT</td>
<td>PADs_OUT</td>
<td>Differential output pair for lane 1 (Tx data)</td>
</tr>
<tr>
<td>TXD2_P, TXD2_N</td>
<td>OUT</td>
<td>PADs_OUT</td>
<td>Differential output pair for lane 2 (Tx data)</td>
</tr>
<tr>
<td>TXD3_P, TXD3_N</td>
<td>OUT</td>
<td>PADs_OUT</td>
<td>Differential output pair for lane 3 (Tx data)</td>
</tr>
</tbody>
</table>
3 – Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call **800.262.1060**
From the rest of the world, call **650.318.4460**
Fax, from anywhere in the world, **650.318.8044**

Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support


Website

You can browse a variety of technical and non-technical information on the Microsemi SoC Products Group home page, at [www.microsemi.com/soc](http://www.microsemi.com/soc).

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

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You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

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Sales office listings can be found at www.microsemi.com/soc/company/contact/default.aspx.

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