SmartDesign MSS

Clock Configuration

Microsemi

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Configuration Options

The Clock Management Configurator provides a single place where all clocks related to the MSS and the communication between the MSS and the FPGA fabric can be configured. For a complete description of the SmartFusion device clocking scheme, please refer to the Actel SmartFusion Microcontroller Subsystem User's Guide.

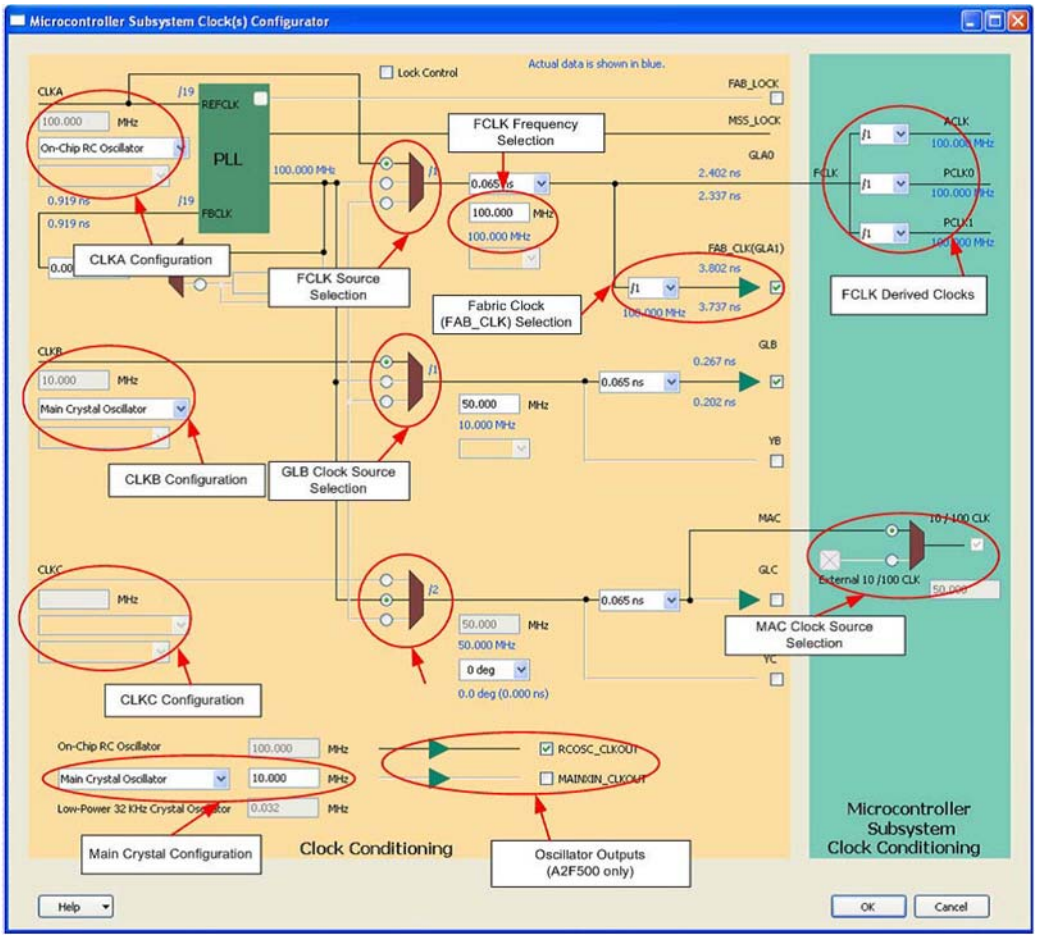

***Figure 1* • MSS CCC Configuration Options**

CLK<x> (x= A/B/C) Reference Clocks

To configure the CLK<x> reference clock, first select the clock source, then define the clock source frequency and, in the case of the hardwired I/O sources, the package pin assignment.

Clock Source Selection

The following sources are available from the reference clock pull-down menu:

- **External I/O -** The clock source can be any fabric I/O. The fabric I/O is routed to the reference clock fabric interface pin.
- **Hardwired I/O -** The clock source is one of three fabric I/Os that has a dedicated path to drive the reference clock. You must select a package pin assignment for the CLK<x> pin when choosing this option (see "Clock Pin Assignment" for more details).
- **Hardwired I/O (LVPECL) -** The clock source is one of two fabric I/Os (P side of the LVPECL pair) that has a dedicated path to drive the reference clock. You must select a package pin assignment for the CLK<x> pin when choosing this option (see "Clock Pin Assignment" for more details).
- **Hardwired I/O (LVDS) -** The clock source is one of two fabric I/Os (P side of the LVDS pair) that has a dedicated path to drive the reference clock. You must select a package pin assignment for the CLK<x> pin when choosing this option (see "Clock Pin Assignment" for more details).
- **Internal logic -** The clock source can be any FPGA fabric logic.
- **On-chip RC Oscillator -** The clock source is a dedicated 100 MHz On-chip RC Oscillator available on the SmartFusion device.
- **Main Crystal Oscillator -** See "Main Crystal Oscillator" on page 6.

Clock Frequency

You must specify the clock source frequency. Note the following frequency requirements:

- The On-chip Oscillator clock frequency is fixed to 100 MHz and cannot be changed.
- The Main Crystal Oscillator frequency is defined in the "Main Crystal Oscillator" on page 6.
- For all other sources, the source clock frequency must be between 1.5 MHz and 176MHz when the PLL is used or between 32 KHz and 350 MHz when the PLL is bypassed.

Clock Pin Assignment

When choosing a hardwired I/O option you must select a package pin assignment for the reference clock port. The pin assignment list may be different based on the hardwired I/O option chosen as well as the package selected for the current design. Note the following pin assignment requirements:

- If the External Memory Controller (EMC) has been enabled in the design, the LVDS option is not available. This is due to the fact that the EMC I/Os are placed in the same bank as the I/Os that have a dedicated connection to the reference clock CLK<x>. The EMC I/Os are using the LVTTL (3.3V) standard which is not compatible with LVDS (2.5V).
- All reference clocks must use compatible differential I/O standards. LVDS (2.5V) is not compatible with LVPECL (3.3V).

FCLK (GLA0) Clock

Clock Source Selection - To achieve the desired the MSS clock (FCLK) frequency, you may need to use the PLL. The following sources are available from the reference clock pull-down menu:

- **PLL Bypass -** To use this option, click the first PLL radio button.
- **VCO (0, 90, 180 and 270 degrees) -** To use this option, click the second PLL radio button then set the phase using the phase selection pull-down menu.
- **VCO (0 degree) with programmable delay -** To use this option, click the third PLL radio button.

Clock Frequency - You must specify your desired FCLK frequency. The actual frequency is displayed in blue below the frequency edit box.

FCLK Derived Clocks

There are three internal APB sub-busses in the MSS: ACE, APB sub-bus 1 and APB sub-bus 2. Each of these sub-bus peripherals are clocked by a derived clock from the MSS clock (FCLK). Each derived clock can be programmed individually as FCLK divided by 1, 2 or 4.

Note that some peripherals may require a slower PCLK to achieve certain configurations. Changing the PCLK of a sub-bus affects all peripherals present on that bus. For more details, please refer to the Actel SmartFusion Microcontroller Subsystem User's Guide.

Fabric Clock (FAB_CLK)

For applications where the AMBA fabric extension is used to connect to a soft AMBA subsystem (soft bus/bridge/peripheral cores), the fabric clock (FAB_CLK) must be configured such that the generated frequency meets the timing requirements of the logic implemented in the fabric. The fabric clock, when used, can only be the MSS clock divided by 1, 2 or 4 as per the architecture requirements for the SmartFusion device. You must verify that the fabric timing meets the selected fabric clock frequency by performing timing analysis of your design using SmartTime.

If you chose a divide value of 2 or 4 for FAB_CLK, then FAB_CLK will use the GLB output of the MSS CCC. In that case, the GLB/YB clock cannot be selected independently in the configurator. It is grayed out.

GLB/YB Clock

Enabling GLB or YB - If GLB is independently available (see Fabric Clock), then you may optionally enable GLB and YB. The GLB output drives a global network in the FPGA fabric while the YB output drives a local routing resource in the FPGA fabric.

Clock Source Selection - To achieve the desired the GLB/YB clock frequency, you may need to use the PLL. The following sources are available from the reference clock pull-down menu:

- **PLL Bypass -** To use this option, click the first PLL radio button.
- **VCO (0, 90, 180 and 270 degrees) -** To use this option, click the second PLL radio button then set the phase using the phase selection pull-down menu.
- **VCO (0 degree) with programmable delay -** To use this option, click the third PLL radio button.

Clock Frequency - You must specify the GLB/YB frequency that you wish to obtain. The actual frequency is displayed in blue below the frequency edit box.

Ethernet MAC Clock

If you enable the MAC peripheral on the MSS configurator canvas the MAC clock is automatically selected (read-only) in the Clock configurator. You also need to define the MAC clock source as one of the two following options:

- The external 10/100 clock on the SmartFusion device.

- A clock generated in the MSS Clock Conditioning Circuit (MCCC). In this case, the clock can either be:
  - Derived from the MSS reference clock using the PLL component output.
  - Selected from one of the following reference clock (CLKC) pull-down menu sources (see CLKC Reference Clock).

GLC/YC Clock

Enabling GLC or YC (Optional) - The GLC output drives a global network in the FPGA fabric; the YC output drives a local routing resource in the FPGA fabric.

Clock Source Selection - To achieve the desired GLC/YC clock frequency, you may need to use the PLL. The following sources are available from the reference clock pull-down menu:

- **PLL Bypass -** To use this option, click the first PLL radio button.
- **VCO (0, 90, 180 and 270 degrees) -** To use this option, click the second PLL radio button then set the phase using the phase selection pull-down menu.
- **VCO (0 degree) with programmable delay -** To use this option, click the third PLL radio button.

Clock Frequency - You must specify the GLC/YC frequency that you wish to obtain. The actual frequency is displayed in blue below the frequency edit box.

Note that the source of the GLC clock is the same as the MAC clock source if the MAC clock is generated from the MSSS CCC.

PLL Locks

MSS_LOCK and FAB_LOCK - These two signals are the MSS_CCC PLL LOCK signal. This is an Active High signal indicating that steady-state lock has been achieved between CLKA and the PLL feedback signal.

The MSS_LOCK signal is connected to the MSS System Register MSS_CCC_SR register (PLL_LOCK_SYNC). This register can be checked to see the status of the MSS CCC PLL lock.

The FAB_LOCK signal is available in the FPGA fabric and can be used by the users programmable logic to check to see the status of the MSS CCC PLL lock.

LockControl - Check the LockControl checkbox to select a slow lock acquisition time for the MSS CCC PLL. Refer to the SmartFusion Customizable System-on-Chip (cSoC) datasheet for a definition and values.

On-Chip RC Oscillator

RCOSC_CLKOUT - The A2F500 device has an extra CCC that is dedicated to the FPGA fabric: FAB_CCC. See the FAB_CCC document for more information. The On-chip RC Oscillator, generated as part of the MSS, can drive the CLKA, CLKB and CLKC clock inputs of the FAB_CCC core.

If you choose to use the on-chip RC oscillator to drive one of the FAB_CCC input clocks you must select the RCOSC_CLKOUT option to expose this port. This port can be then connected at the next level of hierarchy to the FAB_CCC.

Main Crystal Oscillator

The main crystal oscillator source can be chosen for CLKA, CLKB and as a clock source for the fabric CCC (only for the A2F500 device). Use the main crystal configuration options to set up main crystal.

Main Crystal Oscillator - The source is an external Crystal. See the Actel SmartFusion Microcontroller Subsystem User's Guide for details about how the external crystal must be connected on the board to the SmartFusion device.

Main Crystal Oscillator (RC network) - The source is an external RC circuit connected to the main crystal oscillator external pins. See the Actel SmartFusion Microcontroller Subsystem User's Guide for details about how the external RC network must be connected on the board to the SmartFusion device.

Main Crystal Oscillator Frequency

- The Main Crystal Oscillator clock frequency must be between 1.5 MHz and 20 MHz when you use the PLL or between 32 KHz and 20 MHz when you bypass the PLL.
- The Main Crystal Oscillator (RC network configuration) clock frequency must be between 1.5 MHz and 4 MHz when you use the PLL or between 32 KHz and 4 MHz when you bypass the PLL.

MAINXIN_CLKOUT - The A2F500 device has an extra CCC that is dedicated to the FPGA fabric - FAB_CCC. See the FAB_CCC document for more information. The Main Crystal Oscillator, generated as part of the MSS, can drive the CLKA and CLKB clock inputs of the FAB_CCC core. If you use the main crystal to drive one of the FAB_CCC input clocks you must select the MAINXIN_CLKOUT option to expose this port. This port can be then connected at the next level of hierarchy to the FAB_CCC.

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Contacting the Customer Technical Support Center

Microsemi staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions. The Customer Technical Support Center spends a great deal of time creating application notes and answers to FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

Microsemi customers can receive technical support on Microsemi SoC products by calling Technical Support Hotline anytime Monday through Friday. Customers also have the option to interactively submit and track cases online at My Cases or submit questions through email anytime during the week.

Web: www.actel.com/mycases

Phone (North America): 1.800.262.1060

Phone (International): +1 650.318.4460

Email: soc_tech@microsemi.com

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Phone (International): +1 650.318.4900

Email: soc_tech_itar@microsemi.com

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Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

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Phone: +1 650.318.2470

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