

SmartDesign MSS

MSS I/O Configuration

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Printed in the United States of America

Part Number: 5-02-00236-1

Release: July 2010

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Configuration Options

The SmartFusion Microcontroller Subsystem (MSS) has two banks of dedicated MSS I/Os. In the SmartFusion architecture MSS I/Os are shared between two MSS peripherals or between a MSS peripheral and the FPGA fabric. In this document, we describe how to assign and configure MSS I/Os to connect to the FPGA fabric.

Connectivity Options

IO_<index> (<peripheral>) - Select this option to indicate that the selected MSS I/O will be connected to the FPGA fabric. You must select whether you want the MSS I/Os to be configured as an INBUF, OUTBUF, TRIBUFF or BIBUF.

- <index>: indicates which MSS I/O port the parameter relates to.
- <peripheral>: indicates which MSS peripheral this MSS I/O is shared with.

MSS I/O Sharing

In the SmartFusion architecture MSS I/Os are shared between two MSS peripherals or between a MSS peripheral and the FPGA fabric. MSS I/Os that are not used to connect to a MSS peripheral can be connected to the FPGA fabric. The MSS I/O configurator provides direct feedback regarding whether a MSS I/O can be used into the current design.

GPIO[31:16]

MSS I/Os 0 to 15 (IO_<0...15> in the configurator) are shared with GPIO 0 to 15. If GPIO[index] is configured to be used in the GPIO configurator, then the MSS I/O Pad pull-down menu is grayed-out for the corresponding shared GPIOs and an Info icon is displayed next to the pull-down menu. The Info icon indicates that the MSS I/O option cannot be selected because it is already used or, based on the package selected, not bonded.

The blue text in the configurator highlights the package pin name for each MSS I/O. This information is useful for planning board layout.

Example

To demonstrate how the MSS I/O configurations and the GPIO[15:0] configurations are coupled, [Figure 1-1](#) shows both configurators side by side with the following configuration:

- MSS I/O[15] is used as an INBUF port connected to the FPGA fabric. Consequently, GPIO[15] cannot be connected to an MSS I/O.
- GPIO[5] is connected to an MSS I/O as an Input. Consequently MSS I/O[5] cannot be used to connect to the FPGA fabric.
- GPIO[3] is connected to the FPGA fabric as an Output. Consequently MSS I/O[3] cannot be used to connect to the FPGA fabric.

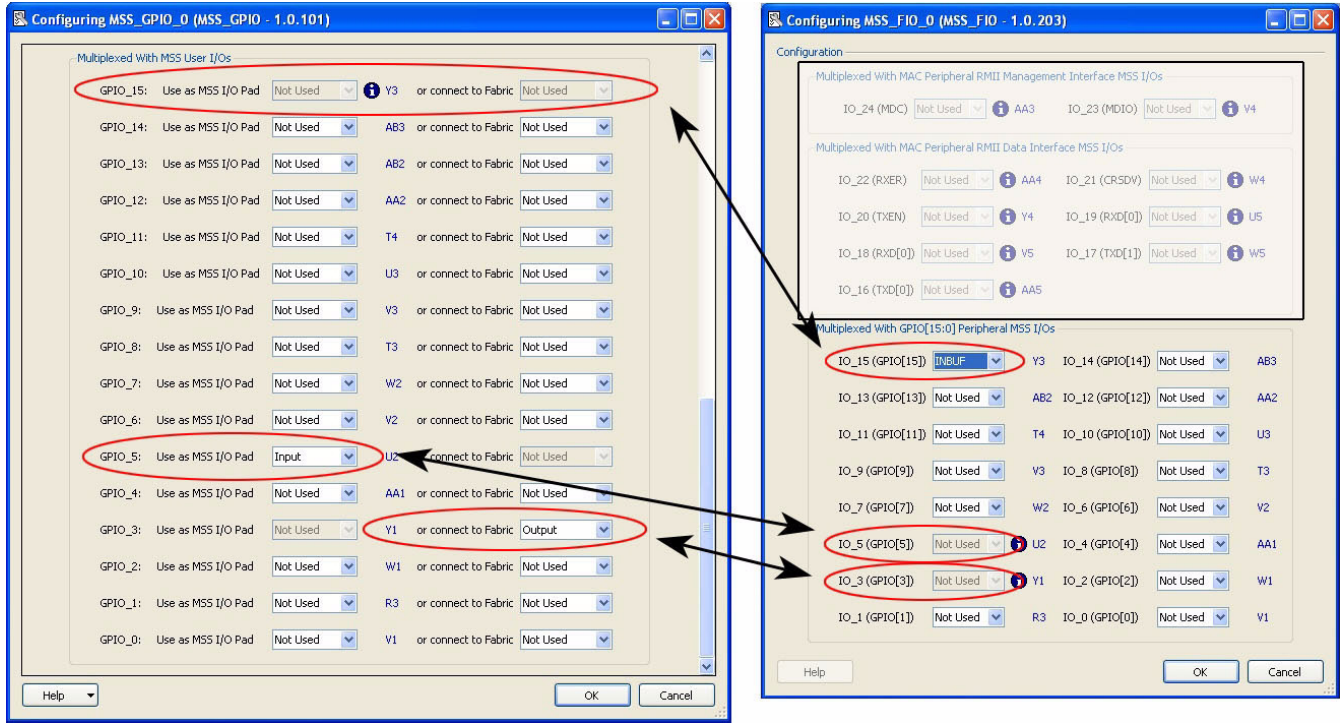


Figure 1-1 · MSS I/O and GPIO Configuration Example

Ethernet MAC

MSS I/Os 16 to 24 (IO_<16...24> in the configurator) are shared with the Ethernet MAC peripheral. MSS I/O availability is a function of the configuration of the MAC peripheral.

MSS I/Os 16 to 24 are broken into two groups in the MAC configurator; the same is done on this configurator (as shown in Figure 1-2). The MAC port names have been added for clarity.

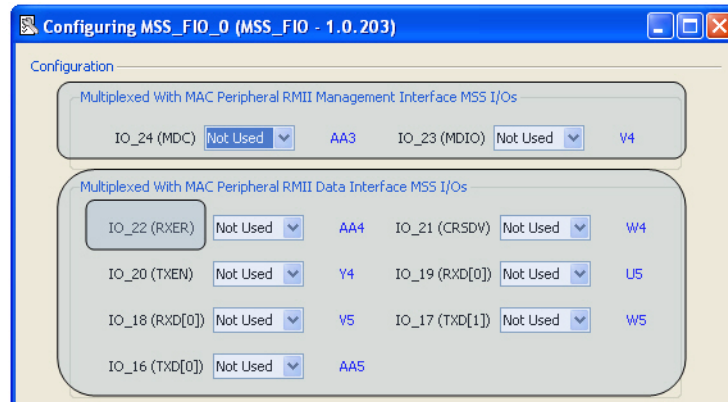


Figure 1-2 · Ethernet MAC Configurator

The configurator implements new DRCs to guarantee that the MSS I/O configuration is compatible with the MAC configuration.

Rule1 - For MSS I/Os using to the RMII Data Interface ports, you can only select a type that is compatible with the corresponding MAC port direction as specified in the compatibility table. The following messages are displayed in the Warning icon tool tip next to the MSS I/O being configured.

When the MAC Data Interface is connected to the fabric, only 'Not Used', 'OUTBUF' or 'TRIBUFF' can be selected.

When the MAC Data Interface is connected to the fabric, only 'Not Used' or 'INBUF' can be selected.

Table 1-1 · MAC and MSS I/O Compatibility

MAC Ports		MSS I/O	
Port	Direction	Port	Compatible Direction
TXD[0]	Output	IO_16	OUTBUF, TRIBUFF
TXD[1]	Output	IO_17	OUTBUF, TRIBUFF
RXD[0]	Input	IO_18	INBUF
RXD[1]	Input	IO_19	INBUF
TXEN	Output	IO_20	OUTBUF, TRIBUFF
CRSDV	Input	IO_21	INBUF
RXER	Input	IO_22	INBUF

A more detailed view of the IOMUX configuration is provided below.

Rule2 - When the Mac RMII Management Interface is connected to the fabric - using the MAC configurator - the MSS I/O IO_22 cannot be selected at all in the MSS I/O configurator. This is due to the fact that the MAC MDEN signal is brought to the FPGA fabric using the same IOMUX as the MAC RXER signal.

If the MAC peripheral is disabled all together on the MSS canvas there are no restrictions to using the corresponding MSS I/Os.

The blue text in the configurator highlights the package pin name for each MSS I/O. This information is useful for planning board layout.

IOMUX Configuration When the MAC RMII Data Interface is Connected to the FPGA Fabric

If the MSS MAC RMII Data Interface signals - TXD[1:0], RXD[1:0], TXEN, RXER and CRSDV - are connected to the FPGA fabric and the corresponding MSS I/Os have been selected in this configurator then the IOMUX structures are configured to provide two independent functions: a path from the MAC to/from the FPGA fabric (orange) and a path from the MSS I/O to/from the FPGA fabric (blue). When using a fabric to MSS I/O path, we can configure the MSS I/O as an INBUF, OUTBUF a TRIBUFF. These configurations are shown in [Figure 1-3](#) and [Figure 1-4](#).

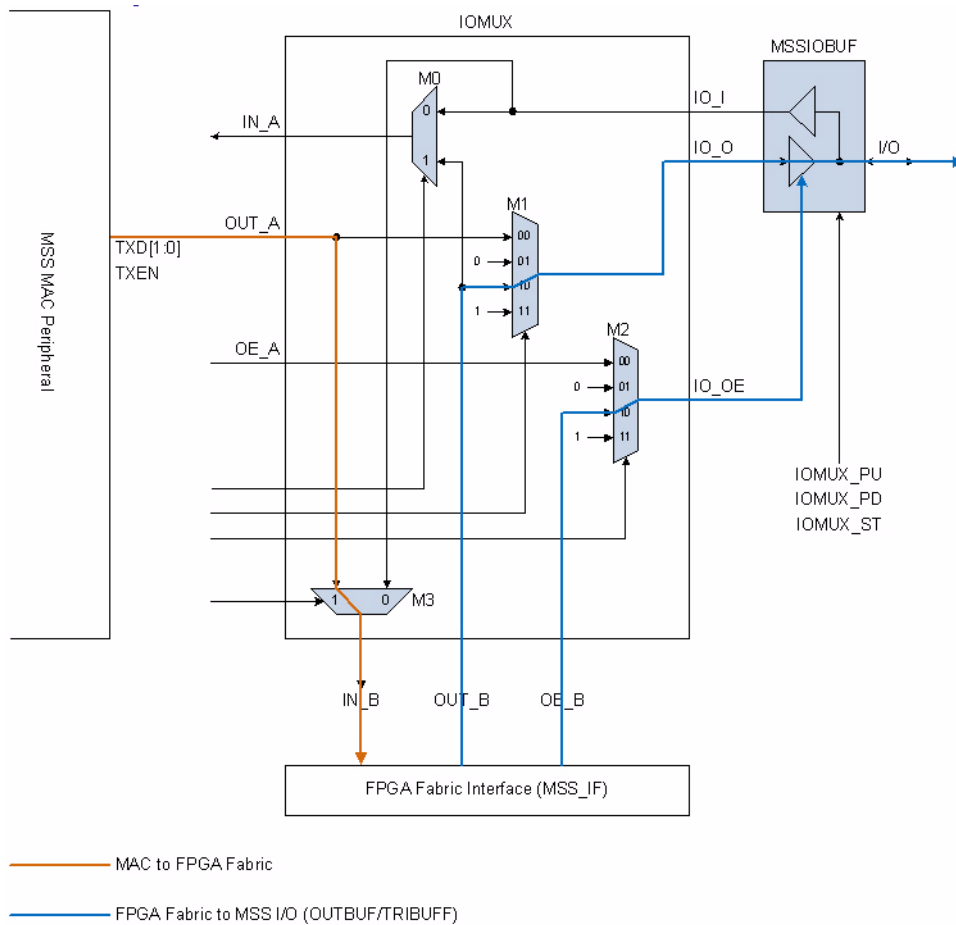


Figure 1-3 · Path from MAC to FPGA Fabric

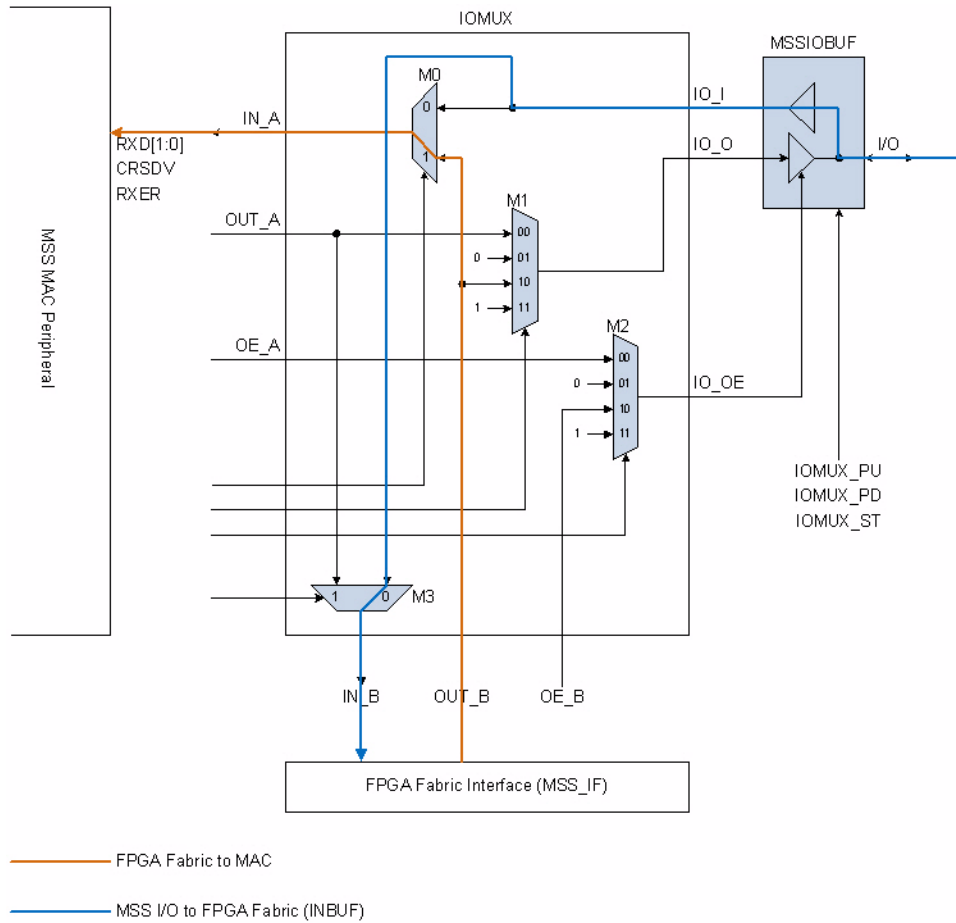


Figure 1-4 · Path from FPGA Fabric to MAC

Port Description

Table 2-1 · MSS I/O Port Description

Port Name	Direction	PAD?	Description
IO_<index>_PADIN	In	Yes	Port name when IO_<index> is configured as an MSS I/O INBUF port
IO_<index>_PADOUT	Out	Yes	Port name when IO_<index> is configured as an MSS I/O OUTBUF port
IO_<index>_PADTRI	Out	Yes	Port name when IO_<index> is configured as an MSS I/O TRIBUFF port
IO_<index>_PADBI	Inout	Yes	Port name when IO_<index> is configured as an MSS I/O BIBUF port
IO_<index>_D	In	No	Port name when IO_<index> is configured to connect to the FPGA fabric as an OUTBUF port (it is really the D port of the OUTBUF macro)
IO_<index>_E	In	No	Port name when IO_<index> is configured to connect to the FPGA fabric as a TRIBUFF or BIBUF port (it is really the E port of the TRIBUFF or BIBUF macro)
IO_<index>_Y	Out	No	Port name when IO_<index> is configured to connect to the FPGA fabric as an INBUF or BIBUF port (it is really the Y port of the INBUF or BIBUF macro)

Note:

- PAD ports are automatically promoted to top throughout the design hierarchy.
- Non-PAD ports must be promoted manually to the top level from the MSS configurator canvas to be available as the next level of hierarchy.

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