Libero SoC v11.8 Service Pack 1

Release Notes

10/2017

Microsemi
Power Matters.™

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Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision 1.3

Added Known Issue 5.17, SPPS: set_hsm_params Not Updating HSM Server Address.

Revision 1.2

Added Known Issue 5.15, SPPS: Job Manager Fails when Back Level Protection is ON. Added Known Issue 5.16, SPI Slave Programming Fails.

Revision 1.1

Removed duplicate entry in Resolved Issues table, updated description in section 2.1.6, RTG4 Reset RAM Block Contents.

Revision 1.0

Revision 1.0 is the first publication of this document.

Contents

1 Libero SoC v11.8 SP1 Release Notes

The Libero® system on chip (SoC) v11.8 SP1 release is a service pack release of the Libero SoC v11.8 software for designing with Microsemi's power efficient flash FPGAs, SoC FPGAs, and rad-tolerant FPGAs. The suite integrates industry standard Synopsys Synplify Pro® synthesis and Mentor Graphics ModelSim® simulation with best-in-class constraints management, debug capabilities, and secure production programming support.

Use Libero SoC v11.8 SP1 for designing with Microsemi's RTG4 Rad-Tolerant FPGAs, SmartFusion® 2 and SmartFusion® SoC FPGAs, and IGLOO® 2, IGLOO®, ProASIC® 3, and Fusion FPGA families.

To access datasheets, silicon user guides, tutorials, and application notes, visit www.microsemi.com, navigate to the relevant product family page, and click the **Documentation** tab. Development Kits & Boards are listed in the **Design Resources** tab.

Additional Reference Sources:

Read the following Product Change Notices (PCN) before using Libero SoC v11.8 SP1:

SmartFusion2/IGLOO2 Product Change Notice (PCN) 17027

RTG4 Product Change Notice (PCN) 17026

2 What's New in Libero SoC v11.8 SP1

2.1 Silicon Features

No new silicon part is introduced with this release.

2.1.1 SmartFusion2/IGLOO2 and RTG4 Timing Data Updates

There have been timing data updates to SmartFusion2/IGLOO2 and RTG4 devices after the release of Libero SoC v11.8.

2.1.2 SmartFusion2/IGLOO2 Bitstream Updates

There have been bitstream updates to SmartFusion2/IGLOO2 devices.

2.1.3 RTG4 On-Die-Termination (ODT) Change

There have been changes to the list of I/O standards that support ODT in the RT4G150 device.

2.1.4 RTG4 Power Data Updates

There have been power data updates to the RT4G150 device after the release of Libero SoC v11.8.

2.1.5 RT4G150-CQ352M

There are changes to the RTG4 CQ352M package.

Programming and export of design specific BSDL are enabled.

When designing with RT4G150-CQ352ES or RT4G150-CQ352MS, select the RT4G150-CQ352M option in Libero SoC.

2.1.6 RTG4 Reset RAM Block Contents

The RTG4 uPROM Configurator has been enhanced to allow addition of a client to be used specifically to reset the contents of all RAM blocks. At device power-up or when the DEVRST_N signal goes active, the RAM initialization client initializes all RAM blocks to Zero. After device power-up, the data read from all uSRAM and LSRAM address locations will be Zero until the RAM blocks are written to.

Note: When you read the initial Zero from an address in a RAM block that has ECC enabled, its SB_CORRECT and DB_DETECT flags will get asserted. The flags for any given RAM address location will be reset once that address location has been written to.

2.1.7 RTG4 Simulation of Power-on Reset/Preset

Post-synthesis and Post-layout simulation models of RTG4 in Libero SoC v11.8 SP1 will initiate a reset/preset of all registers at power-up. Pre-synthesis simulation remains unchanged and will not experience this reset/preset at power-up even if the RTL source instantiates gate-level macros.

2.1.8 RT4G150 DAT File Generation

Libero SoC v11.8 SP1 enables DAT file generation for the RT4G150 device. The DAT file allows customers to do in-system programming using a microprocessor or a state machine running DirectC algorithm.

2.1.9 M2GL025-VFG400 and Simultaneous Switching Noise (SSN)

The M2GL025-VFG400 package is added to the list of devices supported by SSN analysis tool.

2.2 Software Enhancements/Changes

Unless otherwise noted, Software Enhancements apply to all SmartFusion2, IGLOO2, and RTG4 devices.

2.2.1 Generate Simulation Files in Design Flow Window

Libero SoC v11.8 SP1 introduces the **Generate Simulation Files** as a new step in the Design Flow window. This step generates the post-synthesis Verilog or VHDL netlist. The *.v or *.vhd netlist file is placed in the <project_location>/synthesis folder and passed to the Simulator for post-synthesis simulation. The introduction of this new step reduces synthesis runtime.

This step must be preceded by a successful synthesis. If synthesis is not run before this step is invoked, the tool automatically initiates a synthesis run first before generating the netlist.

To run synthesis and post-synthesis simulation in batch mode, enter the following commands:

```
run_tool  -name {SYNTHESIZE} #run synthesis
run_tool  -name {EXPORTNETLIST} #new command to generate simulation files after synthesis
run_tool –name {SIM_POSTSYNTH} #run post-synthesis simulation
```

The second run_tool command, EXPORTNETLIST, is optional if the first run_tool command, SYNTHESIZE, is followed by the run_tool –name {SIM_POSTSYNTH} command.

2.2.2 SmartFusion2/IGLOO2 System Builder/MSS Components and SmartDesign

The Design Template tab in the New Project Wizard (New Project > Design Template) introduces an option to instantiate or not any System Builder/MSS component in a SmartDesign. By default, the checkbox is checked (instantiation). Un-check this box (No Instantiation) if you are using this project to create System Builder or MSS components and do not plan to use them in a SmartDesign based design. This is especially useful for design flows where the System Builder or MSS component is stitched into a design using HDL.

2.2.3 Design Hierarchy Enhancement for VHDL projects

The Libero SoC Design Hierarchy parser has been enhanced to allow import of VHDL entities without a library. It also allows import of linked VHDL files and the import of a source folder containing duplicate modules.

2.2.4 Netlist Viewer Enhancements

The Netlist Viewer has been enhanced with the addition of these new features:

- Mixed Verilog and VHDL source file support
- Maximize Display Area
- Hide/Show Design Tree
- Support empty spaces in project path

See UG0717 Netlist Viewer User Guide for details.

2.2.5 Row-Global Resources Option for Design Blocks

Libero SoC v11.8 SP1 introduces a Row-Global Resources option for design block creation. This option allows the user to specify the number of row-global resources in every half-row available to a design block (to be re-used later in a top level design in bottom-up design methodology). During Place and Route, the tool will not exceed this number on any half-row. The default value (8 for SmartFusion2/IGLOO2) is the maximum number of row-globals in every half-row. If you enter a value lower than the maximum capacity (the default), the layout of the block will be able to integrate with the rest of the design if they consume the remaining row-global capacity.

This option appears in the Layout Options dialog box (**Design Flow window > Place and Route > Configure Options**) only if Block Creation (**Project > Project Settings > Design Flow > Enable Block Creation**) is enabled.

To enable this option in Tcl commands, use the RGB_COUNT parameter as follows:

```
configure_tool  -name {PLACEROUTE}  -params {RGB_COUNT:6}  #use 6 Row-Globals in block
```

See the following documents for more information:

- Designing with Blocks in the Enhanced Constraint Flow User Guide
- Designing with Blocks in the Classic Constraint Flow User Guide

2.2.6 Globals and I/O Bank Assigner Enhancements

Globals and I/O bank assigner algorithms have been enhanced with the following features:

- RTG4 GRESET resource is now automatically assigned to the highest fanout asynchronous reset net, internal or external. Previously, the GRESET was assigned to a net driven from an I/O.
- RTG4 global network instance names now include the name of its source to improve traceability.
- RTG4 placer expands solution for single-ended SSTL/HSTL I/Os within differential pairs.
- RTG4 globals placer expands solution for hardened EPCS clocks generated from SERDES lanes.
- Enable timing-driven I/O register combining on both directions of BIBUF.
- Expand solutions when CCC requires default VREF pins.
- Exempt output I/O data pins from getting demoted from a global network.
- SmartFusion2/IGLOO2 globals placer now explores I/O connections to the global network through Virtual CCC (VCCC) only as a last resort.
- On failure, the I/O bank and Globals assigner will print a table of the most restrictive connections that could potentially have led to the failure.

2.2.7 SmartTime and Timing Analysis Enhancements

Constraint Coverage report

- False paths
- Tied-off register inputs
- SmartFusion2/IGLOO2 paths for "CLK_CONFIG_APB“

Multicycle path constraints

The multicycle factor on the hold side includes the setup multiplier factor. Example:

When a multicycle path constraint "set_multicycle_path -setup 2 - hold 0" is used in constraint editor, the -hold 0 doesn't mean "zero" cycle or 0 ns. It reflects the fact that hold is always checked one clock edge prior to setup edge. Hence, the hold will be checked at edge 1 (2-1-0=1).

2.2.8 Simultaneous Switching Noise (SSN) Enhancements

Pulse Width criteria for Noise Margin computation:

Previously, the SSN tool used 1 ns implicitly as the pulse width (settling time of the signal bounce) for signal noise computation. In Libero SoC v11.8 SP1, 0 ns and 1 ns are available as choices for the pulse width for noise margin computation. Changing the pulse width triggers re-generation of the noise margin report, which shows the pulse width value. The default value is 1 ns.

See the following documents for more information:

- Enhanced Constraint Flow User Guide
- Classic Constraint Flow User Guide

2.2.9 SmartDebug Enhancements

The following new features and enhancements are available in the Libero SoC v11.8 SP1 release.

Demo Mode

The Demo mode allows you to experience SmartDebug features (Active Probe, Live Probe, Memory Blocks, Debug SERDES) without the need to connect a board to the system running SmartDebug.

Note: The demo mode is for demonstration purposes only, and does not provide the full functionality of the integrated mode or standalone mode.

Note: You cannot switch between demo mode and normal mode while SmartDebug is running.

VCD file generated during FHB step function can be opened in ModelSim

Active Probes in SmartDebug supports bus names that are not continuous i.e. with non-contiguous signals added from the same bus (as in the example count_out_c[7:5,3:0], where count_out_c[4] is not included). This naming style is Microsemi-specific and is not supported in generic VCD viewers. To support generic VCD viewers, the probe name has been updated to count_out_c[7:0] where the 4^{th} bit count_out_c[4] is represented as 'x' in the generated *.vcd file generated during FHB step function.

Enhanced Memory Blocks sort options

The Memory Blocks sort options have been enhanced. Sorting can be done in ascending or descending order.

Tooltip on Logical view and physical view in Memory Blocks tab

A tooltip has been added to the logical view and the physical view in the Memory Blocks tab.

For more information, refer to the SmartDebug User Guide.

2.2.10 Script to Check System Packages (Linux systems only)

The Libero SoC v11.8 SP1 installation introduces a shell script to check the existence of runtime packages required to run Libero SoC on Linux systems. This script reports any packages that are required but are not installed in the system.

At the command shell window, run this script as follows:

% cd <Libero_installation> /bin/check_linux_req

% ./check_linux_req.sh

At the command shell window, install the required packages (root or sudo privileges required) as follows:

% yum install -y <package_name>

3 Resolved Issues

The following table lists the customer-reported issues resolved in Libero SoC v11.8 SP1.

Case Number	Descriptions
	Warning: device 'M2GL150T': Device authentication failure: Failed to validate Factory PUF ECC private key on device
493642-2146230106	Enable DAT file generation for RTG4
	Crash when exporting bitstream with lowercase speed grade
	SF2/IGLOO2: DEVICE_INFO fails
493642-2246913738, 493642-2260399698	Removal of VPP and TEMP fields from the programming log file
493642-2207770936	SET filter mitigation option is available in different locations for two constraints flow which is not documented
493642-2033249764	We have 3 different Tcl documents and all missing descriptions of -adv_options
	UEK3 is only available for high-end SF2 "S" devices only
	SPM: Auto Programming doesn't affect Programming Recovery
493642-2263280761	Libero export bitstream file path does not support "@" character
493642-2259121812	Block flow: Enhancement to Router to release fixed routing
	Lack of control over windows such as log and Design View and lack of menu entries
	Netlist Viewer should have Maximize Work Area option
	Highlighted bit in a bus gets un-highlighted when scrolling
	Netlist Viewer: Option to make tree selections not affect View
	SmartDebug should launch even if there is no hardware connected
493642-2216200089	Output drive strength for ProASIC3
493642-2221332135	Libero Help still refers -flash_freeze NO OPTION
	"Insufficient device capabilities" error when trying to program SF bitstream to IGLOO2
	Tcl Cmds: incorrectly a command says it doesn't support IGLOO/ProASIC3 device
	Typo in FlashPro5 3.3V DC Electrical Specs
493642-2100312938	Request to update Libero Online Help document - Adding user templates requires additional steps not mentioned in Help doc
493642-2241533194	Need to enhance SmartDebug documentations
	FP UG 11.8 lists out of date steps for Device Serialization
493642-2202001346	XAUI_TX_OOB port is not related to XAUI mode
493642-2279251730	I/O register combining Rule
493642-2202001346	Incorrectly exposed XAUI_TX_OOB port in XAUI mode
493642-2244741888	ODT restriction not clear
493642-2185477264	Using -Clock fall switch in set clock to output throws error

493642-2175754949	Use of -max/min switch after clock switch in set_output_delay is incorrect.
493642-2250697138	RTG4: Information related to BA macros should be added
493642-2249650203	Timing constraints created by Enhanced flow not compatible with SynplifyPro
493642-2297285906	Back annotated netlist file does not mention the version number
	Constraint coverage shouldn't report false-paths as unconstrained
	RTG4 P&R invalid timing constraint with '*' generates bad timing constraints
493642-2309596991, 493642-2289658196	Inter-clock domain missing in analysis
493642-2134957879	Constraint coverage report shows lot of unconstrained paths for "CLK_CONFIG_APB"
493642-2136636764	Hold value "0" is not taken for timing analysis by SmartTime tool
493642-2261205568	Derive constraints for unnamed Verilog generate blocks
493642-2152360759, 493642-2190745234	Timing constraints coverage - Enhancement Suggestions
	opening a user set for edit should re-open with same settings as created
	inter-clock domain missing in analysis
	Constraint coverage reports tied-off register inputs as unconstrained
	VCD generated from SmartDebug cannot be opened in ModelSim
	UEK3 is only available for G4X "S" devices only
	SPPS: Auto Programming shouldn't affect Programming Recovery
	Fix SPI export when Fabric/eNVM are protected by UPK1
493642-2241459808	RTG4 - Simulation of FPLL-LOCK is unstable in DDR interface when using 120MHz as base clock.
493642-2249006892	Enhancement Request: Memory Block should have filter option
	Crash - Click on "select" for memory Blocks crashes SmartDebug
493642-2299633598	Placer error related to global nets (RTG4)
	Error message when RGRESET is driven with more than 17 GB is not informative
	Libero Crash when Importing HDL
493642-2321792016	Libero crashes when VHDL file is linked
	Libero crashes with VHDL entity without library qualifier
493642-2266013245	Importing VHDL to Libero SoC v11.8 crashes the tool
	Issue with Verilog include files
493642-2258576960	Verify Power failed with Internal Error for specific design
493642-2288909211	PLL_VDDA power supply setting is not reflected in the Verify Power
	VFG400 package support for SSN Analyzer
	Progmode pin in FlashPro hardware is not toggling while executing SPI slave execution

493642-2244822351, 493642-2296006566	SmartPower crashes when trying to open interactively - EDN flow
	SmartPower and On board power is showing noticeable difference in Total Power
Boeing	SmartTime analysis doesn't show falling edge clock for DDR
493642-2190774145	SmartTime takes very long to open up
	Avoid MSS and System Builder automatic instantiation in a SmartDesign
493642-2275110024, 493642-2296774230	Linked Files added to a VHDL Library - Smart Design has component Missing
493642-2287292179	Library not invoked in generated VHDL file when files are linked
	Enhancement in cross probing from SmartTime to Chip Planner
	River routing data needs to be updated
493642-2144545950, 493642-2193476433	Tcl command for Generate component
	Libero hangs after synthesis of SF2 design containing encrypted Verilog + Identify
	Clean up import/generate components (CXF) commands
	Crash during SmartDesign generation
493642-2283603851	Block flow: Question on row globals with block flow
493642-2259121812	Block flow: Enhancement to Block Flow - To improve RGBs usage
	Block flow: preserving row globals fails placement
493642-2283032412	Block flow: RTG4 Placement Failure with Block Flow
	Compile Report Needs to show source net(s) driving rgreset_inst
	Block flow: Remove RGBs from the block to make it easy to find a solution in the top design
	Block flow: keeps the interface buffers in the published block
493642-2259121812	Block flow: Placer failed.
493642-2272990492	RTG4 comps.v vs comps.vhd
493642-2284071623, 493642-2310791544	RTG4 Error: No solution was found which could accommodate the global nets (and their drivers)
	Data update needed for IOD for all SF2 devices
493642-2204357010	M2S060T-FG676I per-pin parasitics not included in IBIS model
493642-2325059646, 493642-2329412360	SF2 layout crashes in Global Net Report
	I/O register: BIBUF I/Os combines registers only in one direction

4 Design Migration

Take note of the following issues when a project created with a release on or before Libero SoC v11.8 is first opened in Libero SoC v11.8 SP1.

4.1 SmartFusion2/IGLOO2 and RTG4 Timing Data Updates

There have been timing data updates to SmartFusion2/IGLOO2 devices after the release of Libero SoC v11.8.

- PCN17027.1 Timing Data Adjustments for a Subset of Fabric to Custom Block Interconnect

There have been timing data updates to the RT4G150 device after the release of Libero SoC v11.8.

- PCN17026.4 Updated Register Timing When Using SET Filter
- PCN17026.5 Timing Data Adjustments for a Subset of Fabric to Custom Block Interconnect
- PCN17026.6 SpaceWire Recovered Data Rate

When a design that has completed Place and Route in a prior release is first opened in Libero SoC v11.8 SP1, there is no design state invalidation.

- Microsemi recommends rerunning timing analysis in Libero SoC v11.8 SP1. If there is no timing violation, no action is required. If rerunning timing analysis in Libero SoC v11.8 SP1 results in timing violations, rerun Place and Route and then Timing Analysis to ensure that there are no timing violations. If timing violations still occur, call Microsemi Technical support for help.

4.2 SmartFusion2/IGLOO2 Bitstream Change

Libero SoC v11.8 SP1 eliminates an I/O glitch at the start of programming a blank SmartFusion2/IGLOO2 device. See PCN 17027.3 for details. When a design that has completed Place and Route in a prior release is first opened in Libero SoC v11.8 SP1, there is no design state invalidation.

- Regenerate the bitstream for programming.

4.3 RTG4 On-Die-Termination (ODT) Change

Libero SoC v11.8 SP1 disables ODT for LVDS33, BusLVDS, and MLVDS I/O standards. See PCN 17026.1 for details. Refer to the RTG4 I/O User Guide and RTG4 Datasheet for correct termination and common mode recommendations to achieve optimal jitter performance.

- When a design has I/Os with ODT enabled on one of these I/O standards and created in a prior release, is first opened in Libero SoC v11.8 SP1, the Generate Programming step is invalidated.
- If the pre-existing design contains I/Os using the ODT for LVDS33 I/O standards for High Speed Serial Interfaces (e.g. the REFCLK I/O has ODT and is on LVDS33 I/O standard), the configuration is no longer supported in this release. The SERDES component needs to be corrected. To continue the design flow in this release, all components, including the SERDES, need to be regenerated.

4.4 RTG4 Power Data Updates

There have been power data updates to the RT4G150 device after the release of Libero SoC v11.8.

- Differential I/Os

When a design that has completed Place and Route in a prior release is first opened in Libero SoC v11.8 SP1, there is no design state invalidation.

- Rerun power analysis in Libero SoC v11.8 SP1.

4.5 RTG4 -CQ352M Package Updates

A package update to the RTG4 CQ352M package after the release of Libero SoC v11.8 removed two MSIO pins (pin #214 and #215) as User I/O pins and therefore unavailable for user I/O assignment. Refer to the latest pin assignment table for the correct pin assignment for this package.

- All existing designs created in prior releases using this package, regardless of whether these two I/Os are used as User I/Os in the design or not, will be invalidated when the project is first opened in Libero SoC v11.8 SP1. On opening the project, a pop-up informational window alerts you to the invalidation. The design state reverts to the pre-synthesis state (for Enhanced Constraint Flow) or the pre-compile state (for Classic Constraint Flow). Make pin re-assignment, if necessary. To continue with the design flow, rerun synthesis (for Enhanced Constraint Flow) or compile (for Classic Constraint Flow).

4.6 RTG4 SmartGen Core Changes

The following RTG4 SgCores have been updated to be compatible with Libero SoC v11.8 SP1. If an existing project contains any of the following cores, you should update the core to the latest version and regenerate the component before continuing with the design flow.

Core	Version	Changes
RTG4UPROM	v1.0.106	Added client for RAM Initialization to zero. User must add at least one client to the system. Copy memory file to project path default to current project directory.
RTG4FCCCAPB_IF	v1.1.108	Hold violation between Dynamic CCC and APB.
PCIE_SERDES_IF_INIT	v1.0.110	Changed title from "*RTG4 High Speed Serial Interface – PCIe, EPCS and XAUI - with Initialization*" to "*RTG4 High Speed Serial Interface 1 - EPCS and XAUI - with Initialization*".
NPSS_SERDES_IF_INIT	v1.0.110	Changed title from "*RTG4 High Speed Serial Interface - EPCS and XAUI - with Initialization*" to "*RTG4 High Speed Serial Interface 2 - EPCS and XAUI - with Initialization*".

5 Known Limitations, Issues and Workarounds

Note: Unless stated otherwise, known issues from Libero SoC v11.8 also apply to Libero SoC v11.8 SP1. Review the Libero SoC v11.8 Release Notes for Known Issues in Libero SoC v11.8.

5.1 Error Message from FlashPro Express

The error message
`HSM operation g4GetAuthCode failed: GetAuthCode call HSM SEE failed : Error Code (16): 'Failed' - Command failed Error code #1009`

appears during ERASE when all of the following are true:

- FlashPro Express is used for programming larger SmartFusion2/IGLOO2 devices (M2S/M2GL060, M2S/M2GL090, and M2S/M2GL150)
- Asymmetric keymodes are used along with HSM
- Programming actions are run in this sequence: PROGRAM, PROGRAM, and ERASE.

Workaround:

Close and open FlashPro Express again and run ERASE again.

5.2 File > Print Report Options on RHEL 7.1 Causes Tool to Crash

When the Print Report option is invoked from the Libero SoC File menu, Libero SoC crashes. The same behavior occurs on Simultaneous Switching Nose (SSN) and SmartTime. This error message originates from the Qt library on which the tool is based.

5.3 Generate Bitstream Fails if FlashPro Profile becomes Unset

If the FlashPro tool profile becomes unset when switching between different releases of the Libero SoC software, Generate Bitstream fails.

5.4 Warning Message During Bitstream Generation/Programming

A warning message **Untested Windows version 6.2 detected!** appears in the Libero SoC Log window during Bitstream Generation on Windows 8 and Windows 10 machines. This warning message originates from the Qt Library on which the bitstream generation tool is based. This message is benign and can be safely ignored.

5.5 SmartDebug – Demo Mode

SmartDebug in standalone mode does not support demo mode without FlashPro programmer connected to the machine and SmartDebug invoked.

5.6 SmartDebug – Empty Popup Window on Windows 10 Operating Systems

An empty popup window appears when SmartDebug is invoked in standalone mode on Windows10 machines.

5.7 SmartDebug – Logical View for LSRAM/uSRAM Known Issues

- The logical view cannot be reconstructed for LSRAM/uSRAM with port width of x1 inferred through RTL.
- The logical view cannot be reconstructed for LSRAM/uSRAM configurations when a single net of the output bus is used, i.e. A_DOUT[0]/B_DOUT[0] for DPSRAM/uSRAM and RD[0] for TPSRAM and others are unused. The memories can be read/write using the physical view.
- The logical view cannot be constructed for the RAM blocks that are generated through nested SmartDesigns.
- The logical view cannot be reconstructed for LSRAM/uSRAM configurations inferred using IP Cores CoreAHBLtoAXI (Verilog flow), and CoreFIFO (Verilog and VHDL flow)
- The logical view width of LSRAM/uSRAM ports is incorrect when a sliced portion of the output port is promoted to the top level and the sliced portion contains the Most Significant Bit (MSB) of the output port.

5.8 SmartDebug – FPGA Hardware Breakpoint (FHB) Auto Instantiation Limitations

- Support is limited to SmartFusion2 and IGLOO2 devices in the Enhanced Constraint Flow only.
- Support is limited to FABCCC driven gated clocks.
- There is no support for EDIF flow and designs having Encrypted IPs.
- Live Probe triggering is limited to the positive edge only.
- When a signal connected to logic zero/ground (1’b0) is used as the live probe trigger, disarming the trigger leads to the forced halt of Device Under Test (DUT).
- The FHB auto instantiation feature is not supported for the block flow.

5.9 FlashPro3/4/5 and VPUMP

Users need to connect VPUMP of SmartFusion2, IGLOO2, and RTG4 devices to the programmer's (FlashPro3/4/5) VPUMP pin to program the device.

This applies to Libero, FlashPro, and FlashPro Express for v11.8 SP1 and before.

5.10 SSN Results Not For Silicon Sign-Off

Simultaneous Switching Noise (SSN) is a noise analysis tool for SmartFusion2 and IGLOO2. The noise margin reported by the SSN Analyzer is computed based on the I/O standards, Drive Strength, and placement of the pin. The SSN Analyzer provides a general guideline and helps the designer to achieve the desired voltage noise margin. It is not intended to be used as a silicon sign-off tool.

5.11 Programming and Debug Reference Manuals

The Programming and Debug Tools Documentation Catalog (Reference Manuals) links open the v11.8 versions of these documents: SmartDebug User Guide, FlashPro User Guide, and FlashPro Express User Guide.

Click the following links to access the v11.8 SP1 versions of the documents:

SmartDebug User Guide

FlashPro User Guide

FlashPro Express User Guide

5.12 Core Configurator User Guides Not Opening on Windows 8 and Windows 10 Machines

Some core configurator user guides (CCC Configurator > Help > User Guide, TAMPER configurator > Help > User Guide, MSS_INTR Configurator > Help > User Guide) are not opening PDF files on Windows 8 and Windows 10 machines. All core configurator user guides open on Windows 7 machines.

5.13 Installation

C++ installation error can be ignored. Required files will install successfully.

On some machines, the InstallShield wizard displays a pop-up message stating:

The installation of Microsoft Visual C++ Redistributable Package (x86) appears to have failed. Do you want to continue the installation?

Click **Yes** to complete the installation.

5.14 Antivirus Software Interaction

Many antivirus and host-based intrusion prevention system (HIPS) tools flag executables and prevent them from running. To eliminate this problem, users must modify their security settings by adding exceptions for specific executables. This is configured in the antivirus tool. Contact the tool provider for assistance.

Many users are running Libero SoC successfully with no modification to their antivirus software. Symantec, McAfee, Avira, Sophos, and Avast tools have known issues. The combination of operating system, antivirus tool version, and security settings all contribute to the end result. Depending on the environment, the operation of Libero SoC, ModelSim ME, and/or Synplify Pro ME may or may not be affected.

5.15 SPPS: Job Manager Fails when Back Level Protection is ON

When using Job Manager, if the JDC or SPM file has Back Level protection ON (in Update Policy), Job Manager fails during bitstream generation. It fails when running the "export_hsmtask" or "export_bitstream_file" Tcl commands.

5.16 SPI Slave Programming Fails on SmartFusion2 and IGLOO2 Devices

SPI Slave Programming fails in Libero SoC v11.8 SP1 on SmartFusion2 and IGLOO2 devices.

Workaround:

Use Libero SoC v11.8 or JTAG interface for programming.

5.17 SPPS: set_hsm_params Not Updating HSM Server Address

If Job Manager or FlashPro Express is open and the HSM server name/address is changed via set_hsm_params, Job Manager or FlashPro Express will continue to use the previous HSM server name/address.

Workaround:

Close and open Job Manager or FlashPro Express.

6 System Requirements

For information about operating system support and minimum system requirements, see the System Requirements web page.

Note: A 64-bit OS is required for designing with SmartFusion2, IGLOO2, and RTG4 devices.

For Linux OS setup instructions, see How to Set Up Linux Environment for Libero User Guide.

6.1 Operating System Support

Supported

- Windows 7, Windows 8.1, Windows 10
- RHEL 5*, RHEL 6, RHEL 7, CentOS 5*, CentOS 6, and CentOS 7
- SuSE 11 SP4 (Libero only. FlashPro Express, SmartDebug, and Job Manager are not supported.)

Note: * RHEL 5 and CentOS 5 do not support programming using FlashPro5.

Not Supported

- 32-bit operating system
- Windows XP
- Support for the following operating systems will cease in the second half of 2017:
  - RedHat Enterprise Linux 5.x through 6.5
  - CentOS 5.x through 6.5

7 Libero SoC v11.8 SP1 Download

Click the following links to download Libero SoC v11.8 SP1 on Windows and Linux operating systems:

- Windows Download
- Linux Download
- Mega Vault Download

Note: Installation requires administrator privileges to the system.

Libero SoC v11.8 SP1 is an incremental service pack and must be installed over Libero SoC v11.8.

7.1 Downloading SoftConsole 3.4/4.0/5.1

Libero SoC v11.8 SP1 is compatible with SoftConsole v3.4 SP1 and SoftConsole v4.0/5.1. The following links contain the download packages, and explain the steps for downloading SoftConsole on different operating systems:

- Download SoftConsole v4.0 for Windows
- Download SoftConsole v4.0 for Linux
- Download SoftConsole v3.4 SP1 for Windows
- Download SoftConsole v5.1 for Windows
- Download SoftConsole v5.1 for Linux