Libero SoC v11.8 Service Pack 2

Release Notes

11/2017

Microsemi
Power Matters.™

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Fax: +1 (949) 215-4996
Email: **sales.support@microsemi.com**
www.microsemi.com

About Microsemi
Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions; security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, California, and has approximately 4,800 employees globally. Learn more at **www.microsemi.com**.

51300187-1/11.17

Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision 1.1

Added Known Issue 4.3 Cannot Set the TCK above 4MHz in Single Mode.

Revision 1.0

Revision 1.0 is the first publication of this document.

Contents

1 Libero SoC v11.8 SP2 Release Notes

The Libero® system on chip (SoC) v11.8 SP2 release is a service pack release of the Libero SoC v11.8 software for designing with Microsemi's power efficient flash FPGAs, SoC FPGAs, and rad-tolerant FPGAs. The suite integrates industry standard Synopsys Synplify Pro® synthesis and Mentor Graphics ModelSim® simulation with best-in-class constraints management, debug capabilities, and secure production programming support.

Use Libero SoC v11.8 SP2 for designing with Microsemi's RTG4 Rad-Tolerant FPGAs, SmartFusion®2 and SmartFusion® SoC FPGAs, and IGLOO® 2, IGLOO®, ProASIC® 3, and Fusion FPGA families.

To access datasheets, silicon user guides, tutorials, and application notes, visit www.microsemi.com, navigate to the relevant product family page, and click the **Documentation** tab. Development Kits & Boards are listed in the **Design Resources** tab.

Libero SoC v11.8 SP2 addresses specific bugs introduced in previous releases, and provides workarounds for certain silicon configurations which are no longer recommended. This release only affects SmartFusion2, IGLOO2, and RTG4 families. Users of other Microsemi FPGA families do not need to upgrade to Libero SoC v11.8 SP2.

Additional Reference Sources:

Read the following Customer Advisory Notifications (CAN) before using Libero SoC v11.8 SP2:

- SmartFusion2/IGLOO2 Vref OE input tie off invalid (CAN 17036.1)
- SmartFusion2/IGLOO2 IO Output and Output enable inversion (CAN 17036.2)
- RTG4 Vref OE input tie off invalid (CAN 18002.1)
- RTG4 IO Output and Output enable inversion (CAN 18002.2)
- RTG4 LSRAM Timing Marginality (CAN 18002.3)

2 What's New in Libero SoC v11.8 SP2

2.1 Software Enhancements/Changes

When you open a pre-v11.8 SP2 project with Libero SoC v11.8 SP2, the software will check the design to see if it is affected by any of the issues mentioned in CAN 17036 and CAN 18002. The design state may automatically be invalidated if the design is affected.

SmartFusion2/IGLOO2/RTG4 Vref Output Enable Tie-off (CAN 17036.1, CAN 18002.1)

If your pre-Libero v11.8 SP2 design contains a Vref-related I/O constraint that is invalid, upon opening it with Libero SoC v11.8 SP2:

- Classic Constraint Flow: Compile will be invalidated.
- Enhanced Constraint Flow: Synthesis will be invalidated.
- In both cases, the Libero log window will print a list of IO pairs that are affected.

User Action: You must change your I/O constraints (edit your PDC file, or use the I/O Editor) to prevent the case where a VREF pin is assigned to the P side of a differential I/O pair, and an output, BIBUF or TRIBUFF is assigned to the N side of the same pair. Resolve the error by either moving the Vref assignment to another pin on the I/O bank, or by moving the output assigned to the N-side. Then rerun the invalidated step and the subsequent downstream design flow.

SmartFusion2/IGLOO2/RTG4 I/O Output Data and Output Enable Inversion CAN 17036.2, CAN 18002.2

If your Libero v11.8 SP1 design contains an invalid inversion on any I/O Output data or Output enable path, upon opening it with Libero SoC v11.8 SP2:

- Place & Route will be invalidated and the Log Window will show the message:
  "Your design '…' contains IO-Register combinations which need to be updated. Please re-run Place and Route."

User Action: Rerun the Place & Route step and the subsequent downstream design flow.

RTG4 LSRAM Timing Marginality (CAN 18002.3)

If your pre-Libero v11.8 SP2 design contains an LSRAM configuration that is affected by this issue, upon opening it with Libero SoC v11.8 SP2:

- Classic Constraint Flow: Compile will be invalidated.
- Enhanced Constraint Flow: Synthesis will be invalidated.
- In both cases, the Libero log window will print a list of LSRAM configurations that have been affected.

User Action:

- If your design contains the Two-Port Write x9, Read x36 configuration that has been deprecated, you must adjust the construction/functionality of the design to utilize another RAM block configuration. This can be achieved by using the LSRAM configurator, by inferring a different sized RAM, or inferring RAM which is mapped to fabric registers. There is no equivalent configuration available for any Write:Read ratio of 1:4. Contact Microsemi Technical Support for more information.
- If your design contains Dual-Port x12 blocks, you must reopen the Dual-Port LSRAM Configurator component that corresponds to these blocks and regenerate. Note that one component may contain multiple LSRAM blocks. The REN functionality may no longer be feasible with depth cascading. See section 4.2 below for a known depth limitation of the Dual-Port LSRAM Configurator.
- In all other cases, Compile (Classic flow) or Synthesize (Enhanced Constraint flow) will automatically remap LSRAM blocks to address the issues.
- Rerun the subsequent downstream design flow.

3 Resolved Issues

The following table lists the customer-reported issues resolved in Libero SoC v11.8 SP2.

Case Number	Description
493642-2322705823	Detect use cases affected by the Vref OE IO config issue
493642-2322705823	Clean up unnecessary Vref (provisioned by IOBA) at the end of P&R
493642-2322705823	IOBank Assigner assigns T4 pin in bank7 as Vref (1.0V)
493642-2341717917	SmartFusion2 Export IBIS Model crashes for customer design
493642-2351636631, 493642-2352260976, 493642-2367510956	IOOEFF behavior is different in v11.8 SP1
	IO-FF combining issue in v11.8 SP1 (CAN 18002.2)
	SmartFusion2 SPPS: Job Manager fails when Back level protection is ON
	RTG4 SPI Slave programming interface should be disabled
	Detect infeasible regions for carry chains

4 Known Limitations, Issues and Workarounds

Note: Unless stated otherwise, known issues from Libero SoC v11.8 and v11.8 SP1 also apply to Libero SoC v11.8 SP2. Review the Libero SoC v11.8 Release Notes and Libero SoC v11.8 SP1 Release Notes for Known Issues in Libero SoC v11.8 and v11.8 SP1.

4.1 Standalone Programming and Debug Tools

No changes in FlashPro, FlashPro Express, SmartDebug, or Job Manager standalone tools have been made in Libero SoC v11.8 SP2. As a result, if you are using the standalone versions of these tools, you can continue to do so. You can use Libero SoC v11.8 SP2 software to generate programming files, job files, or SmartDebug ddc files, and use the standalone v11.8 SP1 versions of the respective tools to work with the generated files.

4.2 RTG4 Dual-Port LSRAM Configurator Depth Limit

Due to the changes made to the supported RTG4 Dual-Port LSRAM configurations, per CAN 18002.3, it is now possible to reach a known depth limit. Currently, the RTG4 Dual-Port LSRAM configurator does not allow cascading for more than 32 LSRAM blocks deep. Possible workarounds include:

- Inferring the deeper dual-port RAM via synthesis.
- Using the LSRAM configurator to generate sub-blocks which can then be depth cascaded manually. For example, a 64K x 18 dual-port memory can be created by using two smaller 32K x 18 dual-port LSRAM components and manually cascading them depth wise in SmartDesign or HDL.

4.3 Cannot Set the TCK above 4MHz in Single Mode

In Libero SoC v11.8 and later releases, you cannot set the TCK above 4MHz in single mode.

Workaround:
Use chain mode to set the TCK above 4MHz.

5 System Requirements

For information about operating system support and minimum system requirements, see the System Requirements web page.

Note: A 64-bit OS is required for designing with SmartFusion2, IGLOO2, and RTG4 devices.

For Linux OS setup instructions, see How to Set Up Linux Environment for Libero User Guide.

5.1 Operating System Support

Supported

- Windows 7, Windows 8.1, Windows 10
- RHEL 5*, RHEL 6, RHEL 7, CentOS 5*, CentOS 6, and CentOS 7
- SuSE 11 SP4 (Libero only. FlashPro Express, SmartDebug, and Job Manager are not supported.)

Note: * RHEL 5 and CentOS 5 do not support programming using FlashPro5.

Not Supported

- 32-bit operating system
- Windows XP
- Support for the following operating systems will cease after December 2017. For more information, refer to PCN17031.
    - RedHat Enterprise Linux 5.x through 6.5
    - CentOS 5.x through 6.5

6 Libero SoC v11.8 SP2 Download

Click the following links to download Libero SoC v11.8 SP2 on Windows and Linux operating systems:

- Windows Download
- Linux Download
- Mega Vault Download

Note: There are no new cores for the Libero SoC v11.8 SP2 release, and all Libero SoC v11.8 SP1 cores are compatible with v11.8 SP2. The v11.8 SP1 Mega Vault location should be used for this release.

Note: Installation requires administrator privileges to the system.

Libero SoC v11.8 SP2 is an incremental service pack and must be installed over Libero SoC v11.8 or v11.8 SP1.

After successful installation, clicking **Help-> About Libero** will show Version: 11.8.2.4.

6.1 Downloading SoftConsole 3.4/4.0/5.1

Libero SoC v11.8 SP2 is compatible with SoftConsole v3.4 SP1, SoftConsole v4.0 and SoftConsole v5.1. The following links contain the download packages, and explain the steps for downloading SoftConsole on different operating systems:

- Download SoftConsole v5.1 for Windows
- Download SoftConsole v5.1 for Linux
- Download SoftConsole v4.0 for Windows
- Download SoftConsole v4.0 for Linux
- Download SoftConsole v3.4 SP1 for Windows