Libero SoC v11.8 Service Pack 3

Release Notes

02/2018

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Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision 1.0

Revision 1.0 is the first publication of this document.

Contents

1 Libero SoC v11.8 SP3 Release Notes

The Libero® system on chip (SoC) v11.8 SP3 release is a service pack release of the Libero SoC v11.8 software for designing with Microsemi's power efficient flash FPGAs, SoC FPGAs, and rad-tolerant FPGAs. The suite integrates industry standard Synopsys Synplify Pro® synthesis and Mentor Graphics ModelSim® simulation with best-in-class constraints management, debug capabilities, and secure production programming support.

Use Libero SoC v11.8 SP3 for designing with Microsemi's RTG4 Rad-Tolerant FPGAs, SmartFusion®2 and SmartFusion® SoC FPGAs, and IGLOO® 2, IGLOO®, ProASIC® 3, and Fusion FPGA families.

To access datasheets, silicon user guides, tutorials, and application notes, visit www.microsemi.com, navigate to the relevant product family page, and click the **Documentation** tab. Development Kits & Boards are listed in the **Design Resources** tab.

Libero SoC v11.8 SP3 implements several customer-reported enhancements and bugfixes focusing on the RTG4, SmartFusion2, and IGLOO2 FPGA and SoC families.

Additional Reference Sources:

- SmartFusion2/IGLOO2: Bitstream Corruption with "S" Devices (CAN 17036.3)

2 What's New in Libero SoC v11.8 SP3

Libero SoC v11.8 SP3 implements several enhancements and bug fixes

2.1 SmartFusion2/IGLOO2: Bitstream Corruption with "S" Devices (CAN 17036.3)

You must regenerate the bitstream before programming any SmartFusion2 or IGLOO2 "S" device over the JTAG port or the dedicated system controller SPI port. A short dummy FPGA bitstream component that places the FPGA fabric in verify mode before bitstream programming has been added and prevents the collision. This will increase the programming time by 2-3 seconds. DirectC is also updated.

User Action: Open your design in Libero SoC v11.8 SP3 and regenerate the bitstream.

2.2 RTG4: Bitstream Detection of DEVRST_N Assertion During Programming

It is not recommended to drive DEVRST_N low while programming any RTG4 device. While programming with STAPL files generated during earlier releases, if the DEVRST_N was asserted, programming would silently fail. Libero SoC v11.8 SP3 will generate STAPL and DirectC files that will detect the state of DEVRST_N during programming.

User Action: To obtain a STAPL that detects DEVRST_N assertion, open your design in Libero SoC v11.8 SP3 and regenerate the bitstream.

2.3 RTG4: SRAM ECC Simulation

Libero SoC v11.8 SP3 supports two additional simulation options [Project Settings->Simulation Options->Vsim commands] to stimulate the ECC flags of all SRAM blocks in an RTG4 design.

- -gERROR_PROBABILITY=<value>, where 0 <= value <= 1
- -gCORRECTION_PROBABILITY=<value>, where 0 <= value <= 1

During simulation, the SB_CORRECT and DB_DETECT flags on each SRAM block will be raised based on generated random numbers being below the above values.

2.4 Simultaneous Switching Noise (SSN)

With this release, SSN analysis is now supported for the following device-package combinations:

- M2GL150-FCG1152
- RT4G150-CG1657
- RT4G150-CQ352

2.5 IBIS Support Enhancements

Design-specific IBIS export is added for all RTG4 devices in this release.

2.6 RTG4 One Time Programmable Feature

Libero SoC v11.8 SP3 supports the One Time Programmable configuration option for RTG4 devices. Users requiring enhanced levels of security can now configure their device to prevent reprogramming. After programming a device with this option enabled, further erase or reprogram actions will not be possible. You will be able to run VERIFY, VERIFY_DIGEST and DIGEST requests. Export bitstream and programming actions will pop up a warning when this option is enabled.

2.7 FlashPro3/4/5 VPUMP Sensing

Starting with Libero SoC v11.8 SP3, for SmartFusion2/IGLOO2/RTG4 devices, FlashPro software/hardware will not sense/drive VPUMP. However, if any ProASIC3/IGLOO/Fusion/SmartFusion device is detected in chain, then FlashPro will drive/sense VPUMP.

- FlashPro will not detect VPP if the board contains only SmartFusion2/IGLOO2/RTG4 devices. Leave the VPUMP pin of the JTAG header floating if the board has only SmartFusion2/IGLOO2/RTG4 devices.
- If the board contains ProASIC3/IGLOO/Fusion/SmartFusion devices along with SmartFusion2/IGLOO2/RTG4 devices in the JTAG chain, connect VPUMP of the ProASIC3/IGLOO/Fusion/SmartFusion device to the JTAG header's VPUMP pin.

2.8 SmartFusion2/IGLOO2/RTG4: Placer Enhancements for Physical Regions

The placer in Libero SoC v11.8 SP3 for SmartFusion2/IGLOO2/RTG4 devices will now print a table of infeasible regions when there is no placement solution possible for fabric cells such as MATH, SRAM, Carry-chain or Logic.

2.9 RTG4: I/O Bank Assigner Enhancements

The automatic I/O Bank Assigner in Libero SoC v11.8 SP3 for RTG4 devices will prefer MSIO and MSIOD banks for hardwired connections to Globals or CCC. Assignments to DDRIO banks, which are not Single-Event Transient (SET) mitigated, will be made as a last resort. Check the Warning section in the Global Net report after running Place and Route.

2.10 RTG4: Repair Minimum Delay Violations Enhancements

The automatic Repair Minimum Delay Violations step in Libero SoC v11.8 SP3 for RTG4 devices will not enable programmable input delays for any I/O on MSIO and MSIOD banks if it drives a global.

3 Resolved Issues

The following table lists the customer-reported issues resolved in Libero SoC v11.8 SP3.

Case Number	Description
493642-1816608745	Block_Flow : BIF: HDLPLUS: Block created for a HDLPLUS design does not retain more than one BIF in the published block
493642-2064667568	Enable simulation of ECC behavior for RTG4
493642-2163243750	RTG4-IBIS: Common mode issue with LVDS IBIS model
493642-2220662408	Block_Flow BIF: AHB Interface bus is not maintained
493642-2245787766, 493642-2345690745, 493642-2365270359, 493642-2372578272	Create ViewDraw symbol throws error
493642-2259463170, 493642-2260203623, 493642-2269362563	Add SSN Analyzer tool for RTG4
493642-2275801276, 493642-2263027456	Add M2S/M2GL 150-FCG1152 to SSN Analyzer
493642-2298490334	Issue with Chip Planner when using generated constraints
493642-2316277871	RTG4: BiDir HSTL15 ODT_STATIC IBIS model
493642-2342926784	Clock_fall error when used as argument for set_external_check
493642-2343019579	RTG4: enhance STAPL to detect DEVRST_N assertion and abort programming
493642-2351836351	RTG4: Add One Time Programmable feature
493642-2354899639	Remove SPI Slave pin reservation for programming
493642-2361905485, 493642-2371188804	Clock Generation value 0 for generated clock
493642-2377255106	RTG4: Truth table and block diagram for GBR and RGB are not correct
493642-2379806960	Placer failure message is insufficient to fix the issue
493642-2389035713	RTG4: SmartPower does not show current for LVDS tribuf at tristate condition
493642-2400444793	Block Import crash in 11.8 SP2- Block has HPMS
	SF2/IGLOO2 SPI Slave Programming Fails
	Bidirectional DDR outputs timing analysis
	DOS window is present upon program launch
	RTG4 placer fails with little report info
	SmartPower incorrectly calculates DDR I/O power
	Archive function does not retain the /component/user folder
	RTG4 PLL Supply Voltage reported as 2.5V when it is 3.3V
	RTG4 incremental layout fails after a passing PAR
	Block_Flow: Some Macros will not place in region
	Chip Planner shows IP blocks in separate hierarchy
	FlashPro3/4/5 and Vpump
	Update Algo to workaround Silicon Issue (JTAG/SPI-Slave programming)

4 Known Limitations, Issues and Workarounds

Note: Unless stated otherwise, known issues from Libero SoC v11.8, v11.8 SP1, and v11.8 SP2 also apply to Libero SoC v11.8 SP3. Review the Libero SoC v11.8 Release Notes, Libero SoC v11.8 SP1 Release Notes , and Libero SoC v11.8 SP2 Release Notes for Known Issues in Libero SoC v11.8, v11.8 SP1, and SP2

4.1 FlashPro TCK cannot be set above 4MHz in single device mode

If the maximum TCK frequency is set above 4MHz in single device mode, it will be reset to 4MHz, and a warning message displayed. Set TCK at 4MHz or below, or use chain mode

4.2 SmartDebug: Live Probe not supported with UPK1

If the UPK1 key is set in a design, Live Probe assignment errors out in SmartDebug, with the error:

Error: Cannot set live probes: UPK1 unlock failed.

This issue is observed only while using the Live Probe feature. Other SmartDebug features work fine as long as the Live Probe action is not performed.

5 System Requirements

For information about operating system support and minimum system requirements, see the System Requirements web page.

For Linux OS setup instructions, see How to Set Up Linux Environment for Libero User Guide.

5.1 Operating System Support

Supported

- Windows 7, Windows 8.1, Windows 10
- RHEL 5*, RHEL 6, RHEL 7, CentOS 5*, CentOS 6, and CentOS 7
- SuSE 11 SP4 (Libero only. FlashPro Express, SmartDebug, and Job Manager are not supported.)

Note: * RHEL 5 and CentOS 5 do not support programming using FlashPro5.

Not Supported

- 32-bit operating systems
- Windows XP
- Support for the following operating systems will cease with the next major Libero SoC release. For more information, refer to PCN17031.
    - RedHat Enterprise Linux 5.x through 6.5
    - CentOS 5.x through 6.5

6 Libero SoC v11.8 SP3 Download

Click the following links to download Libero SoC v11.8 SP3 on Windows and Linux operating systems:

- Windows Download
- Linux Download
- Mega Vault Download

Note: There are no new cores for the Libero SoC v11.8 SP3 release, and all Libero SoC v11.8 SP1 cores are compatible with v11.8 SP3. The v11.8 SP1 Mega Vault location (linked above) should be used for this release.

Note: Installation requires administrator privileges to the system.

Libero SoC v11.8 SP3 is an incremental service pack and must be installed over Libero SoC v11.8, v11.8 SP1, or v11.8 SP2

After successful installation, clicking **Help-> About Libero** will show Version: 11.8.3.6.

6.1 Downloading SoftConsole 3.4/4.0/5.1

Libero SoC v11.8 SP3 is compatible with SoftConsole v3.4 SP1, SoftConsole v4.0 and SoftConsole v5.x

- SoftConsole Download