Libero SoC v11.9

Release Notes

09/2018

Microsemi
Power Matters.™

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Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision 1.2

Added text about unused PLL_ARST_N and PLL_POWERDOWN_N inputs in section 2.2 RTG4 PLL in Internal Feedback Mode (TMR Mode).

Revision 1.1

Added Known Issue 5.6 SmartFusion2/IGLOO2: I/O State During Programming settings are not propagated to the programming file and Generate Bitstream state is not invalidated.

Revision 1.0

Revision 1.0 was the first publication of this document.

Contents

1 Libero SoC v11.9 Release Notes

The Libero® system on chip (SoC) v11.9 is a full software release for designing with Microsemi's power efficient flash FPGAs, SoC FPGAs, and rad-tolerant FPGAs. The suite integrates industry standard Synopsys Synplify Pro® synthesis and Mentor Graphics ModelSim® simulation with best-in-class constraints management, debug capabilities, and secure production programming support.

Use Libero SoC v11.9 for designing with Microsemi's RTG4 Rad-Tolerant FPGAs, SmartFusion®2 and SmartFusion® SoC FPGAs, and IGLOO® 2, IGLOO®, ProASIC® 3, and Fusion FPGA families.

To access datasheets, silicon user guides, tutorials, and application notes, visit www.microsemi.com, navigate to the relevant product family page, and click the **Documentation** tab. Development Kits & Boards are listed in the **Design Resources** tab.

2 What's New in Libero SoC v11.9

Libero SoC v11.9 includes new features, enhancements, and bug fixes.

2.1 RTG4 Dual-Port Large SRAM Read-Before-Write Option Removed

RTG4 no longer supports the Read-Before-Write feature in the large SRAM (LSRAM). In the Dual-Port Large SRAM Configurator, the "*Read before Write*" option for the "*DOUT on Write*" feature has been removed.

For existing designs migrated to Libero SoC v11.9, upon opening the project, Libero SoC checks every LSRAM instance in the design for the usage of the Read-Before-Write feature. If the Read-Before-Write feature is detected during the Compile step (for Classic Constraint Flow) or the Synthesis step (for Enhanced Constraint Flow), an error message appears: "*Instance XYZ is configured to use read-before-write mode which is not supported*". To continue with the design process in the new release, you need to modify the design. Change the functionality that requires Read-Before-Write in the RTL source or in the component instances of the Dual-Port LSRAM Configurator.

See PCN18011.1 for more information.

2.2 RTG4 PLL in Internal Feedback Mode (TMR Mode)

A triple module redundant (TMR) PLL is used when the PLL Internal feedback mode is selected, while a single, non-TMR PLL is used when CCC Internal or External feedback modes are selected in the CCC configurator software. The RTG4 TMR PLL includes three sub-PLLs with a voted lock output to help mitigate single event effects in a radiation environment. When the PLL is configured for triple redundant configuration via the selection of PLL Internal feedback mode, it can experience a loss of lock which does not automatically self-recover and requires toggling the *PLL_ARST_N* reset input to regain lock. In Libero SoC v11.9, the RTG4 CCC configurator v1.1.226 introduces a fabric circuit which will monitor the TMR PLL voted lock signal when it is in PLL Internal feedback mode. This fabric circuit will automatically issue a reset command to the PLL if loss of lock is detected. The circuit requires a 50 MHz clock that is readily available from the on-chip RC oscillator. You need to instantiate the RCOSC_50MHZ macro and distribute its output through a GLx of any one CCC and eventually connect to the exposed CLK50_MHZ input pin of the CCC. The CCC connected to RCOSC_50MHZ could even be the same CCC as this one. When PLL Internal Feedback mode is selected, both PLL_ARST_N and PLL_POWERDOWN_N signals are always exposed to provide additional user access to these signals. The auto-reset circuit for the TMR PLL will still function even if the user connects the exposed PLL_ARST_N input to a logic-high because the circuit combines this user input with the status of the voted lock.

If the PLL_ARST_N and PLL_POWERDOWN_N inputs are unused in your design, these additional exposed ports can be tied to logic-high.

See PCN18009.7 for more information.

2.3 RTG4 LSRAM ECC Errors

In certain circumstances, RTG4 LSRAM can experience data corruption and ECC flag false positive indications. When RTG4 LSRAM blocks are configured in non-pipelined ECC mode, without SET mitigation enabled, a timing issue in the LSRAM ECC circuits can generate incorrect ECC code words and in turn allow read-back of falsely corrected data and flag outputs. Libero SoC v11.9 removes support for LSRAM non-pipelined ECC mode without SET mitigation. Libero SoC v11.9 also introduces features in the Dual-port LSRAM, Two-port LSRAM and uSRAM configurator to generate logic that gates-off ECC flags for inactive

RAM blocks and to ensure that simulation shows ECC flags as unknown when not in valid data out clock cycle or when BLK is de-asserted.

See PCN18009.1 for more information.

2.4 RTG4 Timing Changes

Silicon characterization has highlighted a need for an adjustment to the timing models for certain signal paths connecting programmable gates to the EPCS, SERDES and FDDR blocks. Additionally, signals derived from programming gates connecting to row global buffers (RGB) via local routing tracks are subject to a timing adjustment. Finally, the row global reset macro (*RGRESET*) which connects a fabric output to an asynchronous reset network is also subject to a timing change.

See PCN18009.6 for more information.

2.5 RTG4 CCC Simulation False Failures

The RTG4 simulation library model has been updated in Libero SOC v11.9 software to enhance the PLL modelling equation in cases where specific CCC configurations, coupled with cascaded PLLs, and simulator rounding effects can lead to clock distortion during simulation of the FDDR memory controller. Digital simulators will round to the nearest picosecond, and for example, this means that clock frequencies of 300MHz will have their periods truncated to 3.333 ns. Cascaded PLLs can cause the rounding effect on the clock period to accumulate. One example of this situation occurs when a fabric CCC provides a base clock for the FDDR which in turn generates the DDR clock for the memory interface. The simulation model tries to compensate for this effect using an equation to model the clock period and will periodically add extra time to stabilize the clock period and edge alignment of the output clock. Prior to v11.9, the simulation model equation did not correctly account for the contribution of one of the PLL output dividers which allowed the FDDR PLL clock to have a distorted clock period and duty cycle.

See CN18009.8 for more information.

2.6 RTG4 Synopsys Synplify Safe FSM Setting Change

The following options can be used to insert safe implementation logic:

- Attribute *syn_encoding* = safe
- Attribute *syn_safe_case*
- Enable the options under *Implementation Options -> High Reliability -> Preserve and Decode unreachable states*.

Synplify Pro L-2016.09M-SP1-5 issues the following error: "*Safe state machine option is not recommended for Microsemi RTG4 technology. To continue with safe state machine implementation, downgrade this error to warning*". You have the option to downgrade this error to a warning message, and Synplify Pro implements the safe logic for FSMs if these options are present.

See CAN18009.5 for more information.

2.7 SmartFusion2, IGLOO2 and RTG4 QoR Improvement

Place and Route algorithm advances in Libero SoC v11.9 show Quality of Results (QoR) improvement of 7% on average for large size designs (>88k LE).

2.8 RT4G150-CQ352

Libero SoC v11.9 introduces the -1 speed-grade for the RT4G150-CQ352 device.

Remote sensing is required for the RTG4150-CQ352 device to meet all device performance specifications. See the RTG4 document "DS0130 Datasheet - RTG4 FPGA Pin Descriptions", section 2.11 on the proper usage of the internal power supply sense pins – *VDD_MONITOR* and *VSS_MONITOR* that are provided for the RTG4150-CQ352 device to monitor the device's VDD and VSS planes.

2.9 RTG4 Additional VDDPLL Power-up Sequence

There is a power up sequence requirement that the *VDDPLL* must not be the last supply to ramp up. In Libero SoC v11.9, the RTG4 CCC Configurator v1.1.226 introduces an option to expose a new input *READY_VDDPLL* to assist customers who cannot meet the existing requirement. Tie READY_VDDPLL to high if you are certain that VDDPLL will not be the last supply to ramp up. Otherwise, drive READY_VDDPLL from a circuit that delays the assertion of VDDPLL by 73 ms as described in UG0586: RTG4 FPGA Clocking Resources User Guide. When PLL Internal Feedback mode is selected, READY_VDDPLL is always exposed.

2.10 RTG4 Global Net Report Additional Warning

The Global Net Report in Libero SoC v11.9 includes additional warnings for SET mitigation for routed inputs into the CCC.

2.11 RTG4 Connections of RCOSC_50MHZ, SpaceWire, CCC, CCCDYN and CCCAPB

Libero SoC v11.9 has enhanced checks in RTG4 on connections for the on-chip RC oscillator, SpaceWire, CCC and Dynamic CCC.

2.12 SmartFusion2 and IGLOO2 CCC Spread Spectrum Modulation Frequency

Libero SoC v11.9 has enhanced checks in SmartFusion2 and IGLOO2 for the frequency of CCC Spread Spectrum Modulation.

2.13 SmartFusion2 and IGLOO2 MDDR and FDDR tRFC(min)

Libero SoC v11.9 extends the t(RFC) of MDDR and FDDR in SmartFusion2 and IGLOO2 to 255 cycles.

2.14 RT3PL Radiation Range

Libero SoC v11.9 extends the radiation range of RT3PL to 25 krad.

2.15 FlashPro Lite supported on Windows 10

Libero SoC v11.9 extends support of FlashPro Lite to the Windows 10 platform.

2.16 Synplify Pro ME L2016.09MSP1-5

Libero SoC v11.9 includes the Synplify Pro ME (L2016.09MSP1-5) version, and has the following enhancements for SmartFusion2, IGLOO2, and RTG4 families.

- RTG4 - Disable safe implementation for FSMs
- RTG4 - Write Byte-Enable Support for RAM
- RTG4 - Updated Timing Models

- SmartFusion2, IGLOO2, RTG4 - Soft JTAG Controller feature in Identify Instrumentor

For more information, see the Synplify Pro ME L2016.09MSP1-5 Release Notes.

3 Resolved Issues

The following table lists the customer-reported issues resolved in Libero SoC v11.9.

Case Number	Description
493642-2489506426	RTG4: Netlist crashes due to long INIT string
493642-2287266422	RTG4 LSRAM Configurator: Expose BUSY Signal to top level component
493642-2450294901	RT3P radiation entry in device select wizard should be 0 to 25krad
493642-2447722637	Clock to output paths for Max delay and Min delay are same
493642-2394124921, 493642-2430299943, 493642-2439804921, 493642-2420228396	Detect non-pipelined ECC LSRAMs and enforce SET mitigation
493642-2440676189	Removal of Column from Verify Timing Reports under section Summary
493642-2394124921, 493642-2430299943, 493642-2439804921, 493642-2420228396	RTG4 RAM with ECC: Flags should be unknown in certain conditions
493642-2394124921, 493642-2430299943, 493642-2439804921, 493642-2420228396	RTG4: Generated RAM blocks should gate-off ECC flags using BLK
493642-2440672065	Missing doc for RCOSC_1MHZ_FAB macro
493642-2434780251	FlashPro should accept read only STAPL file
493642-2433782333	SmartTime/Timing Constraints Editor is autogenerating PLL timing constraints
493642-2423169047	RTG4: Simulation does not reflect actual silicon behavior of CCC glitch filter
493642-2388504706	MSIO/MSIOD - Prog Input Delay PDC constraint ignored for inputs using hardwired connection
493642-2421844642	RTG4: PLL output clock drifts (duty cycle distortion) when cascading
493642-2418600964	In SDC file, commands after comments inside procedure are not considered for timing analysis
493642-2418600964	Tcl proc in SDC results in error
493642-2367580180	SmartFusion2/IGLOO2: Export device digest with DEVICE INFO action
493642-2412614121	Windows 10 (Win10) support for FlashPro Lite
493642-2408183444,493642-2399832422	SmartFusion2/IGLOO2: I/O Setting not held correctly prior to programming
493642-2386963737	SmartFusion: IHP request for programming files
493642-2391804130	SmartDebug errors out after setting a LiveProbe with a UPK1 set by the design
493642-2378811397	RTG4 CCC behavior
493642-2371604853, 493642-2379037507	Incorrect connection mentioned between pcie_init and PCI SERDES block
493642-2349889033	M2S encrypted flow causes minimum delay violations
493642-2353722335	Issue: CCC with spread spectrum enabled
493642-2226349856, 493642-2281761072	SmartFusion2 DDR3 tRFC(min) setting over 80 clock cycles is not allowed by the GUI

493642-2438396551	N/C reported when set_input_delay is used with get_clocks
493642-2100791846	RT3PL: radiation range does not match datasheet
493642-2394124921, 493642-2430299943, 493642-2439804921, 493642-2420228396	RTG4: Generated RAM blocks should gate-off ECC flags using BLK
493642-2371604853, 493642-2379037507	Incorrect connection mentioned between pcie_init and PCI SERDES block
493642-2447336052	-enable_set_mitigation is not shown in the exported script file
493642-2388504706	MSIO/MSIOD - Prog Input Delay PDC constraint ignored for inputs using hardwired connection
493642-2423169047	RTG4: Simulation does not reflect actual silicon behavior of CCC glitch filter
493642-1931122687	RTG4: Wrong set up time used in timing calculation
	RTG4: Detect LSRAM Read Before Write mode on project open and convert
	RTG4 globals warning: routed inputs to CCC should be flagged
	RTG4: Add Compile Check to prevent RAM1K18 Read Before Write WMODE
	RTG4 Dual-Port LSRAM Configurator: Remove Read-Before-Write option
	RTG4 uSRAM simulation mismatch with HW behavior
	RTG4 "Radiation Protected" warning should be "SET Mitigated"
	CISCO: Add option to allow device for future key Rotation
	I/O state programming JTAG mode "Z" state means tristate with pull up
	SERDES receive data failures in fabric --> No timing violation but fails in hardware
	"Reserve pin for Device Migration" option checked automatically whenever operating conditions changed, including KRAD
	Error in NDC file not flagged by check or compile
	BLOCK: COREAPBLSRAM_0 instance is outside the hierarchy in the assembled design
	Secured programming fails 2nd time using Libero11.8 SP3

4 Design Migration

Note the following issues when a project created with a release on or before Libero SoC v11.8 SP3 is first opened in Libero SoC v11.9.

4.1 RTG4 Timing Data Updates

There have been timing data updates to the RT4G150 device after the release of Libero SoC v11.8 SP3.

- PCN18009.6 Updated certain paths to EPCS, SERDES, FDDR, RGB and RGRESET

When a project that has completed Place and Route in a prior release is first opened in Libero SoC v11.9, there is no design state invalidation.

- Microchip recommends rerunning timing analysis in Libero SoC v11.9. If there is no timing violation, no action is required. If rerunning timing analysis in Libero SoC v11.9 results in timing violations, rerun Place and Route and then Timing Analysis to ensure that there are no timing violations.

4.2 RTG4 SRAM Updates

There have been functional updates to the RTG4 Two-port LSRAM, Dual-port LSRAM and Micro SRAM components after the release of Libero SoC v11.8 SP3.

- PCN18011.1 Dual-Port Large SRAM Read-Before-Write Option Removed
- PCN18009.1 LSRAM ECC Errors

Existing projects created in prior releases will be invalidated when the project is first opened in Libero SoC v11.9 if any of the above conditions is detected. Upon opening the project, a pop-up informational window alerts you to the invalidation. The design state reverts to the pre-synthesis state (for Enhanced Constraint Flow) or the pre-compile state (for Classic Constraint Flow). Make the design change as necessary. To continue with the design flow, rerun synthesis (for Enhanced Constraint Flow) or compile (for Classic Constraint Flow).

4.3 RTG4 CCC Updates

There have been functional updates to the RTG4 CCC component after the release of Libero SoC v11.8 SP3.

- PCN18009.7 PLL in Internal Feedback Mode (TMR Mode)

Existing projects created in prior releases will be invalidated when the project is first opened in Libero SoC v11.9 if the above condition is detected. On opening the project, a pop-up informational window alerts you to the invalidation. The design state reverts to the pre-synthesis state (for Enhanced Constraint Flow) or the pre-compile state (for Classic Constraint Flow). Download the latest RTG4FCCC core version (v1.1.226 or later) and replace the component. Make the new connections as necessary and regenerate the design. To continue with the design flow, rerun synthesis (for Enhanced Constraint Flow) or compile (for Classic Constraint Flow).

4.4 RTG4 SmartGen Core Changes

The following RTG4 SgCores have been updated to be compatible with Libero SoC v11.9. If an existing project contains one or both of the following cores, you should update the core to the latest version and regenerate the component before continuing with the design flow.

Core	Version	Changes
RTG4 FCCC	1.1.226	Circuit to monitor the lock signal in PLL Internal feedback mode. An option to expose a new input READY_VDDPLL to ensure proper VDDPLL power-up sequence.
RTG4 TPSRAM	1.1.107	Option to expose BUSY output for SmartDebug.

5 Known Limitations, Issues and Workarounds

Note: Unless stated otherwise, known issues from Libero SoC v11.8, v11.8 SP1, v11.8 SP2, and v11.8 SP3 also apply to Libero SoC v11.9. Review the Libero SoC v11.8 Release Notes, Libero SoC v11.8 SP1 Release Notes , Libero SoC v11.8 SP2 Release Notes, and Libero SoC v11.8 SP3 Release Notes for Known Issues in Libero SoC v11.8, v11.8 SP1, SP2, and SP3.

5.1 Probe design crashes for ProASIC3

For designs created with ProASIC3 devices, the “Generate Probed Design” step in Designer leads to a crash if Designer is invoked from the Libero flow.

Workaround: Use Designer in standalone mode for running the Generate Probed Design step to eliminate the crash.

5.2 RTG4 - Dual-Port Large SRAM Read-Before Write Option Removed

RTG4 no longer supports the Read-Before-Write feature in the large SRAM (LSRAM). See RTG4 FPGA PCN18011 for details. In the Dual-Port Large SRAM Configurator, the Read-before-Write option for DOUT on Write has been removed.

For existing designs migrated to Libero SoC v11.9, upon opening the project, Libero SoC will check every LSRAM for any Read-Before-Write feature usage and invalidate the design flow status. If the Read-Before-Write feature is detected during the Compile step (for Classic Constraint Flow) or the Synthesis step (for Enhanced Constraint Flow), an error message appears: “Instance XYZ uses Read-Before-Write which is no longer supported”.

To continue with the design process in the new release, you need to modify the design to change the functionality that requires Read-Before-Write in the RTL source or in the instances of the Dual-Port LSRAM Configurator. See the section on Large SRAM in UG0574: RTG4 FPGA Fabric User Guide.

Modify the RTL source by adding attributes and re-synthesize. Consider whether simultaneous read and write to the same address is possible in the design and apply the appropriate address collision detection measures.

Synplify Pro and the Synopsys document on Inferring RTG4 SRAM blocks will be updated in a future release so that it no longer allows the inference of LSRAMs with the Read-Before-Write option.

5.3 Support for large disk drives

Libero is currently only supported for partitions 2TB or smaller. If either the Libero install or the Libero project is located on a partition that is larger than 2TB, file access errors or tool crashes may occur. Support for larger partitions is expected to be added in the upcoming Libero SoC v12.0 release.

5.4 FlashPro TCK cannot be set above 4MHz in single device mode

If the maximum TCK frequency is set above 4MHz in single device mode, it will be reset to 4MHz, and a warning message will be displayed. Set TCK at 4MHz or below, or use chain mode.

5.5 FlashLock/UPK1 does not protect eNVM bitstream programming/verify and read

Once the Security Policy is programmed, SmartFusion2 and IGLOO2 eNVM bitstream programming and verification is protected by UEK1/UEK2. The user must know the correct UEK1/UEK2 to successfully program or verify the eNVM.

To prevent reading of the eNVM content, select the “No Debug” option under the “SmartDebug access control” option in the Debug Policy of the Security Policy Manager. The eNVM FlashLock/UPK1 protection option will be removed from the Security Policy Manager in the next release.

5.6 SmartFusion2/IGLOO2: I/O State During Programming settings are not propagated to the programming file and Generate Bitstream state is not invalidated

The I/O state during programming is not set according to the settings that the user set in the I/O State During Programming.

Workaround: After setting the I/O State(s) During Programming to the desired states, before programming or reprogramming, run the Generate Bitstream or Export Bitstream command and then run programming.

5.7 SPPS: Ticket counter decrements incorrectly when using HSM flow

Issue: When using HSM SPPS flow for larger SmartFusion2 and IGLOO2 devices (-060, -090 and -150), the number of devices per HSM ticket is incorrectly reduced as follows when running programming action in Flashpro Express:

PROGRAM action decreases program ticket counter by 2.

ERASE action decreases 1 verify ticket counter and 1 erase ticket counter.

Workaround: Specify double the number of devices per ticket in the "max_device" parameter of "new_hsmtask_ticket" in Job Manager.

5.8 SPPS: Erase action in HSM flow fails if VERIFY ticket is not present

If a HSM FlashPro Express job has tickets for PROGRAM and ERASE but not for VERIFY, the ERASE action will fail with the following message:

```
Error: No flashpro ticket data found.
```

Workaround: Add ticket for VERIFY if ERASE action is needed.

Note: Running the ERASE action will reduce the ERASE ticket count and VERIFY ticket count (if VERIFY action has not been run), so the user must specify a number of devices in both ERASE and VERIFY tickets.

5.9 Synplify Pro error: library Fusion not found

There are missing lines related to the Fusion library from the location.map from Synplify Pro installation folder.

Workaround: Updated files can be patched locally upon request.

5.10 High reliability option in Synplify Pro is not inferring the state machine correctly

With High reliability option on, Synplify Pro does not infer state machines from the state machine coding in the correct way.

Workaround: Use the attribute syn_state_machine in the case statement code as below:

attribute syn_state_machine : boolean;
attribute syn_state_machine of state : signal is true;

5.11 Warning message: "@W: CL269 : State error detection not built"

Reason: *Refer to Synplify Pro Help for CL269 warning message.*
In safe mode, the compiler generates a state error detection component for all case statements used to synthesize the state machine logic. If the component is removed, this warning is generated for you to confirm the following:

1. A state machine was not inferred for a particular case statement.
2. A state machine was inferred from a case statement, but the case statement is missing an others clause (VHDL) or default clause (Verilog).

Action: Check for the correct intended behavior. In the first condition above, verify whether the logic should not be a state machine or if the compiler was unable to extract it. For the second scenario, you may need to add an others or default clause to the source code so the compiler knows how to handle a bad state.

Workaround: If you believe a state machine was not inferred for a particular case statement, analyze the RTL to understand why the logic should not be a state machine. If the intended behavior is correct, ignore the warning message. Otherwise, modify the RTL so that a state machine is inferred.

6 System Requirements

For information about operating system support and minimum system requirements, see the System Requirements web page.

For Linux OS setup instructions, see How to Set Up Linux Environment for Libero User Guide.

6.1 Operating System Support

Supported

- Windows 7, Windows 8.1, Windows 10
- RHEL 5*, RHEL 6, RHEL 7, CentOS 5*, CentOS 6, and CentOS 7
- SuSE 11 SP4 (Libero only. FlashPro Express, SmartDebug, and Job Manager are not supported.)

Note: * RHEL 5 and CentOS 5 do not support programming using FlashPro5.

Not Supported

- 32-bit operating systems
- Windows XP
- Support for the following operating systems will cease with the next major Libero SoC release. For more information, refer to PCN17031.
    - RedHat Enterprise Linux 5.x through 6.5
    - CentOS 5.x through 6.5

7 Libero SoC v11.9 Download

Click the following links to download Libero SoC v11.9 on Windows and Linux operating systems:

- Windows Download
- Linux Download
- Mega Vault Download

Note: Installation requires administrator privileges to the system.

After successful installation, clicking **Help-> About Libero** will show Version: 11.9.0.4.

7.1 Downloading SoftConsole 3.4/4.0/5.1

Libero SoC v11.9 is compatible with SoftConsole v3.4 SP1, SoftConsole v4.0 and SoftConsole v5.x

- SoftConsole Download