Libero SoC v11.9 SP2

Release Notes

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Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision 1.1

Added known issue 3.1 SmartTime: False failure during max/best case analysis.

Revision 1.0

Revision 1.0 was the first publication of this document.

Contents

1 Libero SoC v11.9 SP2 Release Notes

The Libero® system on chip (SoC) v11.9 SP2 is a service pack release of the Libero SoC v11.9 software for designing with Microsemi's power efficient flash FPGAs, SoC FPGAs, and rad-tolerant FPGAs. The suite integrates industry standard Synopsys Synplify Pro® synthesis and Mentor Graphics ModelSim® simulation with best-in-class constraints management, debug capabilities, and secure production programming support.

Use Libero SoC v11.9 SP2 for designing with Microsemi's RTG4 Rad-Tolerant FPGAs.

To access datasheets, silicon user guides, tutorials, and application notes, visit www.microsemi.com, navigate to the relevant product family page, and click the **Documentation** tab. Development Kits & Boards are listed in the **Design Resources** tab.

Libero SoC v11.9 SP2 implements several critical bug fixes focusing on the RTG4 FPGA family. This release is only intended for use with the RTG4 family. It is recommended that all Libero projects targeting the RTG4 family be opened with this release, and timing reports regenerated.

2 What's New in Libero SoC v11.9 SP2

Libero SoC v11.9 SP2 implements the following bug fixes targeted to the RTG4 family:

2.1 ECC Flags on Depth Cascaded RAM Blocks

Libero SoC v11.9 introduced features in the Dual-port LSRAM, Two-port LSRAM and uSRAM configurators to generate logic that gates-off the ECC flags for inactive RAM blocks. The gating logic was correctly generated up to the cascading depths listed below, depending on the optimization option of High-speed or Low-power.

- Two-port LSRAM Low-power 4K x 36
- Dual-port LSRAM 8K x 18
- uSRAM 256 x 18

However, due to the depth limits on the RAM configurators, any RAM components built with a cascading depth greater than 8 RAM blocks deep did not include sufficient logic to ensure the correct RAM block's ECC flags reached the component-level flag output ports.

The ECC flags from the active RAM blocks beyond the above depth limits would be in the 'X' state in pre-synthesis simulations and the '0' state in post-synthesis and post-layout simulations.

Furthermore, synthesis with Synplify Pro will generate warnings such as those shown below:

```
@W: CG360 :"C:\...\TPLSRAM_10213x72_0_RTG4TPSRAM.v":334:8:334:21|Removing wire
BLKY2_pipe[2], as there is no assignment to it.
```

```
@W: CL156 :"C:\...\TPLSRAM_10213x72_0_RTG4TPSRAM.v":334:8:334:21|*Input BLKY2_pipe[2] to
expression [instance] has undriven bits; assigning undriven bits to 0.  Simulation
mismatch possible. Assign all bits of the input.
```

Libero SoC v11.9 SP2 lifts the depth limits, enabling the Dual-port LSRAM, Two-port LSRAM and uSRAM configurators to correctly generate logic that gates-off ECC flags for inactive RAM blocks for all depths.

Each RAM component generated by the Dual-port LSRAM, Two-port LSRAM and uSRAM configurators includes a log file within the project's /component/work/<component_name>/<instance_name>/ sub-folder listing the RAM cascade configuration. The number of blocks cascaded depth-wise can be used to determine whether the particular RAM component uses more than 8 RAM blocks deep, and requires regeneration using Libero SOC v11.9 SP2.

```
Cascade Configuration:
     Write Port configuration   : 1024x18
     Read Port configuration    : 1024x18
     Number of blocks depth wise: 10
     Number of blocks width wise: 4
```

Update the RAM components within a design by regenerating them using Libero SoC v11.9 SP2.

2.2 Double accounting of clock latency when applied to generated clocks

When a clock latency constraint is set on a generated clock, the Static Timing Analyzer uses the late clock latency (and respectively early clock latency) value in the calculation of the data arrival time (and respectively the data required time). However, due to an error introduced in Libero SoC v11.7.SP1, an additional delay (equal to late-early) is incorrectly added to the clock net driven by the clock source in the required time calculation.

This issue is fixed in the Libero SoC v11.9 SP2 release.

2.3 Timing arc dropped when using interface logic LUT with inversion

In the specific scenario of a Flip-Flop connected directly to the physical D pin of a neighboring interface logic combinatorial cell with an inversion of the signal, the timing model of the interface logic comb cell was missing the timing arc from the D pin to the Y pin. This rare error prevents the static timing analyzer from accounting for the paths that go through this connection when checking for timing violations.

This issue is fixed in the Libero SoC v11.9 SP2 release.

2.4 Zero delay on hardwired nets from specific IOs to GRESET

IO to GRESET hardwired nets at four specific GRESET input pin locations have zero delay value due to a pin name mismatch with the database. Consequently, the insertion delay on the GRESET is underestimated.

This issue is fixed in the Libero SoC v11.9 SP2 release.

3 Known Limitations, Issues and Workarounds

Known issues from Libero SoC v11.9 also apply to Libero SoC v11.9 SP2. Review the Libero SoC v11.9 Release Notes for Known Issues in Libero SoC v11.9.

3.1 SmartTime: False failure during max/best case analysis

Verify timing may fail during fast corner analysis.

Workaround: Disable Coverage report (Verify Timing>Configure Options) or upgrade to Libero SoC v12.0.

4 System Requirements

For information about operating system support and minimum system requirements, see the System Requirements web page.

For Linux OS setup instructions, see How to Set Up Linux Environment for Libero User Guide:

4.1 Operating System Support

Supported

- Windows 7, Windows 8.1, Windows 10
- RHEL 5*, RHEL 6, RHEL 7, CentOS 5*, CentOS 6, and CentOS 7
- SuSE 11 SP4 (Libero only. FlashPro Express, SmartDebug, and Job Manager are not supported.)

Note: * RHEL 5 and CentOS 5 do not support programming using FlashPro5.

Not Supported

- 32-bit operating systems
- Windows XP
- Support for the following operating systems will cease with the next major Libero SoC release. For more information, refer to PCN17031.
    - RedHat Enterprise Linux 5.x through 6.5
    - CentOS 5.x through 6.5

5 Libero SoC v11.9 SP2 Download

Click the following links to download Libero SoC v11.9 SP2 on Windows and Linux operating systems:

- Windows Download
- Linux Download
- Mega Vault Download
  (Note: There are no changes in the Mega Vault for Libero SoC v11.9 SP2; use the Libero SoC v11.9 Mega Vault for this release as well.)

Note: Installation requires administrator privileges to the system.

Libero SoC v11.9 SP2 is an incremental service pack and can be installed over Libero SoC v11.9, or over Libero SoC v11.9 SP1

After successful installation, clicking **Help-> About Libero** will show Version: 11.9.2.1.

5.1 Downloading SoftConsole 3.4/4.0/5.1

Libero SoC v11.9 SP2 is compatible with SoftConsole v3.4 SP1, SoftConsole v4.0 and SoftConsole v5.x

- SoftConsole Download