Microsemi makes no warranty, representation, or guarantee regarding the information contained herein or the suitability of its products and services for any particular purpose, nor does Microsemi assume any liability whatsoever arising out of the application or use of any product or circuit. The products sold hereunder and any other products sold by Microsemi have been subject to limited testing and should not be used in conjunction with mission-critical equipment or applications. Any performance specifications are believed to be reliable but are not verified, and Buyer must conduct and complete all performance and other testing of the products, alone and together with, or installed in, any end-products. Buyer shall not rely on any data and performance specifications or parameters provided by Microsemi. It is the Buyer’s responsibility to independently determine suitability of any products and to test and verify the same. The information provided by Microsemi hereunder is provided “as is, where is” and with all faults, and the entire risk associated with such information is entirely with the Buyer. Microsemi does not grant, explicitly or implicitly, to any party any patent rights, licenses, or any other IP rights, whether with regard to such information itself or anything described by such information. Information provided in this document is proprietary to Microsemi, and Microsemi reserves the right to make any changes to the information in this document or to any products and services at any time without notice.

About Microsemi
Microsemi Corporation (NASDAQ: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world’s standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions; security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, California, and has approximately 4,800 employees globally. Learn more at www.microsemi.com.

5-02-00754-8/12.18
# Table of Contents

## Table of Contents

Introduction to Tcl Scripting ................................................................. 9
Tcl Commands and Supported Families .................................................. 9
Tcl Command Documentation Conventions .............................................. 9

**Basic Syntax** ....................................................................................... 11
Sample Tcl Script .................................................................................. 11
Types of Tcl commands ......................................................................... 12
Variables ............................................................................................... 13
Command substitution .......................................................................... 13
Lists and arrays .................................................................................... 15
Special arguments (command-line parameters) ...................................... 15
Control structures ................................................................................. 16
Print statement and Return values ....................................................... 16
Exporting Tcl Scripts ........................................................................... 17
extended_run_lib ................................................................................ 18
Sample Tcl Script - Project Manager .................................................... 20
How to Derive Required Part Information from A "Part Number" ....... 21

**Project Manager Tcl Commands** ....................................................... 22
add_file_to_library .............................................................................. 22
add_library ......................................................................................... 22
add_modelsim_path ............................................................................ 22
add_profile ......................................................................................... 23
associate_stimulus ............................................................................ 24
change_link_source ........................................................................... 24
check_fdc_constraints ....................................................................... 25
check_hdl ............................................................................................ 25
cHECK_NDC_CONSTRAINTS ................................................................. 25
cHECK_PDC_CONSTRAINTS ................................................................. 25
cHECK_SDC_CONSTRAINTS ................................................................. 26
close_design ....................................................................................... 26
close_project ...................................................................................... 27
configure_tool ..................................................................................... 27
create_and_configure_core ................................................................. 28
cREATE SET ......................................................................................... 29
cREATE_LINKS ................................................................................... 30
cREATE_SMARTDESIGN ..................................................................... 31
download_core ................................................................................... 31
download_latest_cores ....................................................................... 31
<table>
<thead>
<tr>
<th>Command</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>edit_profile</td>
<td>32</td>
</tr>
<tr>
<td>export_as_link</td>
<td>32</td>
</tr>
<tr>
<td>export_ba_files</td>
<td>33</td>
</tr>
<tr>
<td>export_bitstream_file</td>
<td>34</td>
</tr>
<tr>
<td>export_bsd_file</td>
<td>36</td>
</tr>
<tr>
<td>export_component_to_tcl</td>
<td>36</td>
</tr>
<tr>
<td>export_design_summary</td>
<td>37</td>
</tr>
<tr>
<td>export_fp_pdc</td>
<td>37</td>
</tr>
<tr>
<td>export_ibis_file</td>
<td>38</td>
</tr>
<tr>
<td>export_io_pdc</td>
<td>38</td>
</tr>
<tr>
<td>export_netcst_file</td>
<td>39</td>
</tr>
<tr>
<td>export_pin_reports</td>
<td>39</td>
</tr>
<tr>
<td>export_profiles</td>
<td>40</td>
</tr>
<tr>
<td>export_prog_job</td>
<td>40</td>
</tr>
<tr>
<td>export_script</td>
<td>41</td>
</tr>
<tr>
<td>generate_component</td>
<td>42</td>
</tr>
<tr>
<td>generate_sdc_constraint_coverage</td>
<td>42</td>
</tr>
<tr>
<td>import_files (Libero SoC)</td>
<td>43</td>
</tr>
<tr>
<td>new_project</td>
<td>45</td>
</tr>
<tr>
<td>open_project</td>
<td>48</td>
</tr>
<tr>
<td>open_smartdesign</td>
<td>49</td>
</tr>
<tr>
<td>organize_constraints</td>
<td>49</td>
</tr>
<tr>
<td>organize_sources</td>
<td>50</td>
</tr>
<tr>
<td>organize_tool_files</td>
<td>51</td>
</tr>
<tr>
<td>project_settings</td>
<td>52</td>
</tr>
<tr>
<td>refresh</td>
<td>53</td>
</tr>
<tr>
<td>remove_core</td>
<td>53</td>
</tr>
<tr>
<td>remove_library</td>
<td>53</td>
</tr>
<tr>
<td>remove_profile</td>
<td>54</td>
</tr>
<tr>
<td>rename_file</td>
<td>54</td>
</tr>
<tr>
<td>rename_library</td>
<td>55</td>
</tr>
<tr>
<td>run_tool</td>
<td>55</td>
</tr>
<tr>
<td>save_project_as</td>
<td>57</td>
</tr>
<tr>
<td>save_log</td>
<td>58</td>
</tr>
<tr>
<td>save_project</td>
<td>58</td>
</tr>
<tr>
<td>save_smartdesign</td>
<td>59</td>
</tr>
<tr>
<td>select_profile</td>
<td>59</td>
</tr>
<tr>
<td>set_actel_lib_options</td>
<td>59</td>
</tr>
<tr>
<td>set_as_target</td>
<td>60</td>
</tr>
<tr>
<td>set_device (Project Manager)</td>
<td>60</td>
</tr>
<tr>
<td>set_modelsim_options</td>
<td>61</td>
</tr>
<tr>
<td>set_option</td>
<td>63</td>
</tr>
<tr>
<td>set_root</td>
<td>64</td>
</tr>
<tr>
<td>set_user_lib_options</td>
<td>64</td>
</tr>
<tr>
<td>unlink</td>
<td>65</td>
</tr>
<tr>
<td>unset_as_target</td>
<td>65</td>
</tr>
</tbody>
</table>
use_source_file..................................................................................................................65

**SmartDesign Tcl Commands**..........................................................................................67
sd_add_pins_to_group ................................................................. 67
sd_clear_pin_attributes .............................................................. 67
sd_configure_core_instance ....................................................... 68
sd_connect_instance_pins_to_ports ......................................... 68
sd_connect_pins_to_constant ..................................................... 69
sd_connect_pin_to_port ............................................................. 70
sd_connect_pins ................................................................. 70
sd_create_bif_port ................................................................. 71
sd_create_bus_port ................................................................. 73
sd_create_pin_group ................................................................. 73
sd_create_pin_slices ................................................................. 74
sd_create_scalar_port .............................................................. 74
sd_delete_instances ............................................................... 75
sd_delete_nets ................................................................. 75
sd_delete_pin_group ................................................................. 76
sd_delete_pin_slices ................................................................. 76
sd_delete_ports ................................................................. 77
sd_disconnect_instance .......................................................... 77
sd_disconnect_pins ................................................................. 78
sd_duplicate_instance ............................................................ 78
sd_hide_bif_pins ................................................................. 79
sd_instantiate_component ....................................................... 80
sd_instantiate_core ........................................................... 80
sd_instantiate_hdl_core .......................................................... 81
sd_instantiate_hdl_module .................................................... 81
sd_instantiate_macro ............................................................ 82
sd_invert_pins ................................................................. 82
sd_mark_pins_unused ............................................................. 83
sd_remove_pins_from_group .................................................... 83
sd_rename_instance .............................................................. 84
sd_rename_pin_group ............................................................. 84
sd_rename_port ................................................................. 85
sd_save_core_instance_config .................................................. 86
sd_show_bif_pins ................................................................. 86
sd_update_instance .............................................................. 87

**HDL Tcl Commands** ....................................................................................................88
create_hdl_core ................................................................. 88
hdl_core_add_bif ................................................................. 88
hdl_core_assign_bif_signal .................................................... 89
hdl_core_delete_parameters .................................................. 89
hdl_core_extract_ports_and_parameters ................................ 90
hdl_core_remove_bif ............................................................ 90
Command Tools .......................................................... 93
CONFIGURE_CHAIN ................................................ 93
CONFIGURE_PROG_OPTIONS ....................................... 94
GENERATEPROGRAMMINGFILE .................................... 94
IO_PROGRAMMING_STATE ......................................... 95
PLACEROUTE ....................................................... 95
PROGRAMDEVICE ................................................ 98
PROGRAM_SPI_FLASH_IMAGE ..................................... 100
PROGRAMMER_INFO ............................................... 100
SPM ................................................................. 102
SYNTHESIZE ....................................................... 104
VERIFYPOWER ..................................................... 107
VERIFYTIMING ..................................................... 107
SIMULATE ......................................................... 108

SmartTime Tcl Commands .............................................. 109
create_set .......................................................... 109
expand_path ........................................................ 110
list_paths ........................................................... 112
read_sdc ............................................................. 113
remove_set .......................................................... 114
report ................................................................. 114
Arguments ............................................................ 114
save ................................................................. 117
set_options .......................................................... 118

SmartPower Tcl Commands ........................................... 121
smartpower_add_new_scenario .................................. 121
smartpower_add_pin_in_domain ................................ 121
smartpower_battery_settings .................................... 122
smartpower_change_clock_statistics ......................... 123
smartpower_change_setofpin_statistics ..................... 124
smartpower_commit ................................................. 124
smartpower_compute_vectorless ................................ 124
smartpower_create_domain ...................................... 125
smartpower_edit_scenario ....................................... 125
smartpower_import_vcd .......................................... 126
smartpower_init_do ............................................... 128
smartpower_init_set_clocks_options ......................... 130
smartpower_init_set_combinational_options ............... 131
smartpower_init_set_enables_options ...................... 131
smartpower_init_set_primaryinputs_options ............... 132
smartpower_init_set_registers_options
smartpower_init_setopins_values
smartpower_remove_all_annotations
smartpower_remove_file
smartpower_remove_scenario
smartpower_report_power
smartpower_set_mode_for_analysis
smartpower_set_mode_for_pdpr
smartpower_set_operating_condition
smartpower_set_operating_conditions
smartpower_set_process
smartpower_set_scenario_for_analysis
smartpower_set_temperature_opcond
smartpower_set_voltage_opcond
smartpower_temperature_opcond_set_design_wide
smartpower_temperature_opcond_set_mode_specific
smartpower_voltage_opcond_set_design_wide
smartpower_voltage_opcond_set_mode_specific

Programming and Configuration Tcl Commands ...............152
configure_design_initialization_data ..........................152
calculate_design_initialization_data .........................153
set_client (for RAM) ........................................153
configure_snvm .............................................154
configure_spiflash ..........................................155
SPM_OTP ................................................................156
calculate_uprom ................................................158
export_spiflash_image ..........................................158
generate_design_initialization_data ............................158
generate_initialization_mem_files ............................159
remove_permanent_locks ........................................160
select_programmer ..............................................160
set_auto_update_mode ..........................................161
set_cipher_text_auth_client ....................................161
set_client .......................................................162
set_data_storage_client ................................ .......163
set_manufacturer ...............................................164
set_plain_text_auth_client ....................................165
set_plain_text_client ..........................................166
set_programming_interface ......................................167
set_usk_client ..................................................167

FlashPro Express Tcl Commands ................................169
close_project ....................................................169
configure_flashpro3_prg .......................................169
configure_flashpro4_prg .......................................170
PolarFire FPGA Tcl Commands Reference Guide

configure_flashpro5_prg ................................................................. 170
create_job_project ................................................................. 171
dump_tcl_support ................................................................. 171
open_project ................................................................. 172
ping_prg ................................................................. 172
refresh_prg_list ................................................................. 172
remove_prg ................................................................. 173
run_selected_actions ................................................................. 173
save_log ................................................................. 174
save_project ................................................................. 174
scan_chain_prg ................................................................. 174
self_test_prg ................................................................. 175
set_prg_name ................................................................. 175
set_programming_action ................................................................. 175
set_programming_file ................................................................. 176

SmartDebug Tcl Commands ................................................................. 177
SmartDebug Tcl Support ................................................................. 177
add_probe_insertion_point ................................................................. 179
add_to_probe_group ................................................................. 179
construct_chain_automatically ................................................................. 180
create_probe_group ................................................................. 180
delete_active_probe ................................................................. 181
enable_device ................................................................. 181
event_counter ................................................................. 182
export_smart_debug_data ................................................................. 182
fhb_control ................................................................. 183
frequency_monitor ................................................................. 185
get_programmer_info ................................................................. 185
load_active_probe_list ................................................................. 185
loopback_mode ................................................................. 186
move_to_probe_group ................................................................. 186
optimize_dfe ................................................................. 186
pcie_config_space ................................................................. 187
pcie_ltssm_status ................................................................. 187
plot_eye ................................................................. 188
program_probe_insertion ................................................................. 188
read_active_probe ................................................................. 188
read_isram ................................................................. 189
read_usram ................................................................. 189
remove_from_probe_group ................................................................. 190
remove_probe_insertion_point ................................................................. 191
run_selected_actions ................................................................. 191
save_active_probe_list ................................................................. 191
scan_chain_prg ................................................................. 192
select_active_probe ................................................................. 192
set_live_probe.................................................................193
set_debug_programmer.....................................................193
set_programming_action...................................................194
set_programming_file.....................................................194
smartbert_test...............................................................195
static_pattern_transmit..................................................196
ungroup...........................................................................197
unset_live_probe.............................................................197
uprom_read_memory..........................................................198
write_active_probe..........................................................198
write_lsram....................................................................199
write_usram....................................................................200
xcvr_read_register............................................................200
xcvr_write_register..........................................................202

JTAG Configuration Tcl Commands...........................................205
add_actel_device...............................................................205
add_non_actel_device.........................................................205
add_non_actel_device_to_database.......................................206
construct_chain_automatically..........................................206
copy_device.....................................................................207
cut_device........................................................................207
enable_device..................................................................207
paste_device....................................................................208
remove_device..................................................................208
remove_non_actel_device_from_database................................209
select_libero_design_device..............................................209
set_bsdll_file..................................................................210
set_device_ir....................................................................210
set_device_name................................................................211
set_device_order................................................................211
set_device_tck..................................................................211
set_device_type..................................................................212
set_programming_action.....................................................212
set_programming_file.........................................................213

Example Tcl Script to Create a NativePMA_prbs Design...............214
Introduction to Tcl Scripting

Tcl, the Tool Command Language, pronounced *tickle*, is an easy-to-learn scripting language that is compatible with Libero SoC software. You can run scripts from either the Windows or Linux command line or store and run a series of commands in a *.tcl* batch file.

This section provides a quick overview of the main features of Tcl:

- Basic syntax
- Types of Tcl commands
- Variables
- Command substitution
- Quotes and braces
- Lists and arrays
- Control structures
- Print statement and Return values

For complete information on Tcl scripting, refer to one of the books available on this subject. You can also find information about Tcl at web sites such as http://www.tcl.tk.

Libero SoC provides additional capabilities and built-in Tcl Commands:

- Running Tcl scripts from the command line
- Exporting Tcl scripts
- extended_run_lib
- Tcl Commands as specified in this document

Tcl Commands and Supported Families

This reference guide describes the supported Tcl commands for PolarFire devices in the Libero SoC v12.0 release.

Tcl Command Documentation Conventions

The following table shows the typographical conventions used for the Tcl command syntax.

<table>
<thead>
<tr>
<th>Syntax Notation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>command – argument</td>
<td>Commands and arguments appear in Courier New typeface.</td>
</tr>
<tr>
<td>variable</td>
<td>Variables appear in blue, italic Courier New typeface. You must substitute an appropriate value for the variable.</td>
</tr>
<tr>
<td>[-argument.value +variable]+</td>
<td>Optional arguments begin and end with a square bracket with one exception: if the square bracket is followed by a plus sign (+), then users must specify at least one argument. The plus sign (+) indicates that items within the square brackets can be repeated. Do not enter the plus sign character.</td>
</tr>
</tbody>
</table>

Note: All Tcl commands are case sensitive. However, their arguments are not.
Examples

Syntax for the get_clocks command followed by a sample command:

```
get_clocks variable
```

get_clocks clk1

Syntax for the backannotate command followed by a sample command:

```
backannotate -name file_name -format format_type -language language -dir directory_name [-netlist] [-pin]
```

```
backannotate -dir \
{..\design} -name "fanouttest_ba.sdf" -format "SDF" -language "VERILOG" \
-netlist
```

Wildcard Characters

You can use the following wildcard characters in names used in Tcl commands:

<table>
<thead>
<tr>
<th>Wildcard</th>
<th>What it Does</th>
</tr>
</thead>
<tbody>
<tr>
<td>\</td>
<td>Interprets the next character literally</td>
</tr>
<tr>
<td>?</td>
<td>Matches any single character</td>
</tr>
<tr>
<td>*</td>
<td>Matches any string</td>
</tr>
<tr>
<td>[]</td>
<td>Matches any single character among those listed between brackets (that is, [A-Z] matches any single character in the A-to-Z range)</td>
</tr>
</tbody>
</table>

Note: The matching function requires that you add a slash (/) before each slash in the port, instance, or net name when using wildcards in a PDC command. For example, if you have an instance named “A/B12” in the netlist, and you enter that name as “A\B*” in a PDC command, you will not be able to find it. In this case, you must specify the name as A\\B*.

Special Characters [], { }, and \\

Sometimes square brackets ([ ]) are part of the command syntax. In these cases, you must either enclose the open and closed square brackets characters with curly brackets ({ }) or precede the open and closed square brackets ([ ]) characters with a backslash (\). If you do not, you will get an error message. For example:

```
pin_assign -port {LFSR_OUT[0]} -pin 15
```

or

```
pin_assign -port LFSR_OUT[0] -pin 180
```

Note: Tcl commands are case sensitive. However, their arguments are not.

Entering Arguments on Separate Lines

To enter an argument on a separate line, you must enter a backslash (\) character at the end of the preceding line of the command as shown in the following example:

```
backannotate -dir \
{..\design} -name "fanouttest_ba.sdf" -format "SDF" -language "VERILOG" \
-netlist
```

See Also

Introduction to Tcl scripting
Basic syntax
Basic Syntax

Tcl scripts contain one or more commands separated by either new lines or semicolons. A Tcl command consists of the name of the command followed by one or more arguments. The format of a Tcl command is:

```
command arg1 ... argN
```

The command in the following example computes the sum of 2 plus 2 and returns the result, 4.

```
expr 2 + 2
```

The `expr` command handles its arguments as an arithmetic expression, computing and returning the result as a string. All Tcl commands return results. If a command has no result to return, it returns an empty string.

To continue a command on another line, enter a backslash (\) character at the end of the line. For example, the following Tcl command appears on two lines:

```
import -format "edif" -netlist_naming "Generic" -edif_flavor "GENERIC" {prepi.edn}
```

Comments must be preceded by a hash character (#). The comment delimiter (#) must be the first character on a line or the first character following a semicolon, which also indicates the start of a new line. To create a multi-line comment, you must put a hash character (#) at the beginning of each line.

**Note:** Be sure that the previous line does not end with a continuation character (\). Otherwise, the comment line following it will be ignored.

Special Characters

Square brackets ([])) are special characters in Tcl. To use square brackets in names such as port names, you must either enclose the entire port name in curly braces, for example, `pin_assign -port {LFSR_OUT[15]} -iostd lvttl -slew High`, or lead the square brackets with a slash (\) character as shown in the following example:

```
pin_assign -port LFSR_OUT\[15\] -iostd lvttl -slew High
```

Sample Tcl Script

```
#Create a new project and set up a new design
new_project -location {D:/2Work/my_pf_proj} -name {my_pf_proj} -project_description {} -block_mode 0 -standalone_peripheral_initialization 0 -use_enhanced_constraint_flow 1 -hdl {VERILOG} -family {PolarFire} -die {MPF300TS_ES} -package {FCG152} -speed {-1} -die_voltage [1.0] -part_range [EXT] -adv_options {IO_DEFT_STD:LVC莫斯 1.8V} -adv_options {SYSTEM_CONTROLLER_SUSPEND_MODE:1} -adv_options {RESTRICTPROBEPINS:1} -adv_options {RESTRICTSPIPINS:0} -adv_options {VCCI_1.2_VOLTR:EXT} -adv_options {VCCI_1.5_VOLTR:EXT} -adv_options {VCCI_1.8_VOLTR:EXT} -adv_options {VCCI_2.5_VOLTR:EXT} -adv_options {VCCI_3.3_VOLTR:EXT} -adv_options {VOLTR:EXT}

#Import HDL source file
import_files -convert_EDN_to_HDL 0 -hdl_source {C:/test/prep1.v}

#Import HDL stimulus file
import_files -convert_EDN_to_HDL 0 -stimulus {C:/test/prep1tb.v}

#set the top level design name
set_root -module {prep1::work}

#Associate SDC constraint file to Place and Route tool
organize_tool_files -tool {PLACEROUTE} -file {D:/2Work/my_pf_proj/constraint/user.sdc} -module {prep1::work} -input_type {constraint}

#Associate SDC constraint file to Verify Timing tool
organize_tool_files -tool {VERIFYTIMING} -file {D:/2Work/my_pf_proj/constraint/user.sdc} -module {prep1::work} -input_type {constraint}

#Run synthesize
```
run_tool -name {SYNTHESIZE}
#Configure Place and Route tool
configure_tool -name {PLACEROUTE} -params {DELAY_ANALYSIS:MAX} -params {EFFORT_LEVEL:false}
  -params {INCRPLACEANDROUTE:false} -params {MULTI_PASS_CRITERIA:VIOLATIONS}
  -params {MULTI_PASS_LAYOUT:false} -params {NUM_MULTI_PASSES:5} -params {PDPR:false}
  -params {RANDOM_SEED:0} -params {REPAIR_MIN_DELAY:false} -params {SLACK_CRITERIA:WORST_SLACK}
  -params {SPECIFIC_CLOCK:} -params {START_SEED_INDEX:1} -params {STOP_ON_FIRST_PASS:false}
  -params {TDPR:true}
#Run Place and Route
run_tool -name {PLACEROUTE}
#Configure Timing Report Generation
configure_tool -name {VERIFYTIMING} -run_tool -name {PLACEROUTE} -params {CONSTRAINTS_COVERAGE:1}
  -params {FORMAT:XML} -params {MAX_TIMING_FAST_HV_LT:0} -params {MAX_TIMING_SLOW_LV_HT:1}
  -params {MAX_TIMING_SLOW_LV_LT:0} -params {MAX_TIMING_VIOLATIONS_FAST_HV_LT:0}
  -params {MAX_TIMING_VIOLATIONS_SLOW_LV_HT:1} -params {MAX_TIMING_VIOLATIONS_SLOW_LV_LT:0}
  -params {MIN_TIMING_FAST_HV_LT:1} -params {MIN_TIMING_SLOW_LV_HT:0} -params {MIN_TIMING_VIOLATIONS_FAST_HV_LT:1}
  -params {MIN_TIMING_VIOLATIONS_SLOW_LV_HT:0} -params {MIN_TIMING_VIOLATIONS_SLOW_LV_LT:0}
#Run Verify Timing tool
run_tool -name {VERIFYTIMING}
#Run Power Verification tool
run_tool -name {VERIFYPOWER}
#Export bitstream
export_bitstream_file -file_name {prepare1} \
  -export_dir {D:\Work\my_pf_proj\designer\prepar1\export} -format {STP} -master_file 0 \
  -master_file_components {} -encrypted_uek1_file 0 -encrypted_uek1_file_components {} \
  -encrypted_uek2_file 0 -encrypted_uek2_file_components {} \
  -trusted_facility_file 1 -trusted_facility_file_components (FABRIC)

Types of Tcl commands
This section describes the following types of Tcl commands:

- **Built-in commands**
- **Procedures created with the proc command**

**Built-in commands**

Built-in commands are provided by the Tcl interpreter. They are available in all Tcl applications. Here are some examples of built-in Tcl commands:

- **Tcl** provides several commands for manipulating file names, reading and writing file attributes, copying files, deleting files, creating directories, and so on.
- **exec** - run an external program. Its return value is the output (on stdout) from the program, for example:
  ```tcl
  set tmp [ exec myprog ]
  puts stdout $tmp
  ```
- You can easily create collections of values (lists) and manipulate them in a variety of ways.
- You can create arrays - structured values consisting of name-value pairs with arbitrary string values for the names and values.
- You can manipulate the time and date variables.
- You can write scripts that can wait for certain events to occur, such as an elapsed time or the availability of input data on a network socket.

**Procedures created with the proc command**

You use the proc command to declare a procedure. You can then use the name of the procedure as a Tcl command.

The following sample script consists of a single command named `proc`. The proc command takes three arguments:

- The name of a procedure (myproc)
- A list of argument names (arg1 arg2)
- The body of the procedure, which is a Tcl script

```tcl
proc myproc { arg1 arg2 }
{
    # procedure body
}
myproc a b
```

**Variables**

With Tcl scripting, you can store a value in a variable for later use. You use the set command to assign variables. For example, the following set command creates a variable named x and sets its initial value to 10.

```tcl
set x 10
```

A variable can be a letter, a digit, an underscore, or any combination of letters, digits, and underscore characters. All variable values are stored as strings.

In the Tcl language, you do not declare variables or their types. Any variable can hold any value. Use the dollar sign ($) to obtain the value of a variable, for example:

```tcl
set a 1
set b $a
set cmd expr
set x 11
$cmd $x*$x
```

The dollar sign $ tells Tcl to handle the letters and digits following it as a variable name and to substitute the variable name with its value.

**Global Variables**

Variables can be declared global in scope using the Tcl `global` command. All procedures, including the declaration, can access and modify global variables, for example:

```tcl
global myvar
```

**Command substitution**

By using square brackets ([[]]), you can substitute the result of one command as an argument to a subsequent command, as shown in the following example:

```tcl
set a 12
set b [expr $a*4]
```

Tcl handles everything between square brackets as a nested Tcl command. Tcl evaluates the nested command and substitutes its result in place of the bracketed text. In the example above, the argument that appears in square brackets in the second set command is equal to 48 (that is, 12* 4 = 48).

Conceptually,

```tcl
set b [expr $a * 4]
```

expands to
set b [expr 12 * 4 ]
and then to
set b 48

Quotes and braces
The distinction between braces ({ }) and quotes (" ") is significant when the list contains references to variables. When references are enclosed in quotes, they are substituted with values. However, when references are enclosed in braces, they are not substituted with values.

Example

<table>
<thead>
<tr>
<th>With Braces</th>
<th>With Double Quotes</th>
</tr>
</thead>
<tbody>
<tr>
<td>set b 2</td>
<td>set b 2</td>
</tr>
<tr>
<td>set t { 1 $b 3 }</td>
<td>set t &quot; 1 $b 3 &quot;</td>
</tr>
<tr>
<td>set s { [ expr $b + $b ]}</td>
<td>set s &quot; [ expr $b + $b ] &quot;</td>
</tr>
<tr>
<td>puts stdout $t</td>
<td>puts stdout $t</td>
</tr>
<tr>
<td>puts stdout $s</td>
<td>puts stdout $s</td>
</tr>
</tbody>
</table>

will output
1 $b 3 vs. 1 2 3
[ expr $b + $b ] 4

Filenames
In Tcl syntax, filenames should be enclosed in braces {} to avoid backslash substitution and white space separation. Backslashes are used to separate folder names in Windows-based filenames. The problem is that sequences of "\n" or "\t" are interpreted specially. Using the braces disables this special interpretation and specifies that the Tcl interpreter handle the enclosed string literally. Alternatively, double-backslash "\"n" and "\"t" would work as well as forward slash directory separators "/n" and "/t". For example, to specify a file on your Windows PC at c:\newfiles\thisfile.adb, use one of the following:

{C:\newfiles\thisfile.adb}
C:\\newfiles\\thisfile.adb
"C:\newfiles\thisfile.adb"
C:/newfiles/thisfile.adb
"C:/newfiles/thisfile.adb"

If there is white space in the filename path, you must use either the braces or double-quotes. For example:

C:\program data\thisfile.adb

should be referenced in Tcl script as

{C:\program data\thisfile.adb} or "C:\\program data\\thisfile.adb"

If you are using variables, you cannot use braces {} because, by default, the braces turn off all special interpretation, including the dollar sign character. Instead, use either double-backslashes or forward slashes with double quotes. For example:

"$d\esign_name.adb"

Note: To use a name with special characters such as square brackets [], you must put the entire name between curly braces {} or put a slash character \ immediately before each square bracket.

The following example shows a port name enclosed with curly braces:

pin_assign -port {LFSR_OUT[15]} -iostd lvttl -slew High

The next example shows each square bracket preceded by a slash:

pin_assign -port LFSR_OUT\[15\] -iostd lvttl -slew High
Lists and arrays

A list is a way to group data and handle the group as a single entity. To define a list, use curly braces { } and double quotes " ". For example, the following set command `{1 2 3}`, when followed by the list command, creates a list stored in the variable "a." This list will contain the items "1," "2," and "3."

```
set a {1 2 3}
```

Here's another example:
```
set e 2
set f 3
set a [list b c d [expr $e + $f]]
puts $a
```

displays (or outputs):
```
b c d 5
```

Tcl supports many other list-related commands such as lindex, linsert, llength, lrange, and lappend. For more information, refer to one of the books or web sites available on this subject.

Arrays

An array is another way to group data. Arrays are collections of items stored in variables. Each item has a unique address that you use to access it. You do not need to declare them nor specify their size.

Array elements are handled in the same way as other Tcl variables. You create them with the set command, and you can use the dollar sign ($) for their values.

```
set myarray(0) "Zero"
set myarray(1) "One"
set myarray(2) "Two"
for {set i 0} {$i < 3} {incr i 1} {
    puts $i
}
```

Output:
```
Zero
One
Two
```

In the example above, an array called "myarray" is created by the set statement that assigns a value to its first element. The for-loop statement prints out the value stored in each element of the array.

Special arguments (command-line parameters)

You can determine the name of the Tcl script file while executing the Tcl script by referring to the $argv0 variable.
```
puts "Executing file $argv0"
```

To access other arguments from the command line, you can use the lindex command and the argv variable:

```
To read the Tcl file name:
lindex $argv 0
To read the first passed argument:
lindex $argv 1
```

Example
```
puts "Script name is $argv0" ; # accessing the scriptname
puts "first argument is [lindex $argv 0]"
puts "second argument is [lindex $argv 1]"
puts "third argument is [lindex $argv 2]"
puts "number of argument is [llength $argv]"
set des_name [lindex $argv 0]
puts "Design name is $des_name"
```
Control structures

Tcl control structures are commands that change the flow of execution through a script. These control structures include commands for conditional execution (if-then-else-if-else) and looping (while, for, catch).

An "if" statement only executes the body of the statement (enclosed between curly braces) if the Boolean condition is found to be true.

if/else statements

```tcl
if { "$name" == "paul" } then {
    ...
    # body if name is paul
} elseif { $code == 0 } then {
    ...
    # body if name is not paul and if value of variable code is zero
} else {
    ...
    # body if above conditions is not true
}
```

for loop statement

A "for" statement will repeatedly execute the body of the code as long as the index is within a specified limit.

```tcl
for { set i 0 } { $i < 5 } { incr i } {
    ...
    # body here
}
```

while loop statement

A "while" statement will repeatedly execute the body of the code (enclosed between the curly braces) as long as the Boolean condition is found to be true.

```tcl
while { $p > 0 } {
    ...
}
```

catch statement

A "catch" statement suspends normal error handling on the enclosed Tcl command. If a variable name is also used, then the return value of the enclosed Tcl command is stored in the variable.

```tcl
catch { open "$inputFile" r } myresult
```

Print statement and Return values

Print Statement

Use the puts command to write a string to an output channel. Predefined output channels are "stdout" and "stderr." If you do not specify a channel, then puts display text to the stdout channel.

Note: The STDIN Tcl command is not supported by Microsemi SoC tools.

Example:

```tcl
set a [ myprog arg1 arg2 ]
puts "the answer from myprog was $a (this text is on stdout)"
puts stdout "this text also is on stdout"
```
Return Values
The return code of a Tcl command is a string. You can use a return value as an argument to another function by enclosing the command with square brackets [ ].

Example:
```tcl
set a [ prog arg1 arg2 ]
exec $a
```

The Tcl command "exec" will run an external program. The return value of "exec" is the output (on stdout) from the program.

Example:
```tcl
set tmp [ exec myprog ]
puts stdout $tmp
```

Exporting Tcl Scripts
You can write out a Tcl script file that contains the commands executed in the current session. You can then use this exported Tcl script to re-execute the same commands interactively or in batch. You can also use this exported script to become more familiar with Tcl syntax.

You can export Tcl scripts from the Project Manager.

To export a Tcl session script from the Project Manager:
1. From the File menu, choose Export Script File. The Export Script dialog box appears.
2. Click OK. The Script Export Options dialog box appears:

![Figure 1 - Script Export Options](image)

3. Check the Include Commands from Current Design [Project] Only checkbox. This option applies only if you opened more than one design or project in your current session. If so, and you do not check this box, Project Manager exports all commands from your current session.
4. Select the radio button for the appropriate filename formatting. To export filenames relative to the current working directory, select Relative filenames (default) formatting. To export filenames that include a fully specified path, select Qualified filenames (full path; including directory name) formatting.

Choose Relative filenames if you do not intend to move the Tcl script from the saved location, or Qualified filenames if you plan to move the Tcl script to another directory or machine.
5. Click OK.

Project Manager saves the Tcl script with the specified filename.
Note:

- When exporting Tcl scripts, Project Manager always encloses filenames in curly braces to ensure portability.
- Libero SoC software does not write out any Tcl variables or flow-control statements to the exported Tcl file, even if you had executed the design commands using your own Tcl script. The exported Tcl file only contains the tool commands and their accompanying arguments.

extended_run_lib

Note: This is not a Tcl command; it is a shell script that can be run from the command line.
The extended_run_lib Tcl script enables you to run the multiple pass layout in batch mode from a command line.

```
$ACTEL_SW_DIR/bin/libero script:$ACTEL_SW_DIR/scripts/extended_run_lib.tcl
```

Note:

- There is no option to save the design files from all the passes. Only the (Timing or Power) result reports from all the passes are saved.

Arguments

- `-root path/designer/module_name`
The path to the root module located under the designer directory of the Libero project.

  `-n numPasses`
Sets the number of passes to run. The default number of passes is 5.

  `-starting_seed_index numIndex`
Indicates the specific index into the array of random seeds which is to be the starting point for the passes. Value may range from 1 to 100. If not specified, the default behavior is to continue from the last seed index that was used.

  `-compare_criteria value`
Sets the criteria for comparing results between passes. The default value is set to frequency when the `-c` option is given or timing constraints are absent. Otherwise, the default value is set to violations.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>frequency</td>
<td>Use clock frequency as criteria for comparing the results between passes. This option can be used in conjunction with the <code>-c</code> option (described below).</td>
</tr>
<tr>
<td>violations</td>
<td>Use timing violations as criteria for comparing the results between passes. This option can be used in conjunction with the <code>-analysis</code>, <code>-slack_criteria</code> and <code>-stop_on_success</code> options (described below).</td>
</tr>
<tr>
<td>power</td>
<td>Use total power as criteria for comparing the results between passes, where lowest total power is the goal.</td>
</tr>
</tbody>
</table>

  `-c clockName`
Applies only when the clock frequency comparison criteria is used. Specifies the particular clock that is to be examined. If no clock is specified, then the slowest clock frequency in the design in a given pass is used. The clock name should match with one of the Clock Domains in the Summary section of the Timing report.

  `-analysis value`
Applies only when the timing violations comparison criteria is used. Specifies the type of timing violations (the slack) to examine. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>max</td>
<td>Examines timing violations (slack) obtained from maximum delay analysis. This is the default.</td>
</tr>
<tr>
<td>min</td>
<td>Examines timing violations (slack) obtained from minimum delay analysis.</td>
</tr>
</tbody>
</table>

[-slack_criteria value]
Applies only when the timing violations comparison criteria is used. Specifies how to evaluate the timing violations (slack). The type of timing violations (slack) is determined by the -analysis option. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>worst</td>
<td>Sets the timing violations criteria to Worst slack. For each pass obtains the most amount of negative slack (or least amount of positive slack if all constraints are met) from the timing violations report. The largest value out of all passes will determine the best pass. This is the default.</td>
</tr>
<tr>
<td>tns</td>
<td>Sets the timing violations criteria to Total Negative Slack (tns). For each pass it obtains the sum of negative slack values from the first 100 paths from the timing violations report. The largest value out of all passes determines the best pass. If no negative slacks exist for a pass, then the worst slack is used to evaluate that pass.</td>
</tr>
</tbody>
</table>

[-stop_on_success]
Applies only when the timing violations comparison criteria is used. The type of timing violations (slack) is determined by the -analysis option. Stops running the remaining passes if all timing constraints have been met (when there are no negative slacks reported in the timing violations report).

[-timing_driven|-standard]
Sets layout mode to timing driven or standard (non-timing driven). The default is -timing_driven or the mode used in the previous layout command.

[-power_driven value]
Enables or disables power-driven layout. The default is off or the mode used in the previous layout command. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>off</td>
<td>Does not run power-driven layout.</td>
</tr>
<tr>
<td>on</td>
<td>Enables power-driven layout.</td>
</tr>
</tbody>
</table>

[-placer_high_effort value]
Sets placer effort level. The default is off or the mode used in the previous layout command. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>off</td>
<td>Runs layout in regular effort.</td>
</tr>
<tr>
<td>on</td>
<td>Activates high effort layout mode.</td>
</tr>
</tbody>
</table>
Return

A non-zero value will be returned on error.

Exceptions

None

See Also

Place and Route - PolarFire
Multiple Pass Layout - PolarFire

Sample Tcl Script - Project Manager

The following Tcl commands create a new project and set your project options.

```
new_project -location [D:/2Work/my_pf_proj] -name {my_pf_proj} -project_description {}
    -block_mode 0 -standalone_peripheral_initialization 0 -use_enhanced_constraint_flow 1
    -hdl {VERILOG} -family {PolarFire} -die {MPP300TS_ES} -package {FGG1152} -speed {-1}
    -die_voltage {1.0} -part_range {EXT} -adv_options {IO_DEFT_STD:LVCMOS 1.8V}
    -adv_options {RESTRICTPROBEPIBS:1} -adv_options {RESTRICTSPIPINS:0}
    -adv_options {SYSTEM_CONTROLLER_SUSPEND_MODE:1} -adv_options {TEMPR:EXT}
    -adv_options {VCCI_1_2_VOLTR:EXT} -adv_options {VCCI_1_5_VOLTR:EXT}
    -adv_options {VCCI_1_8_VOLTR:EXT} -adv_options {VCCI_2_5_VOLTR:EXT}
    -adv_options {VCCI_3_3_VOLTR:EXT} -adv_options {VOLTR:EXT}

#Import HDL source file
import_files -convert_EDN_to_HDL 0 -hdl_source {C:/test/prep1.v}
#Import HDL stimulus file
import_files -convert_EDN_to_HDL 0 -stimulus {C:/test/prep1tb.v}
#set the top level design name
set_root -module {prep1::work}
#Associate SDC constraint file to Place and Route tool
organize_tool_files -tool {PLACEROUTE} -file {D:/2Work/my_pf_proj/constraint/user.sdc}
    -module {prep1::work} -input_type {constraint}
#Associate SDC constraint file to Verify Timing tool
organize_tool_files -tool {VERIFYTIMING} -file {D:/2Work/my_pf_proj/constraint/user.sdc}
    -module {prep1::work} -input_type {constraint}
#Run synthesize
run_tool -name {SYNTHESIZE}
#Configure Place and Route tool
configure_tool -name {PLACEROUTE} -params {DELAY_ANALYSIS:MAX} -params {EFFORT_LEVEL:false}
    -params {INCRPLACEANDROUTE:false} -params {MULTI_PASS_CRITERIA:VIOLATIONS}
    -params {MULTI_PASS_LAYOUT:FAIL} -params {NUM_MULTI_PASSES:5} -params {PDPR:false}
    -params {RANDOM_SEED:0} -params {REPAIR_MIN_DELAY:0} -params {SLACK_CRITERIA:WORST_SLACK}
    -params {SPECIFIC_CLOCK:} -params {START_SEED_INDEX:1} -params {STOP_ON_FIRST_PASS:0}
    -params {TDPR:true}
#Run Place and Route
run_tool -name {PLACEROUTE}
#Configure Timing Report Generation
configure_tool -name {VERIFYTIMING} -run_tool -name {PLACEROUTE}params
    {CONSTRAINTS_COVERAGE:1}
        -params {FORMAT:XML} -params {MAX_TIMING_FAST_HV_LT:0} -params {MAX_TIMING_SLOW_LV_HT:0}
        -params {MAX_TIMING_SLOW_LV_LT:0} -params {MAX_TIMING_VIOLATIONS_FAST_HV_LT:0}
        -params {MAX_TIMING_VIOLATIONS_SLOW_LV_HT:0} -params {MAX_TIMING_VIOLATIONS_SLOW_LV_LT:0}
        -params {MIN_TIMING_FAST_HV_LT:0} -params {MIN_TIMING_SLOW_LV_HT:0} -params
```
How to Derive Required Part Information from A "Part Number"

In order to use Tcl Commands such as `set_device` or `new_design`; certain part information items must be specified. Many of these items can be derived from the "Part Number" you have chosen. For example, suppose the Part Number is: **MPF300XT-1FCG784I**

- **family** <family name>
The <family name> usually known, e.g.
   -family {PolarFire}

- **die** <die name>
From the Part Number, the characters before the ":-": **MPF300XT-1FCG784I**
   -die {MPF300XT}

- **speed** <speed grade>
If there is a digit immediately after the ":-", `<digit>` will be the <speed grade> value (preceded by a "-"). In this case: **MPF300XT-1FCG784I**
   -speed {-1}
      - **NOTE:** If there is no digit, the default speed grade is STD.

- **package** <package name>
The next sequence of letters, followed by a sequence of digits will constitute the package type and "size". 
**NOTE:** If there is a trailing letter after the <digits>; this letter is not part of the <package name>; but is rather part of the <part_range> (see below).
   - For PolarFire, this combination will simply constitute the <package name> e.g.: **MPF300XT-1FCG784I**
      -package {FCG784}

- **part_range** <part range>
The last letter (if any) will indicate the <part_range> according to the following table:

<table>
<thead>
<tr>
<th>last letter</th>
<th>expansion value</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>IND</td>
</tr>
<tr>
<td>E</td>
<td>EXT</td>
</tr>
<tr>
<td>M</td>
<td>MIL</td>
</tr>
<tr>
<td>&lt;none&gt;</td>
<td>COM</td>
</tr>
</tbody>
</table>

- **In this case:** **MPF300XT-1FCG784I**
   -part_range {IND}
add_file_to_library

Tcl command; adds a file to a library in your project.

```
add_file_to_library
-library name
-file name
```

Arguments

- **-library name**
  Name of the library where you wish to add your file.
- **-file name**
  Specifies the new name of the file you wish to add (must be a full pathname).

Example

Add a file named foo.vhd from the ./project/hdl directory to the library 'my_lib'
```
add_file_to_library -library my_lib -file ./project/hdl/foo.vhd
```

See Also

add_library
remove_library
rename_library

add_library

Tcl command; adds a VHDL library to your project.

```
add_library
-library name
```

Arguments

- **-library name**
  Specifies the name of your new library.

Example

Create a new library called 'my_lib'.
```
add_library -library my_lib
```

See Also

remove_library
rename_library

add_modelsim_path

Tcl command; adds a ModelSim simulation library to your project.
add_modelsim_path -lib library_name [-path library_path] [-remove " "]

Arguments

- lib library_name
  Name of the library you want to add.
- path library_path
  Path to library that you want to add.
- remove " 
  Name of library you want to remove (if any).

Example

Add the ModelSim library 'msim_update2' located in the c:\modelsim\libraries directory and remove the library 'msim_update1':

```
add_modelsim_path -lib msim_update2 [-path c:\modelsim\libraries] [-remove msim_update1]
```

add_profile

Tcl command; sets the same values as the Add or Edit Profile dialog box. The newly added profile becomes the active tool profile for the specified type of tool.

```
add_profile -name profilename -type value -tool profiletool -location tool_location [-args tool_parameters] [-batch value]
```

Arguments

- name profilename
  Specifies the name of your new profile.
- type value
  Specifies your profile type, where value is one of the following:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>synthesis</td>
<td>New profile for a synthesis tool</td>
</tr>
<tr>
<td>simulation</td>
<td>New profile for a simulation tool</td>
</tr>
<tr>
<td>stimulus</td>
<td>New profile for a stimulus tool</td>
</tr>
<tr>
<td>flashpro</td>
<td>New FlashPro tool profile</td>
</tr>
</tbody>
</table>

- tool profiletool
  Name of the tool you are adding to the profile.
- location tool_location
  Full pathname to the location of the tool you are adding to the profile.
- args tool_parameters
  Profile parameters (if any).
- batch value
  Runs the tool in batch mode (if TRUE). Possible values are:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TRUE</td>
<td>Runs the profile in batch mode</td>
</tr>
<tr>
<td>Value</td>
<td>Description</td>
</tr>
<tr>
<td>---------</td>
<td>---------------------------</td>
</tr>
<tr>
<td>FALSE</td>
<td>Does not run the profile in batch mode</td>
</tr>
</tbody>
</table>

**Example**

Create a new Synthesis tool profile called 'synpol' linked to a Synplify Pro ME installation in my /sqatest/bin directory:

```bash
add_profile -type synthesis -name synpol -tool "Synplify Pro ME" -location "/sqatest9/bin/synplify_pro" -batch FALSE
```

**associate_stimulus**

Tcl command; associates a stimulus file in your project.

```bash
 associate_stimulus
 [-file name]*
 [-mode value]
 -module value
```

**Arguments**

- **-file name**
  Specifies the name of the file to which you want to associate your stimulus files.

- **-mode value**
  Specifies whether you are creating a new stimulus association, adding, or removing; possible values are:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>new</td>
<td>Creates a new stimulus file association</td>
</tr>
<tr>
<td>add</td>
<td>Adds a stimulus file to an existing association</td>
</tr>
<tr>
<td>remove</td>
<td>Removes an stimulus file association</td>
</tr>
</tbody>
</table>

- **-module value**
  Sets the module, where value is the name of the module.

**Example**

The example associates a new stimulus file 'stim.vhd' for stimulus.

```bash
associate_stimulus -file stim.vhd -mode new -module stimulus
```

**change_link_source**

Tcl command; changes the source of a linked file in your project.

```bash
 change_link_source -file filename -path new_source_path
```

**Arguments**

- **-file filename**
  Name of the linked file you want to change.

- **-path new_source_path**
  Location of the file you want to link to.
Example

Change the link to a file 'sim1.vhd' in your project and link it to the file in
\c:\microsemi\link_source\simulation_test.vhd

```
change_link_source -file sim1.vhd -path c:\microsemi\link_source\simulation_test.vhd
```

check_fdc_constraints

This Tcl command checks FDC constraints files associated with the Synthesis tool.

```
check_fdc_constraints -tool {synthesis}
```

Arguments

- -tool {synthesis}

Example

```
check_fdc_constraints -tool {synthesis}
```

Return Value

This command returns "0" on success and "1" on failure.

check_hdl

Tcl command; checks the HDL in the specified file.

```
check_hdl -file filename
```

Arguments

- -file filename
  Name of the HDL file you want to check.

Example

```
Check HDL on the file hdl1.vhd.
check_hdl -file hdl1.vhd
```

check_ndc_constraints

This Tcl command checks NDC constraints files associated with the Synthesis tool. NDC constraints are used to optimize the post-synthesis netlist with the Libero SoC Compile engine.

```
check_ndc_constraints -tool {synthesis}
```

Arguments

- -tool {synthesis}

Example

```
check_ndc_constraints -tool {synthesis}
```

check_pdc_constraints

This Tcl command checks PDC constraints files associated with the Libero Place and Route tool.

```
check_pdc_constraints -tool {designer}
```
Arguments
- tool {designer}

Example
check_pdc_constraints -tool {designer}

Return Value
This command returns "0" on success and "1" on failure.

check_sdc_constraints
This Tcl command checks SDC constraints files associated with the Libero tools: designer, synthesis, or timing.
check_sdc_constraints -tool {tool_name}

Arguments
- tool {synthesis|designer|timing}

Example
This command checks the SDC constraint files associated with Timing Verification.
check_sdc_constraints -tool {timing}
This command checks the SDC constraint files associated with Place and Route.
check_sdc_constraints -tool {designer}
This command checks the SDC constraint files associated with Synthesis.
check_sdc_constraints -tool {synthesis}

Return Value
The command returns "0" on success and "1" on failure.

close_design
Tcl command; closes the current design and brings Designer to a fresh state to work on a new design.
This is equivalent to selecting the Close command from the File menu.
close_design

Arguments
None

Example
if { [catch { close_design }] } {
    puts "Failed to close design"
    # Handle Failure
} else {
    puts "Design closed successfully"
    # Proceed with processing a new design
}

See Also
open_design
close_project

Tcl command; closes the current project in Libero SoC. Equivalent to clicking the File menu, and choosing Close Project.

Arguments

None

Example

close_project

See Also

open_project

configure_tool

configure_tool is a general-purpose Tcl command that is used to set the parameters for any tool called by Libero. The command requires the name of the tool and one or more parameters in the format `toolParameter:Value`. These parameters are separated and passed to the tool to set up its run.

configure_tool

- `name` `<tool_name>` # Each tool_name has its own set of parameters
- `params` `<parameter>:<value>` # List of parameters and values

`tool_name ::=  CONFIGURE_PROG_OPTIONS | SYNTHESIZE | PLACEROUTE |
GENERATEPROGRAMMINGFILE | PROGRAMDEVICE | PROGRAMMER_INFO | IO_PROGRAM_STATE | SPM | VERIFYTIMING | PROGRAM_SPI_FLASH_IMAGE | SPM_OTP`

Supported tool_names

The following table lists the supported tool_names.

<table>
<thead>
<tr>
<th>tool_name</th>
<th>Parameter (-params)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>&quot;CONFIGURE_PROG_OPTIONS&quot; on page 94</td>
<td>See the topic for parameter names and values.</td>
<td>See the topic for description.</td>
</tr>
<tr>
<td>SYNTHESIZE</td>
<td>See the topic for parameter names and values.</td>
<td>See the topic for description.</td>
</tr>
<tr>
<td>PLACEROUTE</td>
<td>See the topic for parameter names and values.</td>
<td>See the topic for description.</td>
</tr>
<tr>
<td>&quot;GENERATEPROGRAMMINGFILE&quot; on page 94</td>
<td>See the topic for parameter names and values.</td>
<td>See the topic for description.</td>
</tr>
<tr>
<td>PROGRAMDEVICE</td>
<td>See the topic for parameter names and values.</td>
<td>See the topic for description.</td>
</tr>
<tr>
<td>PROGRAMMER_INFO</td>
<td>See the topic for parameter names and values.</td>
<td>See the topic for description.</td>
</tr>
<tr>
<td>tool_name</td>
<td>Parameter (-params)</td>
<td>Description</td>
</tr>
<tr>
<td>-------------------------</td>
<td>---------------------</td>
<td>--------------------------------------</td>
</tr>
<tr>
<td>IO_PROGRAMMING_STATE</td>
<td>See the topic for parameter names and values. See the topic for description.</td>
<td></td>
</tr>
<tr>
<td>SPM</td>
<td>See the topic for parameter names and values. See the topic for description.</td>
<td></td>
</tr>
<tr>
<td>VERIFYTIMING</td>
<td>See the topic for parameter names and values. See the topic for description.</td>
<td></td>
</tr>
<tr>
<td>“PROGRAM_SPI_FLASH_IMAGE” on page 100</td>
<td>See the topic for parameter names and values. See the topic for description.</td>
<td></td>
</tr>
<tr>
<td>SPM_OTP</td>
<td>See the topic for parameter names and values. See the topic for description.</td>
<td></td>
</tr>
</tbody>
</table>

See Also
Tcl documentation conventions

**create_and_configure_core**

Tcl command; creates a configured core component for a core selected from the Libero Catalog.

To use this command to create a configured core component with valid parameters and values, it is recommended to use the GUI to configure the core as desired. Then export the core configuration Tcl description by selecting the “Export Component Description(Tcl)” action on the right-click menu of the component in the Design Hierarchy. You can then use the exported Tcl command to create the configured core in a regular Tcl script.

```tcl
create_and_configure_core \
-core_vlnv Vendor:Library:Name:version \
-component_name component_name \
[-params core_parameters]
```

**Arguments**

- `core_vlnv Vendor:Library:Name:Version`
  Specifies the version identifier of the core being configured. It is mandatory.
- `component_name component_name`
  Specifies the name of the configured core component. It is mandatory.
- `[-params core_parameters]`
  Specifies the parameters that need to be configured for the core component. It is optional. If the core parameters are not specified with this argument, the component is configured and generated with the core’s default configuration. It is recommended to specify all the core parameters of interest as a part of this argument in this command.

**Examples**

```tcl
create_and_configure_core -core_vlnv {Actel:SgCore:PF_CCC:1.0.115} -component_name {PF_CCC_C3} -params {
  "PLL_IN_FREQ_0:25"
  "GL0_0_IS_USED:true"
  "GL0_0_OUT_FREQ:150"
} 
```
"GL0_1_IS_USED:true" \
"GL0_1_OUT_FREQ:50" }

Notes

For DirectCore and Solutions cores, refer to the core handbook or the core user guide for a list of valid parameters and values.

See Also

Tcl Command Documentation Conventions

create_set

Tcl command; creates a set of paths to be analyzed. Use the arguments to specify which paths to include. To create a set that is a subset of a clock domain, specify it with the -clock and -type arguments. To create a set that is a subset of an inter-clock domain set, specify it with the -source_clock and -sink_clock arguments. To create a set that is a subset (filter) of an existing named set, specify the set to be filtered with the -parent_set argument.

create_set name <name> -parent_set <name> -type <set_type> -clock <clock name> -source_clock <clock name> -sink_clock <clock name> -in_to_out -source <port/pin pattern> -sink <port/pin pattern>

Arguments

-name <name>
Specifies a unique name for the newly created path set.

-parent_set <name>
Specifies the name of the set to filter from.

-clock <clock name>
Specifies that the set is to be a subset of the given clock domain. This argument is valid only if you also specify the -type argument.

-type <value>
Specifies the predefined set type on which to base the new path set. You can only use this argument with the -clock argument, not by itself.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>reg_to_reg</td>
<td>Paths between registers in the design</td>
</tr>
<tr>
<td>async_to_reg</td>
<td>Paths from asynchronous pins to registers</td>
</tr>
<tr>
<td>reg_to_async</td>
<td>Paths from registers to asynchronous pins</td>
</tr>
<tr>
<td>external_recovery</td>
<td>The set of paths from inputs to asynchronous pins</td>
</tr>
<tr>
<td>external_removal</td>
<td>The set of paths from inputs to asynchronous pins</td>
</tr>
<tr>
<td>external_setup</td>
<td>Paths from input ports to registers</td>
</tr>
<tr>
<td>external_hold</td>
<td>Paths from input ports to registers</td>
</tr>
<tr>
<td>clock_to_out</td>
<td>Paths from registers to output ports</td>
</tr>
</tbody>
</table>

-in_to_out
Specifies that the set is based on the “Input to Output” set, which includes paths that start at input ports and end at output ports.

```tcl
-source_clock <clock_name>
```

Specifies that the set will be a subset of an inter-clock domain set with the given source clock. You can only use this option with the `-sink_clock` argument.

```tcl
-sink_clock <clock_name>
```

Specifies that the set will be a subset of an inter-clock domain set with the given sink clock. You can only use this option with the `-source_clock` argument.

```tcl
-source <port/pin_pattern>
```

Specifies a filter on the source pins of the parent set. If you do not specify a parent set, this option filters all pins in the current design.

```tcl
-sink <port/pin_pattern>
```

Specifies a filter on the sink pins of the parent set. If you do not specify a parent set, this option filters all pins in the current design.

### Examples

```tcl
create_set -name { my_user_set } -source { C* } -sink { D* }
create_set -name { my_other_user_set } -parent_set { my_user_set } -source { CL* }
create_set -name { adder } -source { ALU_CLOCK } -type { REG_TO_REG } -sink { ADDER* }
create_set -name { another_set } -source_clock { EXTERN_CLOCK } -sink_clock { MY_GEN_CLOCK }
```

### create_links

Tcl command; creates a link (or links) to a file/files in your project.

```
create_links [-hdl_source file]* [-stimulus file]* [-sdc file]* [-pin file]* [-dcf file]* [-gcf file]* [-pdc file]* [-crt file]* [-vcd file]*
```

### Arguments

- `hdl_source file`
  Name of the HDL file you want to link.

- `stimulus file`
  Name of the stimulus file you want to link.

- `sdc file`
  Name of the SDC file you want to link.

- `pin file`
  Name of the PIN file you want to link.

- `dcf file`
  Name of the DCF file you want to link.

- `gcf file`
  Name of the GCF file you want to link.

- `pdc file`
  Name of the PDC file you want to link.

- `crt file`
  Name of the crt file you want to link.

- `vcd file`
  Name of the VCD file you want to link.
Example

Create a link to the file hdl1.vhd.
create links [-hdl_source hdl1.vhd]

create_smartdesign
Tcl command; creates a SmartDesign.

create_smartdesign
  -sd_name <smartdesign_component_name>

Arguments

-sd_name <smartdesign_component_name>
Specifies the name of the SmartDesign component to be created. It is mandatory.

Examples

create_smartdesign -sd_name {top}

See Also

Tcl Command Documentation Conventions

download_core
Tcl command; downloads a core and adds it to your repository.
download_core [-vlnv "vlnv"]+ [-location "location"]

Arguments

-vlnv vlnv
Vendor, library, name and version of the core you want to download.
-location core_name
Location of the repository where you wish to add the core.

Example

Download the core CoreAXI to the repository www.actel-ip.com/repositories/SgCore:
download_core -vlnv {Actel:SystemBuilder:PF_DDR4:1.0.102} -location {www.actel-ip.com/repositories/SgCore}

download_latest_cores
This Tcl command is used to download the latest cores into the vault. A project does not need to be open to run this command.
download_latest_cores

This command takes no arguments.
If there are no cores to be downloaded, you will see the following message:
Info:All the latest cores are present in the vault.
edit_profile
Tcl command; sets the same values as the Add or Edit Profile dialog box.

```
edit_profile -name profilename -type value -tool profiletool -location profilelocation [-args parameters] [-batch value] [-new_name name]
```

Arguments

- **-name profilename**
  Specifies the name of your new profile.

- **-type value**
  Specifies your profile type, where value is one of the following:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>synthesis</td>
<td>New profile for a synthesis tool</td>
</tr>
<tr>
<td>simulation</td>
<td>New profile for a simulation tool</td>
</tr>
<tr>
<td>stimulus</td>
<td>New profile for a stimulus tool</td>
</tr>
<tr>
<td>flashpro</td>
<td>New FlashPro tool profile</td>
</tr>
</tbody>
</table>

- **-tool profiletool**
  Name of the tool you are adding to the profile.

- **-location profilelocation**
  Full pathname to the location of the tool you are adding to the profile.

- **-args parameters**
  Profile tool parameters (if any).

- **-batch value**
  Runs the tool in batch mode (if TRUE). Possible values are:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TRUE</td>
<td>Runs the profile in batch mode</td>
</tr>
<tr>
<td>FALSE</td>
<td>Does not run the profile in batch mode</td>
</tr>
</tbody>
</table>

- **-new_name name**
  Name of new profile.

Example

Edit a FlashPro tool profile called 'myflashpro' linked to a new FlashPro installation in my c:\programs\actel\flashpro\bin directory, change the name to updated_flashpro.

```
edit_profile -name myflashpro -type flashpro -tool flashpro.exe -location c:\programs\actel\flashpro\bin\flashpro.exe -batch FALSE -new_name updated_flashpro
```

export_as_link
Tcl command; exports a file to another directory and links to the file.
export_as_link -file filename -path link_path

**Arguments**
- **-file filename**
  Name of the file you want to export as a link.
- **-path link_path**
  Path of the link.

**Example**
Export the file hdl1.vhd as a link to c:\microsemi\link_source.
export_as_link -file hdl1.vhd -path c:\microsemi\link_source

export_ba_files
Tcl command to export the backannotated files. The backannotated files are <design_name>_ba.v (Verilog backannotated netlist) or <design_name>_ba.vhd (VHDL backannotated netlist) and <design_name>_ba.sdf (Standard Delay Format) timing file. These files are passed to the default simulator for postlayout simulation.

```
export_ba_files
-export_dir {absolute path to folder location}
-export_file_name {name of file}
-vhdl {value}
-min_delay {value}
```

**Arguments**
- **-export_dir {absolute path to directory/folder location}**
  Folder/directory location.
- **-export_file_name {name of file}**
  File name to generate the files. If not specified, it takes <design_name> as the default.
- **-vhdl {value}**
  Generates the <design_name>_ba.v and <design_name>_ba.sdf when set to 0 and <design_name>_ba.vhd and <design_name>_ba.sdf when set to 1. Default is 0.
- **-min_delay {value}**
  Set to 1 to export enhanced min delays to include your best-case timing results in your Back Annotated file. Default is 0.

**Returns**
Returns 0 on success, 1 on failure.

**Example**
```
export_ba_files\n-export_dir {E:\designs\export\sdl}\n-export_file_name {test}\n-vhdl 0\n-min_delay 1
```
export_bitstream_file

Configures the parameters for the bitstream to be exported from Libero.

```
export_bitstream_file
[-file_name file]
[-export_dir dir]
[-format STP | DAT | SPI]
[-master_file 0 | 1]
[-master_file_components SECURITY | FABRIC | SNVM]
[-encrypted_uek1_file 1 | 0]
[-encrypted_uek1_file_components FABRIC | SNVM]
[-encrypted_uek2_file 1 | 0]
[-encrypted_uek2_file_components FABRIC | SNVM]
[-trusted_facility_file 1 | 0]
[-trusted_facility_file_components FABRIC | SNVM]
[-zeroization_likenew_action 0 | 1]
[-zeroization_unrecoverable_action 0 | 1]
[-master_backlevel_bypass 0 | 1]
[-uek1_backlevel_bypass 0 | 1]
[-uek2_backlevel_bypass 0 | 1]
[-master_include_plaintext_passkey 0 | 1]
[-uek1_include_plaintext_passkey 0 | 1]
[-uek2_include_plaintext_passkey 0 | 1]
```

Arguments

- **-file_name file**
  The name of the file. File name must start with design name. If omitted, design name will be used.

- **-export_dir dir**
  Location where the bitstream file will be exported. If omitted, design export folder will be used.

- **-format STP | CHAIN_STP | DAT | SPI**
  Specifies the bitstream file formats to be exported. Space is used as a delimiter. If omitted, STP and DAT files will be exported.

Zeroization Options:

- **-zeroization_likenew_action 0 | 1**
  Specifies that all the data will be erased and the device can be reprogrammed immediately

- **-zeroization_unrecoverable_action 0 | 1**
  Specifies that all the data will be erased and the device cannot be reprogrammed and it must be scrapped.

Security-related options:

Note: One of the trusted_facility_file or master_file or encrypted_uek1_file or encrypted_uek2_file must be set to "1". 1 indicates that this particular file type will be exported; 0 indicates that it will not be exported. For example, if trusted_facility_file is set to 1, all other file types must be set to 0.

Or, if trusted_facility_file is set to 0, a combination of master_file and uek1_file and uek2_file can be set to 1. In this case, master_file must be set to 1.

Bitstream encryption with default key (default security):

- **-trusted_facility_file 1 | 0**
  Specifies the bitstream file to be exported.

- **-trusted_facility_file_components FABRIC | SNVM**
  Specifies the components of the design that will be saved to the bitstream file. The value can only be FABRIC and SNVM.

Custom security options:

- **-master_file 0 | 1**
Specifies the bitstream files to be exported. Depends on the selected security.
Note: If -master_file is 1, SECURITY must be selected.
-master_file_components SECURITY | FABRIC | SNVM

Specifies the components in the design that will be saved to the bitstream file. The value can be any
either SECURITY or SECURITY, FABRIC and SNVM

Notes:
1. The SECURITY option is available in -bitstream_file_components only when file type is MASTER in –
   bitstream_file_type.
2. SNVM should be programmed with FABRIC
3. Security only programming must be performed only on erased or new devices. If performed on device
   with fabric programmed, the fabric will be disabled after performing security only programming. You must
   reprogram the fabric to re-enable it.
   -encrypted_uek1_file 0 | 1
   -encrypted_uek1_file_components FABRIC | SNVM

Specifies the components of the design that will be saved to uek1 bitstream.
Note: SNVM should be programmed with FABRIC

-encrypted_uek2_file 0 | 1
-encrypted_uek2_file_components FABRIC | SNVM

Specifies the components of the design that will be saved to uek2 bitstream.
Note: SNVM should be programmed with FABRIC

-master_include_plaintext_passkey 0 | 1

Specifies that the master file includes plaintext passkey. This argument is optional.
-uek1_include_plaintext_passkey 0 | 1

Specifies that uek1 includes plaintext passkey. This argument is optional.
-uek2_include_plaintext_passkey 0 | 1

Specifies that uek2 includes plaintext passkey. This argument is optional.

Bypass Back Level Protection Options:
-master_backlevel_bypass 0 | 1

Specifies the Bypass Back Level protection for Golden/Recovery bitstream if back level protection is
enabled in _master file.
-uek1_backlevel_bypass 0 | 1

Specifies the Bypass Back Level Protection for Golden/Recovery bitstream if back level protection is
enabled in _uek1 file.
-uek2_backlevel_bypass 0 | 1

Specifies the Bypass Back Level Protection for Golden/Recovery bitstream if back level protection is
enabled in _uek2 file.

Bitstream file to be exported and the components of the design that will be saved to the bitstream file are
required.
Note: A TCL script file exported from Libero will include all command options. You can modify options you need
and remove options you do not need.

Example
Export a bitstream file:

Export bitstream file for design with default security
export_bitstream_file \ -trusted_facility_file 1
-trusted_facility_file_components {FABRIC SNVM}

Export bitstream file for design with custom security options
Export bitstreams to master, uek1 and uek2 encrypted files. Master file to include security, fabric and SNVM components and Export Pass Key in Plaintext, uek1 and uek2 encrypted files to include FABRIC and SNVM with Like new Zeroization option enabled.

```tcl
export_bitstream_file
- file_name {fftousram_new} \
- export_dir \{X:10_docs_review\pf2.2_sp1\Programming_sars\99412\clkint_fftousram_ac_latch_launch\design\fftousram_new\export\} \
- format {STP DAT} \
- master_file 1 \
- master_file_components {SECURITY FABRIC SNVM} \ 
- encrypted_uek1_file 1 \ 
- encrypted_uek1_file_components {FABRIC SNVM} \ 
- encrypted_uek2_file 1 \ 
- encrypted_uek2_file_components {FABRIC SNVM} \ 
- trusted_facility_file 0 \ 
- trusted_facility_file_components {} \ 
- zeroization_likenew_action 1 \ 
- zeroization_unrecoverable_action 0 \ 
- master_backlevel_bypass 0 \ 
- uek1_backlevel_bypass 0 \ 
- uek2_backlevel_bypass 0 \ 
- master_include_plaintext_passkey 1 \ 
- uek1_include_plaintext_passkey 0 \ 
- uek2_include_plaintext_passkey 0
```

**export bsdl_file**

Tcl command to export the BSDL to a specified file. The exported file has a *.bsd file name extension.

```tcl
export bsdl_file
- file {absolute path and name of BSDL file}
```

**Arguments**

- `file {absolute path and name of BSDL file}`

  Specifies the *.bsd file.

**Returns**

Returns 0 on success, 1 on failure.

**Example**

```tcl
export bsdl_file
- file {E:/designs/export/sd1.bsd}
```

**export_component_to_tcl**

Tcl command; exports the Tcl command for the selected component. The components can be SmartDesign components, configured cores and HDL+ cores.

```tcl
export_component_to_tcl \
- component component_name \ 
[ -library library_name ]
```
[-package package_name] 
-file file_path

**Arguments**

- **component component_name**
  Specifies the name of the component for which the Tcl command is exported. It is mandatory.
- **library library_name**
  Specifies the name of the library the component belongs to. It is optional.
- **package package_name**
  Specifies the name of the package the HDL+core belongs to. It is optional.
- **file file_path**
  Specifies the path where you wish to export the Tcl file. It is mandatory.

**Example**

```
export_component_to_tcl -component {pattern_gen_checker} -library {work} -package {} -file {./pattern_gen_checker.tcl}
```

**export_design_summary**

This Tcl command exports an HTML file containing information about your root SmartDesign in your project. The HTML report provides information on:

- Generated Files
- I/Os
- Hardware Instances
- Firmware
- Memory Map

```
export_design_summary -file {D: /Designs/test/sd1.html}
```

**Returns**

Returns 0 on success, 1 on failure.

**export_fp_pdc**

Tcl command to export the Floorplanning Physical Design Constraint (*.pdc) File. The exported file has a *.fp.pdc file name extension.

```
export_fp_pdc
-file {absolute path and name of *.fp.pdc file}
-mode {PDC_PLACE | PDC_FULL_PLACEMENT}
```

**Arguments**

- **file {absolute path and name of *.fp.pdc file}**
  Specifies the *.fp.pdc file.
- **mode {PDC_PLACE | PDC_FULL_PLACEMENT}**
  Use PDC_PLACE to export user’s floorplanning constraints, for example, fixed logic and regions.
  Use PDC_FULL_PLACEMENT to export information about all of the physical design constraints (I/O constraints, I/O Banks, routing constraints, region constraints, global and local clocks).
Returns
Returns 0 on success, 1 on failure.

Example
```tcl
export_fp_pdc
   -file {E:/designs/export/sd1_fp.pdc}\n   -mode {PDC_FULL_PLACEMENT}
```

export_ibis_file
Tcl command to export the IBIS (Input/Output Buffer Information Specification) model report. The exported file has a *.ibs file name extension.

```
export_ibis_file
   -file {absolute path and name of *.ibs file}
```

Arguments
- `file {absolute path and name of *.ibs file}`
  Specifies the IBIS file to export.

Returns
Returns 0 on success, 1 on failure.

Example
```tcl
export_ibis_file
   -file {E:/designs/export/sd1.ibs}
```

export_io_pdc
Tcl command to export the I/O constraints Physical Design Constraint (*.pdc) File. The exported file has a *_io.pdc file name extension.

```
export_io_pdc
   -file {absolute path and name of *_io.pdc file}
```

Arguments
- `file {absolute path and name of *_io.pdc file}`
  Specifies the *_io.pdc file.

Returns
Returns 0 on success, 1 on failure.

Example
```tcl
export_io_pdc
   -file {E:/designs/export/sd1_io.pdc}
```
export_netlist_file

Tcl command to export the netlist after the compile state has completed. The netlist can be either Verilog or VHDL. Microsemi recommends exporting the netlist after the compile state has successfully completed.

```tcl
export_netlist_file
-file {absolute path and filename for netlist}
-vhdl {value}
```

Arguments
- `file {absolute path and filename}`
  Specifies the path and name of netlist file.
- `vhdl {value}`
  Generates the netlist in VHDL (when set to 1) or Verilog (when set to 0). Default is 0 (Verilog netlist).

Returns
Returns 0 on success, 1 on failure.

Example
```tcl
export_netlist_file
-file {E:/designs/export/sd1/sd1.v}
-vhdl 0
```

export_pin_reports

Tcl command to configure and export a pin report file to a specified folder/directory location.

```tcl
export_pin_reports
-export_dir {absolute path to folder location}
-pin_report_by_name {value}
-pin_report_by_pkg_pin {value}
-bank_report {value}
-io_report {value}
```

Arguments
- `export_dir {absolute or relative path to the folder for pin report file}`
  Specifies the folder.
- `pin_report_by_name {value}`
  Set to 1 to have the pin report sorted by pin name. Default is 1.
- `pin_report_by_pkg_pin {value}`
  Set to 1 to have pin report sorted by package pin number, 0 to not sort by package pin number. Default is 1.
- `bank_report {value}`
  Set to 1 to generate the I/O bank report, 0 to not generate the report. Default is 1.
- `io_report {value}`
  Set to 1 to generate the I/O report, 0 to not generate the report. Default is 1.

At least one argument must be specified for this command.

Returns
Returns 0 on success, 1 on failure.
Example

```tcl
export_pin_reports
-export_dir {E:/designs/export}
-pin_report_by_name {1}
-pin_report_by_pkg_pin {0}
-bank_report {1}
-io_report {1}
```

**export_profiles**

Tcl command; exports your tool profiles. Performs the same action as the Export Profiles dialog box.

```
export_profile -file name [-export value]
```

**Arguments**

- **-file name**
  Specifies the name of your exported profile.
- **-export value**
  Specifies your profile export options. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>predefined</td>
<td>Exports only predefined profiles</td>
</tr>
<tr>
<td>user</td>
<td>Exports only user profiles</td>
</tr>
<tr>
<td>all</td>
<td>Exports all profiles</td>
</tr>
</tbody>
</table>

Example

The following command exports all profiles to the file 'all_profiles':

```tcl
export_profiles -file all_profiles [-export all]
```

**export_prog_job**

Tcl command; configures the parameters for the FlashPro Express programming job to be exported.

```
export_prog_job
-job_file_name file
-export_dir dir
-bitstream_file_type TRUSTED_FACILITY | MASTER | UEK1 | UEK2
-bitstream_file_components SECURITY | FABRIC | SNVM
-zeroization likenew_action 0 | 1
-zeroization unrecoverable_action 0 | 1
-program_design 0 | 1
-program_spi_flash 0 | 1
-include_plaintext_passkey 0 | 1
```

**Arguments**

- **-job_file_name file**
  The name of the file. Name must start with design name. If omitted, design name will be used.
-export_dir  
dir
Location where the job file will be saved; any folder can be specified. The default folder is the Libero
export folder.

-bitstream_file_type  TRUSTED_FACILITY | MASTER | UEK1 | UEK2
Bitstream file to be included in the programming job. Only one bitstream file can be included in a
programming job.

-bitstream_file_components  SECURITY | FABRIC | SNVM
The list of components to be included in the programming job. Components should be delimited by space.
bitstream_file_components can be any one of SECURITY or SECURITY, FABRIC and SNVM

Notes:
1. The SECURITY option is available in -bitstream_file_components only when file type is MASTER in –
bitstream_file_type.
2. SNVM must always be programmed with FABRIC.
3. Security-only programming must be performed only on erased or new devices. If performed on a device
with fabric programmed, the fabric will be disabled after performing security-only programming. You must
reprogram the fabric to re-enable it.

-zeroization_likenew_action 0 | 1
Specifies that all data will be erased and the device can be reprogrammed immediately.

-zeroization_unrecoverable_action 0 | 1
Specifies that all data will be erased. The device cannot be reprogrammed and it must be scrapped.

-program_design 0 | 1
Specifies to program the design. This argument is optional.

-program_spi_flash 0 | 1
Specifies to program SPI Flash. This argument is optional.

-include_plaintext_passkey 0 | 1
Specifies to include plaintext passkey. This argument is optional.

Example

export_prog_job \  
-job_file_name {fftousram_new} \  
-export_dir \{X:\10_docs_review\12.0_Release\102018\clkint_fftousram_ac_latch_launch\designer\fftousram_new\export\} \ 
-bitstream_file_type {MASTER} \ 
-bitstream_file_components {SECURITY FABRIC SNVM} \ 
-zeroization_likenew_action 0 \ 
-zeroization_unrecoverable_action 0 \ 
-program_design 1 \ 
-program_spi_flash 0 \ 
-include_plaintext_passkey 0

export_script

Tcl command; export_script is a command that explicitly exports the Tcl command equivalents of the current
Libero session. You must supply a file name with the -file parameter. You may supply the optional -relative_path
parameter to specify whether an absolute or relative path is used in the exported script file.

export_script\  
-file {<absolute or relative path to constraint file>} \ 
-relative_path <value> \
Arguments

- `file {<absolute or relative path to constraint file>}`
  Specifies the absolute or relative path to the constraint file; there may be multiple `file` arguments (see example below).
- `relative_path {<value>}`
  Sets your option to use a relative or absolute path in the exported script; use 1 for relative path, 0 for absolute.

Example

```
export_script -file {./exported.tcl} -relative_path 1
```

generate_component

Tcl command; generates a SmartDesign or a core component.

```
generate_component \
- component_name component_name \
[-recursive 0|1]
```

Arguments

- `component_name component_name`
  Specifies the name of the SmartDesign component or the core component to be generated. It is mandatory.
- `recursive 0|1`
  Specifies if a SmartDesign component needs to be generated recursively. It is optional. It is ‘0’ by default and generates only the specified component. If set to ‘1’, all the dependent components which are in ungenerated state will be generated along with the SmartDesign component. It is recommended to generate all components individually.

Examples

The following command generates SmartDesign “sd2” only.
```
generate_component -component_name {sd2}
```

The following command generates SmartDesign “TOP” and all its dependent components which are in ungenerated state.
```
generate_component -component_name {TOP} -recursive 1
```

See Also

Tcl Command Documentation Conventions

generate_sdc_constraint_coverage

Tcl command to generate the constraint coverage report. The constraint coverage report contains information about the coverage of the paths from associated SDC constraints in the design. Two constraints coverage reports can be generated, one for Place and Route and one for Timing Verification.

This command is available for the Enhanced Constraint Flow only. To run this command, there is no need to run Place-and-Route first, but the design must be in the post-synthesis state. The generated constraint coverage reports (*.xml) are listed in the Reports tab and are physically located in `<prj_folder>/designer/<module>/*constraints_coverage.xml`.

```
generate_sdc_constraint_coverage -tool {PLACEROUTE | VERIFYTIMING}
```
Arguments

-tool {PLACEROUTE|VERIFYTIMING}

Specifies whether the constraint coverage report is based on the SDC constraint file associated with Place and Route or associated with Timing Verification.

Returns

Returns 0 on success, 1 on failure.

Example

This command generates the SDC Constraint Coverage report for the SDC file associated with Place and Route:

generate_sdc_constraint_coverage -tool {PLACEROUTE}

This command generates the SDC Constraint Coverage report for the SDC file associated with Timing Verification:

generate_sdc_constraint_coverage -tool {VERIFYTIMING}

See Also

Understanding Constraints Coverage Reports

import_files (Libero SoC)

Tcl command; enables you to import design source files and constraint files.

**SmartFusion2, IGLOO2, RTG4, PolarFire**: For importing constraint files, import_files has retired the -pdc parameter for SmartFusion2 and IGLOO2. It has been replaced with two new parameters to match the new design flow. Physical Design Constraints (PDC) Tcl must now be divided between I/O attribute and pin information from all floorplanning and timing constraints. These commands must now reside in and be imported as separate files. The new parameters specify the type of *.pdc file being imported.

Use of the -pdc parameter with SmartFusion2 or IGLOO2 families will cause an error. The path to the file can be absolute or relative but must be enclosed in curly braces `{}`.

Use the -can_convert_EDN_to_HDL parameter to convert the EDIF file to HDL and then import the converted HDL file.

Note: The EDIF File is not imported.

<table>
<thead>
<tr>
<th>Argument</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>-smartgen_core</td>
<td></td>
</tr>
<tr>
<td>-ccp</td>
<td></td>
</tr>
<tr>
<td>-stimulus</td>
<td></td>
</tr>
<tr>
<td>-hdl_source</td>
<td></td>
</tr>
<tr>
<td>-io_pdc</td>
<td><em>(absolute or relative path to file)</em> # For PDC containing I/O attribute</td>
</tr>
<tr>
<td>-fp_pdc</td>
<td><em>(absolute or relative path to file)</em> # For PDC containing timing and</td>
</tr>
<tr>
<td>-edif</td>
<td>placement info</td>
</tr>
<tr>
<td>-sdc</td>
<td></td>
</tr>
<tr>
<td>-pin</td>
<td></td>
</tr>
<tr>
<td>-dcf</td>
<td></td>
</tr>
<tr>
<td>-pdc</td>
<td></td>
</tr>
<tr>
<td>-vcd</td>
<td></td>
</tr>
<tr>
<td>-saif</td>
<td></td>
</tr>
<tr>
<td>-crt</td>
<td></td>
</tr>
<tr>
<td>-simulation</td>
<td></td>
</tr>
<tr>
<td>-profiles</td>
<td></td>
</tr>
<tr>
<td>-cxf</td>
<td></td>
</tr>
<tr>
<td>-templates</td>
<td></td>
</tr>
<tr>
<td>-ccz</td>
<td></td>
</tr>
</tbody>
</table>
-wf_stimulus {file}
-modelsim_ini {file}
-library {file}
-can_convert_EDN_to_HDL {true | false

**Arguments**

- **smartgen_core {file}**
  Specifies the cores you wish to import into your project. Type parameter must be repeated for each file.

- **ccp {file}**
  Specifies the ARM or Cortex-M1 cores you wish to import into your project. Type parameter must be repeated for each file.

- **stimulus {file}**
  Specifies HDL stimulus files you wish to import into your project. Type parameter must be repeated for each file.

- **hdl_source {file}**
  Specifies the HDL source files you wish to import into your project. Type parameter must be repeated for each file.

- **io_pdc {<absolute or relative path to file>}**
  SmartFusion2 and IGLOO2 only - Specifies the PDC file that contains the I/O attribute and pin information.

- **fp_pdc {<absolute or relative path to file>}**
  SmartFusion2 and IGLOO2 only - Specifies the PDC file that contains the timing and placement information.

- **edif {file}**
  Specifies the EDIF files you wish to import into your project. Type parameter must be repeated for each file. This is a mandatory option if you want to convert EDIF to HDL with the –can_convert_EDN_to_HDL option.

- **can_convert_EDN_to_HDL {true |false |1 | 0} #Boolean {true | false | 1 | 0}**
  The –edif option is mandatory. If the –edif option is not specified or the –can_convert_EDN_to_HDL is used with another option, EDIF to HDL conversion will fail.

- **constraint_sdc {file}**
  Specifies the SDC constraint files you wish to import into your project. Type parameter must be repeated for each file.

- **constraint_pin {file}**
  Specifies the PIN constraint files you wish to import into your project. Type parameter must be repeated for each file.

- **constraint_dcf {file}**
  Specifies the DCF constraint files you wish to import into your project. Type parameter must be repeated for each file.

- **constraint_pdc {file}**
  Specifies the PDC constraint files you wish to import into your project. Type parameter must be repeated for each file.

- **constraint_gcf {file}**
  Specifies the GCF constraint files you wish to import into your project. Type parameter must be repeated for each file.

- **constraint_vcd {file}**
  Specifies the VCD constraint files you wish to import into your project. Type parameter must be repeated for each file.

- **constraint_saif {file}**
  Specifies the SAIF constraint files you wish to import into your project. Type parameter must be repeated for each file.
-constraint_crt {file}
Specifies the CRT constraint files you wish to import into your project. Type parameter must be repeated for each file.

-simulation {file}
Specifies the simulation files you wish to import into your Libero SoC project. Type parameter must be repeated for each file.

-profiles {file}
Specifies the profile files you wish to import into your Libero SoC project. Type parameter must be repeated for each file.

-cxf {file}
Specifies the CXF file (such as SmartDesign components) you wish to import into your Libero SoC project. Type parameter must be repeated for each file.

-templates {file}
Specifies the template file you wish to import into your IDE project.

-ccz {file}
Specifies the IP core file you wish to import into your project.

-wf_stimulus {file}
Specifies the WaveFormer Pro stimulus file you wish to import into your project.

-modelsim_ini {file}
Specifies the ModelSIM INI file that you wish to import into your project.

-library {file}
Specifies the library file that you wish to import into your project. If a library file is not available it will be created and added to the library.

Example
The command below imports the HDL source files file1.vhd and file2.vhd:
import_files -hdl_source file1.vhd -hdl_source file2.vhd

new_project
Tcl command; creates a new project in Libero SoC. If you do not specify a location, Libero SoC saves the new project in your current working directory.

new_project -name project_name\
-location project_location -family family_name\n-project_description brief text description of project\n-die device_die -package package_name -hdl HDL_type\n-speed speed_grade -die_voltage value\n-ondemand_build_dh {1 | 0}\n-adv_options value

Arguments
-name project_name
The name of the project. This is used as the base name for most of the files generated from Libero SoC.

-location project_location
The location of the project. Must not be an existing directory.

-project_description project_description
A brief text description of the design in your project.
-family family_name
The Microsemi SoC device family for your targeted design.

die device_die
Die for your targeted design.

package package_name
Package for your targeted design.

-hdl HDL_type
Sets the HDL type for your new project.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VHDL</td>
<td>Sets your new projects HDL type to VHDL</td>
</tr>
<tr>
<td>VERILOG</td>
<td>Sets your new projects to Verilog</td>
</tr>
</tbody>
</table>

-speed speed_grade
Sets the speed grade for your project. Possible values depend on your device, die and package. See your device datasheet for details.

die_voltage value
Sets the die voltage for your project. Possible values depend on your device. See your device datasheet for details.

-ondemand_build_dh {1 | 0}
Enter "1" to enable or "0" (default) to disable On Demand Build Design Hierarchy.

-adv_options value
Sets your advanced options, such as operating conditions.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
</table>
| IO_DEFT_STD:LVTTL            | Sets your I/O default value to LVTTL. This value defines the default I/O technology to be used for any I/Os that the user does not explicitly set a technology for in the I/O Editor. It could be any of:
  - LVTTL
  - LVCMOS 3.3V
  - LVCMOS 2.5V
  - LVCMOS 1.8V
  - LVCMOS 1.5V
  - LVCMOS 1.2V |
| RESTRICTPROBE_PINS           | This value reserves your pins for probing if you intend to debug using SmartDebug. Two values are available:
  - 1 (Probe pins are reserved)
  - 0 (No probe pins are reserved) |
| SYSTEM_CONTROLLER_SUSPEND_MODE | Enables designers to suspend operation of the System Controller. Enabling this bit instructs the System Controller to place itself in a reset state once the device is powered up. This effectively suspends all system services from being performed. For a list of system services, refer to the PolarFire FPGA Fabric User Guide for your device on the Microsemi website.
  Two values are available:
  - 1 (System Controller Suspend Mode is enabled) |
The following options are for Analysis Operating Conditions so that Timing and Power analysis can be performed at different operating conditions.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>• 0</td>
<td>(System Controller Suspend Mode is disabled)</td>
</tr>
</tbody>
</table>

**TEMPR**
Sets your default temperature range for operating condition analysis to EXT or IND.

**VCCI_1.2_VOLTR**
Sets the Default I/O Voltage Range for 1.2V to EXT or IND. These settings are propagated to Verify Timing, Verify Power and Backannotated Netlist to perform Timing/Power Analysis.

**VCCI_1.5_VOLTR**
Sets the Default I/O Voltage Range for 1.5V to EXT or IND. These settings are propagated to Verify Timing, Verify Power and Backannotated Netlist to perform Timing/Power Analysis.

**VCCI_1.8_VOLTR**
Sets the Default I/O Voltage Range for 1.8V to EXT or IND. These settings are propagated to Verify Timing, Verify Power and Backannotated Netlist to perform Timing/Power Analysis.

**VCCI_2.5_VOLTR**
Sets the Default I/O Voltage Range for 2.5V to EXT or IND. These settings are propagated to Verify Timing, Verify Power and Backannotated Netlist to perform Timing/Power Analysis.

**VCCI_3.3_VOLTR**
Sets the Default I/O Voltage Range for 3.3V to EXT or IND. These settings are propagated to Verify Timing, Verify Power and Backannotated Netlist to perform Timing/Power Analysis.

**VOLTR**
Sets the core voltage range for operating condition analysis to EXT or IND. This setting is propagated to Verify Timing, Verify Power and Backannotated Netlist to perform Timing/Power Analysis.

**PART_RANGE**
Sets your default temperature range for your project to EXT or IND.

---

**Example**

```tcl
#Create a new project and set up a new design
new_project -location {D:/2Work/my_pf_proj} -name {my_pf_proj} -project_description {} -block_mode 0 -standalone_peripheral_initialization 0 -use_enhanced_constraint_flow 1 -hdl {VERILOG} -family {PolarFire} -die {MPF300TS_ES} -package {FCG1152} -speed (-1) -die_voltage {1.0} -part_range {EXT} -adv_options {IO_DEFT_STD:LVCMOS 1.8V} -adv_options {SYSTEM_CONTROLLER_SUSPEND_MODE:1} -adv_options {TEMPR:EXT} -adv_options {VCCI_1.2_VOLTR:EXT} -adv_options {VCCI_1.5_VOLTR:EXT} -adv_options {VCCI_1.8_VOLTR:EXT} -adv_options {VCCI_2.5_VOLTR:EXT} -adv_options {VCCI_3.3_VOLTR:EXT} -adv_options {VOLTR:EXT} #Import HDL source file
import_files -convert_EDN_to_HDL 0 -hdl_source {C:/test/prep1.v} #Import HDL stimulus file
import_files -convert_EDN_to_HDL 0 -stimulus {C:/test/prepltb.v} #set the top level design name
set_root -module {prepl::work}
```
open_project

Tcl command; opens an existing Libero SoC project.

```
open_project project_name [do_backup_on_convert value] [backup_file backup_filename]
```

**Arguments**

- **project_name**: Must include the complete path to the PRJ file. If you do not provide the full path, Libero SoC infers that you want to open the project from your current working directory.
- **do_backup_on_convert value**: Sets the option to backup your files if you open a project created in a previous version of Libero SoC.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TRUE</td>
<td>Creates a backup of your original project before opening</td>
</tr>
<tr>
<td>FALSE</td>
<td>Opens your project without creating a backup</td>
</tr>
</tbody>
</table>

- **backup_file backup_filename**: Sets the name of your backup file (if you choose to do_backup_on_convert).

**Example**

Open project.prj from the c:/netlists/test directory.

```
open_project c:/netlists/test/project.prj
```

**See Also**

- close_project
- new_project
- save_project
open_smartdesign

Tcl command; opens a SmartDesign. You must either open or create a SmartDesign before using any of the SmartDesign specific commands "sd_*".

open_smartdesign \
-sd_name smartdesign_component_name

Arguments

- sd_name smartdesign_component_name
  Specifies the name of the SmartDesign component to be opened. It is mandatory.

Examples

open_smartdesign -sd_name {top}

Notes

This command is not required to build a SmartDesign component. This command maps to an interactive user action in the SmartDesign Canvas and will not be present in the exported SmartDesign component Tcl description.

See Also
Tcl Command Documentation Conventions

organize_constraints

Tcl command; organizes the constraint files in your project.

organize_constraints
[-file name]*
[-mode value]
-designer_view name
-module value
-tool value

Arguments

- file name
  Specifies the name of the file to which you want to associate your stimulus files.

  mode value
  Specifies whether you are creating a new stimulus association, adding, or removing; possible values are:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>new</td>
<td>Creates a new stimulus file association</td>
</tr>
<tr>
<td>add</td>
<td>Adds a stimulus file to an existing association</td>
</tr>
<tr>
<td>remove</td>
<td>Removes an stimulus file association</td>
</tr>
</tbody>
</table>

-designer_view name
  Sets the name of the Designer View in which you wish to add the constraint file, where name is the name of the view (such as impl1).

-module value
  Sets the module, where value is the name of the module.
-tool value

Identifies the intended use for the file, possible values are:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>synthesis</td>
<td>File to be used for synthesis</td>
</tr>
<tr>
<td>designer</td>
<td>File to be used in Designer</td>
</tr>
<tr>
<td>phsynth</td>
<td>File to be used in physical synthesis</td>
</tr>
</tbody>
</table>

**Example**

The example adds the constraint file delta.vhd in the Designer View impl2 for the Designer tool.

```
-organize_constraints -file delta.vhd -mode new -designer_view impl2 -module constraint -tool designer
```

**organize_sources**

Tcl command; organizes the source files in your project.

```
-organize_sources
  [-file name] *
  [-mode value]
  -module value
  -tool value
  [-use_default value]
```

**Arguments**

- **-file name**
  Specifies the name of the file to which you want to associate your stimulus files.

- **-mode value**
  Specifies whether you are creating a new stimulus association, adding, or removing; possible values are:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>new</td>
<td>Creates a new stimulus file association</td>
</tr>
<tr>
<td>add</td>
<td>Adds a stimulus file to an existing association</td>
</tr>
<tr>
<td>remove</td>
<td>Removes an stimulus file association</td>
</tr>
</tbody>
</table>

- **-module value**
  Sets the module, where value is the name of the module.

- **-tool value**
  Identifies the intended use for the file, possible values are:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>synthesis</td>
<td>File to be used for synthesis</td>
</tr>
<tr>
<td>simulation</td>
<td>File to be used for simulation</td>
</tr>
</tbody>
</table>
-use_default value

Uses the default values for synthesis or simulation; possible values are:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TRUE</td>
<td>Uses default values for synthesis or simulation.</td>
</tr>
<tr>
<td>FALSE</td>
<td>Uses user-defined values for synthesis or simulation.</td>
</tr>
</tbody>
</table>

**Example**

The example organizes a new stimulus file 'stim.vhd' using default settings.

```tcl
-organize_sources -file stim.vhd -mode new -module stimulus -tool synthesis -use_default TRUE
```

**See Also**

[Project Manager Tcl Command Reference]

**organize_tool_files**

This Tcl command is used to specify specific constraint files to be passed to and used by a Libero tool.

```tcl
organize_tool_files \  
-tool {tool_name} \  
-params {tool parameters} \  
-file {<absolute or relative path to constraint file>} \  
-module {$design::work} \  
-input_type {value}
```

**Arguments**

- **-tool {<tool_name>}**
  Specifies the name of the tool files you want to organize. Valid values are:
  SYNTHESEIZE | PLACEROUTE | SIM_PRESYNTH | SIM_POSTSYNTH | SIM_POSTLAYOUT | VERIFYTIMING

- **-file {<absolute or relative path to constraint file>}**
  Specifies the absolute or relative path to the constraint file; there may be multiple -file arguments (see example below).

- **-module {<design::work>}**
  Module definition, format is <$design:work>

- **-input_type {<constraint>}**
  Specifies type of input file. Possible values are: constraint | source | simulation | stimulus | unknown

**Example**

The following command organizes the test_derived.sdc and user.sdc files of SDC file type for the tool VERIFYTIMING for the sd1: work design.

```tcl
organize_tool_files \  
-tool {VERIFYTIMING} \  
-file {D:/Designs/my_proj/constraints/test_derived.sdc} \  
-file {D:/Designs/my_proj/constraints/user.sdc} \  
-module {sd1::work} \  
-input_type {constraint}
```
**project_settings**

This Tcl command modifies project flow settings for your Libero SoC project.

```tcl
project_settings
  [-hdl "VHDL | VERILOG"]
  [-verilog_mode {VERILOG_2K | SYSTEM_VERILOG}]
  [-vhdl_mode {VHDL_2008 | VHDL_93}]
  [-auto_update_modelsim_ini "TRUE | FALSE"]
  [-auto_update_viewdraw_ini "TRUE | FALSE"]
  [-block_mode "TRUE | FALSE"]
  [-auto_generate_synth_hdl "TRUE | FALSE"]
  [-auto_run_drc "TRUE | FALSE"]
  [-auto_generate_viewdraw_hdl "TRUE | FALSE"]
  [-auto_file_detection "TRUE | FALSE"]
  [-standalone_peripheral_initialization "1 | 0"]
  [-ondemand_build_dh "1 | 0"]
  [-enable_design_separation "1 | 0"]
  [-enable_set_mitigation "1 | 0"]
  [-display_fanout_limit {integer}]
```

**Arguments**

- **-hd1 **"VHDL | VERILOG"
  Sets your project HDL type.
- **-verilog_mode **{VERILOG_2K | SYSTEM_VERILOG}
  Sets the Verilog standard to Verilog-2001 or System Verilog.
- **-vhdl_mode **{VHDL_2008 | VHDL_93}
  Sets the VHDL standard to VHDL-2008 or VHDL-1993.
- **-auto_update_modelsim_ini **"TRUE | FALSE"
  Sets your auto-update modelsim.ini file option. TRUE updates the file automatically.
- **-auto_update_viewdraw_ini **"TRUE | FALSE"
  Sets your auto-update viewdraw.ini file option. TRUE updates the file automatically.
- **-block_mode **"TRUE | FALSE"
  Puts the Project Manager in Block mode, enables you to create blocks in your project.
- **-auto_generate_synth_hdl **"TRUE | FALSE"
  Auto-generates your HDL file after synthesis (when set to TRUE).
- **-auto_run_drc **"TRUE | FALSE"
  Auto-runs the design rule check immediately after synthesis (when set to TRUE).
- **-auto_generate_viewdraw_hdl **"TRUE | FALSE"
  Auto-generates your HDL netlist after a Save & Check in ViewDraw (when set to TRUE).
- **-auto_file_detection **"TRUE | FALSE"
  Automatically detects when new files have been added to the Libero SoC project folder (when set to TRUE).
- **-standalone_peripheral_initialization **"1 | 0"
  When set to 1, this option instructs System Builder not to build the initialization circuitry for your Peripherals. Set this option to 1 if you want to build your own peripheral initialization logic in SmartDesign to initialize each of the peripherals (MDDR/FDDR/SERDES) independently.
- **-ondemand_build_dh **"1 | 0"
  Enter "1" to enable or "0" (default) to disable On Demand Build Design Hierarchy.
- **-enable_design_separation **"1 | 0"
  Set it to "1" if your design is for security and safety critical applications and you want to make your design’s individual subsystems (design blocks) separate and independent (in terms of physical layout and
programming) to meet your design separation requirements. When set to “1”, Libero generates a parameter file (MSVT.param) that details design blocks present in the design and the number of signals entering and leaving a design block. Microsemi provides a separate tool, known as Microsemi Separation Verification Tool (MSVT), which checks the final design place and route result against the MSVT.param file and determines whether the design separation meets your requirements.

- **display_fanout_limit {integer}**

  Use this option to set the limit of high fanout nets to be displayed; the default value is 10. This means the top 10 nets with the highest fanout will appear in the <root>_compile_netlist.log file.

### Example

The following example sets your project to VHDL, disables the auto-update of the ModelSim INI or ViewDraw INI files, enables the auto-generation of HDL after synthesis, enables auto-detection for files, sets the display of high fanout nets to the top 12 high fanout nets, enables SET filters to mitigate radiation-induced transients, and enables design separation methodology for the design.

```tcl
project_settings -hdl "VHDL" \
-auto_update_modelsim_ini "FALSE" \
-auto_update_viewdraw_ini "FALSE"\n-block_mode "FALSE" -auto_generate_synth_hdl "TRUE"\n-auto_file_detection "TRUE"\n-display_fanout_limit {12}\n-enable_set_mitigation {1}\n-enable_design_separation {1}
```

### refresh

**Tcl command; refreshes your project, updates the view and checks for updated links and files.**

```tcl
refresh .
```

### Example

```tcl
refresh .
```

### remove_core

**Tcl command; removes a core from your project.**

```tcl
remove_core -name core_name
```

### Arguments

- **-name core_name**

  Name of the core you want to remove.

### Example

```tcl
Remove the core ip-beta2:
remove_core -name ip-beta2.cc2
```

### remove_library

**Tcl command; removes a VHDL library from your project.**

```tcl
remove_library
-.library name
```
Arguments
- library name
  Specifies the name of the library you wish to remove.

Example
Remove (delete) a library called 'my_lib'.
remove_library -library my_lib

See Also
add_library
rename_library

remove_profile
Tcl command; deletes a tool profile.

remove_profile -name profilename

Arguments
- name profilename
  Specifies the name of the profile you wish to delete.

Example
The following command deletes the profile 'custom1':
remove_profile -name custom1

rename_file
This Tcl command renames a constraint file specified by the -file parameter to a different name specified by the -target parameter.

rename_file -file {filename} -target {new_filename}

Arguments
- file {filename}
  Specifies the original name of the file.
- target {new_filename}
  Specifies the new name of the file.

Example
This command renames the file a.sdc to b.sdc.
rename_file -file c:/user/a.sdc -target c:/user/b.sdc

Return Value
This command returns 0 on success and 1 on failure.
rename_library

Tcl command; renames a VHDL library in your project.

**rename_library**
- **-library name**
  Identifies the current name of the library that you wish to rename.
- **-name name**
  Specifies the new name of the library.

**Example**

Rename a library from 'my_lib' to 'test_lib1'

```tcl
rename_library -library my_lib -name test_lib1
```

**See Also**

add_library, remove_library

run_tool

run_tool starts the specified tool. For tools that support command files, an optional command file can be supplied through the **-script** parameter.

**run_tool**
- **-name {<tool_name>}**
- **-script {<absolute or relative path to script file>}**

**-script** is an optional parameter.

**tool_name**: SYNTHESIZE, COMPILe, SIM_PRESYNTH, SIM_POSTSYNTH, PLACEROUTE, VERIFYTIMING, VERIFYPOWER, GENERATEPROGRAMMINGFILE, GENERATE_MEMORY_MAP, PROGRAMDEVICE, CONFIGURE_CHAIN, SMARTDEBUG, SSNANALYZER, GENERATE_SPI_FLASH_IMAGE, PROGRAM_SPI_FLASH_IMAGE

**Return**

run_tool returns 0 on success and 1 on failure.

**Supported tool_names**

The following table lists tool_names for run_tool –name {tool_name}.

<table>
<thead>
<tr>
<th>tool_name</th>
<th>Parameter</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SYNTHESIZE</td>
<td>-script {script_file}</td>
<td>Runs synthesis on your design.</td>
</tr>
<tr>
<td>COMPILe</td>
<td>N/A</td>
<td>Runs Compile with default or configured settings.</td>
</tr>
<tr>
<td>SIM_PRESYNTH</td>
<td>N/A</td>
<td>Runs pre-synthesis simulation with your default simulation tool.</td>
</tr>
<tr>
<td>tool_name</td>
<td>Parameter</td>
<td>Description</td>
</tr>
<tr>
<td>------------------------</td>
<td>-----------</td>
<td>------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>SIM_POSTSYNTH</td>
<td>N/A</td>
<td>Runs post-synthesis simulation with your default simulation tool.</td>
</tr>
<tr>
<td>PLACEROUTE</td>
<td>N/A</td>
<td>Runs Layout with default or configured settings.</td>
</tr>
<tr>
<td>VERIFYTIMING</td>
<td>-script {script_file}</td>
<td>Runs timing analysis with default settings/configured settings in script_file.</td>
</tr>
<tr>
<td>VERIFYPOWER</td>
<td>-script {script_file}</td>
<td>Runs power analysis with default settings/configured settings in script_file.</td>
</tr>
<tr>
<td>GENERATEPROGRAMMINGFILE</td>
<td>N/A</td>
<td>Generates the bitstream used for programming within Libero.</td>
</tr>
<tr>
<td>GENERATE_MEMORY_MAP</td>
<td>N/A</td>
<td>Exports an XML file in &lt;prj_folder&gt; component/work/&lt;design&gt; /&lt;design&gt;_DataSheet.xml. The file contains information about your root SmartDesign in your project.</td>
</tr>
<tr>
<td>PROGRAMDEVICE</td>
<td>N/A</td>
<td>Programs your device with configured parameters.</td>
</tr>
<tr>
<td>CONFIGURE_CHAIN</td>
<td>-script {script_file}</td>
<td>Takes a script that contains FlashPro-specific Tcl commands and passes them to FlashPro Express for execution.</td>
</tr>
<tr>
<td>SMARTDEBUG</td>
<td>-script {script_file}</td>
<td>Takes a script that contains SmartDebug-specific Tcl commands and passes them to SmartDebug for execution.</td>
</tr>
<tr>
<td>GENERATE_SPI_FLASH_IMAGE</td>
<td>N/A</td>
<td>Generates SPI Flash Image file used for programming SPI FLASH Image within Libero.</td>
</tr>
<tr>
<td>PROGRAM_SPI_FLASH_IMAGE</td>
<td>N/A</td>
<td>Programs SPI Flash Image with configured parameters.</td>
</tr>
</tbody>
</table>

```
-run_tool \
- name {COMPILE}
-run_tool \
- name {SYNTHESIZE} -script {./control_synopsys.tcl}
  #control_synopsys.tcl contains the synthesis-specific Tcl commands
-run_tool \
- name {VERIFYTIMING} \
- script {./SmartTime.tcl}
```

Example
# Script file contains SmartTime-specific Tcl commands
run_tool \
    -name {VERIFYPOWER} \
    -script {./SmartPower.tcl}

# Script file contains SmartPower-specific Tcl commands
run_tool \
    -name {SMARTDEBUG} \
    -script {./sd_test.tcl}

# Script file contains SmartDebug-specific Tcl commands

Note
Where possible, the value of tool_name corresponds to the name of the tool in Libero SoC.
Invoking some tools will cause Libero SoC to automatically run some upstream tools in the design flow. For example, invoking Place and Route will invoke Synthesis (if not already run) before it runs Place and Route.

save_project_as
Tcl command; the save_project_as command saves the current project in Libero SoC with a different name and in a specified directory. You must specify a location with the -location parameter.

```
save_project_as
    -name project_name
    -location project_location
    -files value
    -designer_views value
    -replace_links value
```

Arguments

- **-name project_name**
  Specifies the name of your new project.

- **-location project_location**
  Must include the complete path of the PRJ file. If you do not provide the full path, Libero SoC infers that you want to save the project to your current working directory. This is a required parameter.

- **-files value**
  Specifies the files you want to copy into your new project.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>all</td>
<td>Copies all your files into your new project</td>
</tr>
<tr>
<td>project</td>
<td>Copies only your Libero SoC project files into your new project</td>
</tr>
<tr>
<td>source</td>
<td>Copies only the source files into your new project</td>
</tr>
<tr>
<td>none</td>
<td>Copies none of the files into your new project; useful if you wish to manually copy only specific project files</td>
</tr>
</tbody>
</table>

- **-designer_views value**
  Specifies the Designer views you wish to copy into your new project.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>all</td>
<td>Copies all your Designer views into your new project</td>
</tr>
<tr>
<td>Value</td>
<td>Description</td>
</tr>
<tr>
<td>--------</td>
<td>--------------------------------------------------</td>
</tr>
<tr>
<td>current</td>
<td>Copies only your current Designer view files into your new project</td>
</tr>
<tr>
<td>none</td>
<td>Copies none of your views into your new project</td>
</tr>
</tbody>
</table>

```
-replace_links value
```

Specifies whether or not you want to update your file links in your new project.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>true</td>
<td>Replaces (updates) the file links in your project during your save</td>
</tr>
<tr>
<td>false</td>
<td>Saves your project without updating the file links</td>
</tr>
</tbody>
</table>

**Example**

Saves your current Libero SoC project as mydesign.prj in the c:/netlists/testprj/mydesign directory:
```
save_project_as -location c:/netlists/testprj/mydesign -name mydesign.prj
```

**See Also**

new_project
open_project
save_project

**save_log**

Tcl command; saves your Libero SoC log file.
```
save_log -file value
```

**Arguments**

```
-file value
```

Value is your name for the new log file.

**Example**

Save the log file file_log.
```
save_log -file file_log
```

**See Also**

close_project
new_project

**save_project**

Tcl command; the save_project command saves the current project in Libero SoC.
```
save_project
```
Arguments
None

Example
Saves the project in your current working directory:
save_project

See Also
new_project
open_project

save_smartdesign
Tcl command; saves all the changes made in a SmartDesign component.

```
save_smartdesign \
-sd_name smartdesign_component_name
```

Arguments
- `sd_name` `smartdesign_component_name`  
  Specifies the name of the SmartDesign component to be saved. It is mandatory.

Examples
```
save_smartdesign -sd_name {top}
```

See Also
Tcl Command Documentation Conventions

select_profile
Tcl command; selects a profile to use in your project.

```
select_profile -name profilename
```

Arguments
- `name` `profilename`  
  Specifies the name of the profile you wish to use.

Example
The following command selects the profile 'custom1':
s```
select_profile -name custom1
```

set_actel_lib_options
Tcl command; the set_actel_lib_options command sets your simulation library to default, or to another library (when you specify a path).

```
set_actel_lib_options -use_default_sim_path value -sim_path {path}
```
Arguments

-use_default_sim_path value

Possible values are:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TRUE</td>
<td>Uses the default simulation library.</td>
</tr>
<tr>
<td>FALSE</td>
<td>Disables the default simulation library; enables you to specify a different</td>
</tr>
<tr>
<td></td>
<td>simulation library with the -sim_path {path} option.</td>
</tr>
</tbody>
</table>

-sim_path {path}

Specifies the path to your simulation library.

Example

Uses a simulation library in the directory c:sim_lib\test.

set_actel_lib_options -use_default_sim_path FALSE -sim_path {c:sim_lib\test}

set_as_target

This Tcl command sets a SDC, PDC or FDC file as the target file to receive and store new constraints.

set_as_target -type {constraint_file_type} \  
-file {constraint_file_path}

Arguments

-type {sdc | pdc | fdc}

Specifies the file type: SDC, PDC, or FDC.

Example

This command sets the SDC file <project_folder> /constraints/user.sdc as the target to receive and store new SDC commands.

set_as_target -type {sdc} -file {./constraint/user.sdc}

This command sets the PDC file <project_folder> /constraints/user.pdc as the target to receive and store new PDC commands.

set_as_target -type {pdc} -file {./constraint/user.pdc}

Return Value

This command returns 0 on success and 1 on failure.

set_device (Project Manager)

Tcl command; sets your device family, die, and package in the Project Manager.

set_device [-family family] [-die die] [-package package] [-speed speed_grade] [-adv_options value]

Arguments

-family family

Sets device family.

-die die
Sets device die.
- `package package`

Sets device package.
- `speed speed_grade`

Sets device speed grade.
- `adv_options value`

Sets your advanced options, such as temperature and voltage settings.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IO_Deft_STD:LVTTL</td>
<td>Sets your I/O default value to LVTTL</td>
</tr>
<tr>
<td>TEMPR:COM</td>
<td>Sets your default temperature range; can be COM (Commercial), MIL (Military) or IND (industrial).</td>
</tr>
<tr>
<td>VCCI_1.5_VOLTR:COM</td>
<td>Sets VCCI to 1.5 and voltage range to Commercial</td>
</tr>
<tr>
<td>VCCI_1.8_VOLTR:COM</td>
<td>Sets VCCI to 1.8 and voltage range to Commercial</td>
</tr>
<tr>
<td>VCCI_2.5_VOLTR:COM</td>
<td>Sets VCCI to 2.5 and voltage range to Commercial</td>
</tr>
<tr>
<td>VCCI_3.3_VOLTR:COM</td>
<td>Sets VCCI to 3.3 and voltage range to Commercial</td>
</tr>
<tr>
<td>VOLTR:COM</td>
<td>Sets your voltage range; can be COM (Commercial), MIL (Military) or IND (industrial).</td>
</tr>
<tr>
<td>RESTRICTPROBEPINS:1</td>
<td>(For SmartFusion2, IGLOO2 and RTG4 only) Sets to 1 to reserve your pins for probing if you intend to debug using SmartDebug.</td>
</tr>
</tbody>
</table>

See Also

*How to Derive Required Part Information from A "Part Number"*

**set_modelsim_options**

Tcl command; sets your ModelSim simulation options.

```tcl
set_modelsim_options
([-use_automatic_do_file value]
[-user_do_file {path}]
[-sim_runtime {value}]
[-tb_module_name {value}]
[-tb_top_level_name {value}]
[-include_do_file value]
[-included_do_file {value}]
[-type {value}]
[-resolution {value}]
[-add_vsim_options {value}]
[-display_dut_wave value]
[-log_all_signals value]
[-do_file_args value]
[-dump_vcd "TRUE | FALSE"]
[-vcd_file "VCD file name"]
```
Arguments

- `use_automatic_do_file value`
  Uses an automatic.do file in your project. Possible values are:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TRUE</td>
<td>Uses the default automatic.do file in your project.</td>
</tr>
<tr>
<td>FALSE</td>
<td>Uses a different *.do file; use the other simulation options to specify it.</td>
</tr>
</tbody>
</table>

- `user_do_file {path}`
  Specifies the location of your user-defined *.do file.

- `sim_runtime {value}`
  Sets your simulation runtime. Value is the number and unit of time, such as {1000ns}.

- `tb_module_name {value}`
  Specifies your testbench module name, where value is the name.

- `tb_top_level_name {value}`
  Sets the top-level instance name in the testbench, where value is the name.

- `include_do_file value`
  Includes a *.do file; possible values are:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TRUE</td>
<td>Includes the *.do file.</td>
</tr>
<tr>
<td>FALSE</td>
<td>Does not include the *.do file</td>
</tr>
</tbody>
</table>

- `included_do_file {value}`
  Specifies the path of the included *.do file, where value is the name of the file.

- `type {value}`
  Resolution type; possible values are:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>min</td>
<td>Minimum</td>
</tr>
<tr>
<td>typ</td>
<td>Typical</td>
</tr>
<tr>
<td>max</td>
<td>Maximum</td>
</tr>
</tbody>
</table>

- `resolution {value}`
  Sets your resolution value, such as {1ps}.

- `add_vsim_options {value}`
  Adds more Vsim options, where value specifies the option(s).

- `display_dut_wave value`
  Enables ModelSim to display signals for the tested design; possible values are:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Displays the signal for the top_level_testbench</td>
</tr>
<tr>
<td>1</td>
<td>Enables ModelSim to display the signals for the tested design</td>
</tr>
</tbody>
</table>
-log_all_signals value
Enables you to log all your signals during simulation; possible values are:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TRUE</td>
<td>Logs all signals</td>
</tr>
<tr>
<td>FALSE</td>
<td>Does not log all signals</td>
</tr>
</tbody>
</table>

-do_file_args value
Specifies *.do file command parameters.

dump_vcd value
Dumps the VCD file when simulation is complete; possible values are:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TRUE</td>
<td>Dumps the VCD file</td>
</tr>
<tr>
<td>FALSE</td>
<td>Does not dump the VCD file</td>
</tr>
</tbody>
</table>

-vcd_file {value}
Specifies the name of the dumped VCD file, where value is the name of the file.

Example
Sets ModelSim options to use the automatic *.do file, sets simulation runtime to 1000ns, sets the testbench module name to "testbench", sets the testbench top level to <top>_0, sets simulation type to "max", resolution to 1ps, adds no vsim options, does not log signals, adds no additional DO file arguments, dumps the VCD file with a name power.vcd.

```
set_modelsim_options -use_automatic_do_file 1 -sim_runtime {1000ns} -tb_module_name {testbench} -tb_top_level_name {<top>_0} -include_do_file 0 -type {max} -resolution {1ps} -add_vsim_options {} -display_dut_wave 0 -log_all_signals 0 -do_file_args {} -dump_vcd 0 -vcd_file {power.vcd}
```

set_option
Tcl command; sets your synthesis and FPGA Hardware Breakpoint Auto Instantiation options on a module.

```
set_option [-synth "TRUE | FALSE"] [-fhb "TRUE | FALSE"] [-module "module_name"]
```

Arguments

- synth "TRUE | FALSE"
Runs synthesis (for a value of TRUE).

- fhb "TRUE | FALSE"
Enable/disable FPGA Hardware Breakpoint Auto Instantiation.

- module module_name
Identifies the module on which you will run synthesis.

Example
Run synthesis on the module test1.vhd:

```
set_option [-synth TRUE] [-module <module_name>]
```
**set_root**

Tcl command; sets the module you specify as the root.

```
set_root module_name
```

**Arguments**

- `set_root module_name`
  
  Specifies the name the module you want to set as root.

**Example**

Set the module `mux8` as root:

```
set_root mux8
```

**set_user_lib_options**

Tcl command; sets your user library options during simulation. If you do not use a custom library these options are not available.

```
set_user_lib_options
-name {value}
-path {path}
-option {value}
```

**Arguments**

- `-name {value}`
  
  Sets the name of your user library.
- `-path {path}`
  
  Sets the pathname of your user library.
- `-option {value}`
  
  Sets your default compile options on your user library; possible values are:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>do_not_compile</td>
<td>User library is not compiled</td>
</tr>
<tr>
<td>refresh</td>
<td>User library is refreshed</td>
</tr>
<tr>
<td>compile</td>
<td>User library is compiled</td>
</tr>
<tr>
<td>recompile</td>
<td>User library is recompiled</td>
</tr>
<tr>
<td>refresh_and_compile</td>
<td>User library is refreshed and compiled</td>
</tr>
</tbody>
</table>

**Example**

The example below sets the name for the user library to "test1", the path to `c:/msemi_des_files/libraries/test1`, and the compile option to "do not compile".

```
set_user_lib_options -name {test1} -path {c:/msemi_des_files/libraries/test1} -option {do_not_compile}
```
### unlink

Tcl command; removes a link to a file in your project.

**Syntax**

```
unlink -file filename [-local local_filename]
```

#### Arguments

- **-file filename**
  
  Name of the linked (remote) file you want to unlink.

- **-local local_filename**
  
  Name of the local file that you want to unlink.

#### Example

Unlink the file hdl1.vhd from my local file test.vhd

```
unlink -file hdl1.vhd [-local test.vhd]
```

### unset_as_target

This Tcl command unsets a target file in the Constraints view.

**Syntax**

```
unset_as_target -file {filename}
```

#### Arguments

- **-file {filename}**
  
  Specifies the name of the file to be unset as a target.

#### Example

This command unsets the PDC file `<project_folder>/constraints/user.pdc`:

```
unset_as_target -file {c:/user/a_io.pdc}
```

### Return Value

This command returns 0 on success and 1 on failure.

### use_source_file

Tcl command; defines a module for your project.

**Syntax**

```
use_source_file
-file value
-module value
```

#### Arguments

- **-file value**
  
  Specifies the Verilog or VHDL file. Value is the name of the file you wish use (including the full pathname).

- **-module value**
  
  Specifies the module in which you want to use the file.

#### Example

Specify file1.vhd in the `.project/hdl` directory, in the module named top.

```
use_source_file -file `./project/hdl/file1.vhd` -module `top`
```
See Also

use_file
SmartDesign Tcl Commands

The SmartDesign Tcl commands can be used to create a design in the SmartDesign. You must either create or open a SmartDesign before you can use any of the SmartDesign commands - sd_*.

All SmartDesign Tcl commands are supported by the PolarFire family.

sd_add_pins_to_group
Tcl command; adds one or more pins to a pin group on an instance in a SmartDesign component.

```
sd_add_pins_to_group -sd_name smartdesign_component_name -instance_name instance_name -group_name group_name -pin_names pin_names
```

Arguments

- **-sd_name smartdesign_component_name**
  Specifies the name of the SmartDesign component. It is mandatory.
- **-instance_name instance_name**
  Specifies the name of the instance on which the pin group is present. It is mandatory.
- **-group_name group_name**
  Specifies the name of the group to add the pins to. It is mandatory.
- **-pin_names pin_names**
  Specifies the list of instance pins to be added to the pin group. It is mandatory.

Examples

```
sd_add_pins_to_group -sd_name {TOP} -instance_name {COREAXI4INTERCONNECT_C0_0} -group_name {Group} -pin_names {ARESETN ACLK}
```

See Also

Tcl Command Documentation Conventions

sd_clear_pin_attributes
Tcl command; clears all attributes on one or more pins/ports in a SmartDesign. Pin attributes include pin inversion, mark as unused and constant value settings.

```
sd_clear_pin_attributes -sd_name smartdesign_component_name -pin_names port_or_pin_names
```

Arguments

- **-sd_name smartdesign_component_name**
  Specifies the name of the SmartDesign component. It is mandatory.
- **-pin_names port_or_pin_names**
  Specifies the name of the port/pin for which all the attributes must be cleared. It is mandatory.
Examples

```
sd_clear_pin_attributes -sd_name {sd1} -pin_names {RAM1K18_0:A_DOUT_CLK}
sd_clear_pin_attributes -sd_name {top} -pin_names {CARRY_OUT}
```

Notes

This command will not work on multiple pins/ports in this release. Support for multiple pins/ports will be provided in the next Libero release. This command is not required to build a SmartDesign component. This command maps to an interactive user action in the SmartDesign Canvas and will not be present in the exported SmartDesign component Tcl description.

See Also

Tcl Command Documentation Conventions

**sd_configure_core_instance**

Tcl command; configures the parameters of a core instance (Direct Instantiation) in a SmartDesign component. This command is typically used after instantiating a core from the catalog directly into a SmartDesign component (Direct Instantiation) without first creating a component for the core (using sd_instantiate_core). This command can configure multiple core parameters at a time.

```
sd_configure_core_instance
  -sd_name smartdesign_component_name
  -instance_name core_instance_name
  -params core_parameters
  [-validate_rules 0|1]
```

Arguments

- **-sd_name smartdesign_component_name**
  Specifies the name of the SmartDesign component. It is mandatory.

- **-instance_name instance_name**
  Specifies the name of the core instance in the SmartDesign which needs to be configured. It is mandatory.

- **-params core_parameters**
  Specifies the parameters that need to be configured for the core instance. It is mandatory.

- **-validate_rules 0|1**
  Validates the rules of the updated configuration. It is optional.

Examples

```
sd_configure_core_instance -sd_name {SD1} -instance_name {COREFIFO_0} -params {"SYNC:0" "param2:value2" "param3:value3"} -validate_rules 0
```

See Also

Tcl Command Documentation Conventions

**sd_connect_instance_pins_to_ports**

Tcl command; connects all pins of an instance to new SmartDesign top level ports.

```
sd_connect_instance_pins_to_ports
  -sd_name smartdesign_component_name
  -instance_name instance_name
```

68
Arguments

- `sd_name smartdesign_component_name`
  Specifies the name of the SmartDesign component. It is mandatory.
- `instance_name instance_name`
  Specifies the instance name for which all the pins must be connected to top level ports. It is mandatory. The instance pins are connected to new top level ports created with the same instance pin names. If a top level port with the same name already exists, then the tool automatically creates a new port with name `<port_name>_<index>` (index is an automatically generated integer starting at 0 such that the port name is unique in the SmartDesign).

Examples

```
sd_connect_instance_pins_to_ports -sd_name {top} -instance_name {CORESPI_C0_0}
```
```
sd_connect_instance_pins_to_ports -sd_name {top} -instance_name {ddr_out_0}
```

Notes

This command is not required to build a SmartDesign component. This command maps to an interactive user action in the SmartDesign Canvas and will not be present in the exported SmartDesign component Tcl description.

See Also

[Tcl Command Documentation Conventions](#)

sd_connect_pins_to_constant

Tcl command; connects SmartDesign top level output ports or input instance pins to constant values.

```
sd_connect_pins_to_constant \
-sd_name smartdesign_component_name \
-pin_names port_or_pin_names \
-value constant_value
```

Arguments

- `sd_name smartdesign_component_name`
  Specifies the name of the SmartDesign component. It is mandatory.
- `pin_names port_or_pin_names`
  Specifies the names of the top level output ports or the instance level input pins to be tied to constant values. It is mandatory. Bus pins/ports and pin/port slices can also be tied to constant values. This command will fail if the specified port/pin does not exist. The command will also fail if the assigned object is a port of direction IN/INOUT or a pin of direction OUT/INOUT.
- `value constant_value`
  Specifies the constant value to be assigned to the port/pin. It is mandatory. The acceptable values to this argument are GND/VCC/hexadecimal numbers.

Examples

```
sd_connect_pins_to_constant -sd_name {top} -pin_name {bypass} -value {GND}
sd_connect_pins_to_constant -sd_name {top} -pin_name {sle_0:en} -value {VCC}
sd_connect_pins_to_constant -sd_name {top} -pin_name {ram64x12_0:w_data} -value {0x7f}
```
Notes

This command will not work on multiple pins/ports in this release. Support for multiple pins/ports will be provided in the next Libero release.

See Also

Tcl Command Documentation Conventions

sd_connect_pin_to_port

Tcl command; connects a SmartDesign instance pin to a new top level port. This command is equivalent to the ‘Promote to Top Level’ GUI action on an instance pin.

```tcl
sd_connect_pin_to_port
- sd_name smartdesign_component_name
- pin_name pin_name
[- port_name port_name]
```

Arguments

- **-sd_name smartdesign_component_name**
  Specifies the name of the SmartDesign component. It is mandatory.

- **-pin_name pin_name**
  Specifies the name of the instance level pin that needs to be connected to a top level port. It is mandatory.

- **-port_name port_name**
  Specifies the name of the new top level port that the instance pin will be connected to. It is optional. If the port name is not specified, the new port takes the name of the instance pin. If the port name as defined by these rules already exists, the tool automatically creates a new port with name <port_name>_<<index>> (index is an automatically generated integer starting at 0 such that the port name is unique in the SmartDesign).

Examples

```
sd_connect_pin_to_port -sd_name {top} -pin_name {DFN1_0:D}
da_connect_pin_to_port -sd_name {top} -pin_name {DFN1_0:Q} -port_name {Q_OUT}
```

Notes

This command is not required to build a SmartDesign component. This command maps to an interactive user action in the SmartDesign Canvas and will not be present in the exported SmartDesign component Tcl description.

See Also

Tcl Command Documentation Conventions

sd_connect_pins

Tcl command; connects a list of SmartDesign top level ports and/or instance pins together.

```tcl
sd_connect_pins
- sd_name smartdesign_component_name
- pin_names port_or_pin_or_slice_names
```

Arguments

- **-sd_name smartdesign_component_name**
Specifies the name of the SmartDesign component. It is mandatory.

```
-pi_names port_or_pin_or_slice_names
```

Specifies the port names, pin names and/or slice names to be connected together. It is mandatory. This command will fail if the ports, pins or slices do not exist. This command will also fail if the ports, pins and/or slices are not of the same size/range.

**Examples**

```
sd_connect_pins -sd_name {top} -pi_names {CLK MACC_PA_0:CLK DFN1_0:CLK}
```

```
sd_connect_pins -sd_name {top} -pi_names {MACC_PA_0:A RAM1K20_0:A_DIN[17:0]}
```

**See Also**

[Tcl Command Documentation Conventions](#)

## sd_create_bif_port

Tcl command; creates a SmartDesign Bus Interface port of a given type. This command is used to create top level Bus Interface ports in a SmartDesign component to connect to the instance level Bus Interface ports of the same type.

To use this command, it is recommended to first use the GUI to instantiate the core component or the HDL module with Bus Interface port to be promoted in the SmartDesign. Then use the UI action "Promote to Top Level" on the Bus Interface port of interest and export the Tcl script for the SmartDesign component by selecting "Export Component Description(Tcl)" on the right-click menu of the SmartDesign component in the Design Hierarchy. You can then use the Tcl command `sd_create_bif_port` from the exported Tcl script (note to change the SmartDesign name in the command) to create a bus interface port anywhere in a regular Libero script. Note that there can be different Bus Interface types and roles defined by the arguments –port_bif_vlnv and –port_bif_role.

```
sd_create_bif_port \
-sd_name smartdesign_component_name \\
-port_name port_name \\
-port_bif_vlnv vendor:library:name:version \\
-port_bif_role port_bif_role \\
-port_bif_mapping [bif_port_name:port_name]+
```

### Arguments

- **-sd_name smartdesign_component_name**
  
  Specifies the name of the SmartDesign component. It is mandatory.

- **-port_name port_name**
  
  Specifies the name of the Bus Interface port to be added in the SmartDesign. It is mandatory.

  `port_bif_vlnv {vendor:library:name:version}`

- **-port_bif_role port_bif_role**
  
  Specifies the version identifier of the Bus Interface port to be added in the SmartDesign. It is mandatory.

- **-port_bif_role port_bif_role**
  
  Specifies the role of the Bus Interface port to be added in the SmartDesign. Role values depend on the type of Bus Interface (VLNV) that is being defined for the port. The figure below shows the roles for different Bus Interface ports supported by Libero.
-port_bif_mapping {[bif_port_name:port_name ]+}

Specifies the mapping between the bus interface formal names and the SmartDesign ports mapped onto that bus interface port. It is mandatory.

### Examples

```
sd_create_bif_port -sd_name {sd1} -port_name {BIF_1} -port_bif_vlnv {AMBA:AMBA2:APB:r0p0} -port_bif_role {slave} -port_bif_mapping {
"PADDR:PADDR" \ 
"PSELx:pselx" \ 
"PENABLE:PENABLE" \ 
"PWRITE:PWRITE" \ 
"PRDATA:PRDATA" \ 
"PWDATA:PWDATA" \ 
"PREADY:PREADY" \ 
"PSLVERR:PSLVERR" }
```

### See Also

[Tcl Command Documentation Conventions](#)
sd_create_bus_port

Tcl command; creates a bus port of a given range in a SmartDesign component.

```tcl
sd_create_bus_port \
-sd_name  smartdesign_component_name \
-port_name port_name \-port_direction IN|OUT|INOUT \
-port_range {[left_range_index:right_range_index]}
```

**Arguments**

- `sd_name smartdesign_component_name`
  Specifies the name of the SmartDesign component. It is mandatory.
- `port_name`
  Specifies the name of the bus port added to be SmartDesign component. It is mandatory.
- `port_direction IN|OUT|INOUT`
  Specifies the direction of the bus port added to the SmartDesign component. It is mandatory.
- `port_range {[left_range_index:right_range_index]}`
  Specifies the range of the bus port added to the SmartDesign component. The range is defined by the left and right indices. It is mandatory. The range must be specified inside the square brackets.

**Examples**

```tcl
sd_create_bus_port -sd_name {top} -port_name {test_port13} -port_direction {OUT} -port_range {[9:36]}
sd_create_bus_port -sd_name {top} -port_name {test_port4} -port_direction {IN} -port_range {[31:0]}
```

**See Also**

[Tcl Command Documentation Conventions](#)

sd_create_pin_group

Tcl command; creates a group of pins in a SmartDesign component. A pin group is only used to manage the complexity of the SmartDesign canvas. There is no actual netlist functionality related to pin group commands. Pin groups cannot be created for top level ports.

```tcl
sd_create_pin_group \
-sd_name  smartdesign_component_name \
-instance_name instance_name \ 
[-group_name group_name] \ 
[-pin_names pin_to_be_added_to_the_group]
```

**Arguments**

- `sd_name smartdesign_component_name`
  Specifies the name of the SmartDesign component. It is mandatory.
- `instance_name`
  Specifies the name of the instance on which the pin group is added. It is mandatory.
- `group_name`
  Specifies the name of the pin group. It is optional. If the group name is not specified, the default name will be ‘Group’. If the name ‘Group’ is already taken, then the group name will be ‘Group_<index>’ (index is auto-incremented).
- `pin_names pins_to_be_added_to_the_group`
  Specifies the list of instance pins to be added to the pin group. It is optional.
Examples

sd_create_pin_group -sd_name {TOP} -instance_name {COREAXI4INTERCONNECT_C0_0} -group_name {MyGroup} -pin_names {AClk ARESETN}

See Also
Tcl Command Documentation Conventions

**sd_create_pin_slices**

Tcl command; creates slices for a SmartDesign top level bus port or an instance level bus pin.

<table>
<thead>
<tr>
<th>Argument</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>sd_name</td>
<td>smartdesign_component_name</td>
</tr>
<tr>
<td>pin_name</td>
<td>port_or_pin_name</td>
</tr>
<tr>
<td>pin_slices</td>
<td>port_or_pin_slices</td>
</tr>
</tbody>
</table>

**Arguments**

- **sd_name smartdesign_component_name**
  Specifies the name of the SmartDesign component. It is mandatory.

- **pin_name port_or_pin_name**
  Specifies the name of the bus port or bus pin to be sliced. It is mandatory. This command will fail if the port/pin is scalar or if the bus port/pin does not exist.

- **pin_slices port_or_pin_slices**
  Specifies the port/pin slices as a list of bus ranges which must be contained within the port/pin bus range. It is mandatory. This command will fail if the sliced object is top level OUT/INOUT port and the slice ranges overlap. This command will also fail if the sliced object is an instance level IN/INOUT pin and the slice ranges overlap.

**Examples**

sd_create_pin_slices -sd_name {sub} -pin_name {Rdata} -pin_slices {[4:3] [2:0]} # top level port slicing
sd_create_pin_slices -sd_name {sub} -pin_name {DDR_memory_arbiter_C0_0:VIDEO_RDATA_4_O} -pin_slices {[3:3] [2:0]} # instance level pin slicing

See Also
Tcl Command Documentation Conventions

**sd_create_scalar_port**

Tcl command; creates a scalar port in a SmartDesign component.

<table>
<thead>
<tr>
<th>Argument</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>sd_name</td>
<td>smartdesign_component_name</td>
</tr>
<tr>
<td>port_name</td>
<td>port_name</td>
</tr>
<tr>
<td>port_direction</td>
<td>IN</td>
</tr>
</tbody>
</table>

**Arguments**

- **sd_name smartdesign_component_name**
  Specifies the name of the SmartDesign component. It is mandatory.

- **port_name port_name**
  Specifies the name of the port added to the SmartDesign component. It is mandatory.

- **port_direction IN|OUT|INOUT**
Specifies the direction of the port added to the SmartDesign component. It is mandatory.

**Examples**

```tcl
sd_create_scalar_port -sd_name {main} -port_name {po2} -port_direction {INOUT}
```

**See Also**

[ Tcl Command Documentation Conventions ](#)

### sd_delete_instances

Tcl command; deletes one or more instances from a SmartDesign component.

```tcl
sd_delete_instances \
  -sd_name smartdesign_component_name \
  -instance_names instance_names
```

**Arguments**

- `-sd_name smartdesign_component_name`
  
  Specifies the name of the SmartDesign component. It is mandatory.

- `-instance_names instance_names`
  
  Specifies the instance names to be deleted. It is mandatory.

**Examples**

```tcl
sd_delete_instances -sd_name {top} -instance_names {RAM64X12_0}  
sd_delete_instances -sd_name {SUB} -instance_names {coreahblite_c0_0  
coreriscv_axi4_c0_0 pf_ccc_c0_0}
```

**Notes**

This command is not required to build a SmartDesign component. This command maps to an interactive user action in the SmartDesign Canvas and will not be present in the exported SmartDesign component Tcl description.

**See Also**

[ Tcl Command Documentation Conventions ](#)

### sd_delete_nets

Tcl command; deletes one or more nets from the SmartDesign component.

```tcl
sd_delete_nets \
  -sd_name smartdesign_component_name \
  -net_names net_names
```

**Arguments**

- `-sd_name smartdesign_component_name`
  
  Specifies the name of the SmartDesign component. It is mandatory.

- `-net_names net_names`
  
  Specifies the net names to be deleted. It is mandatory.

**Examples**

```tcl
sd_delete_nets -sd_name {topp} -net_names {B_REN_0}
```
Notes
This command will not delete multiple nets in this release. Support for deleting multiple nets will be provided in the next Libero release. This command is not required to build a SmartDesign component. This command maps to an interactive user action in the SmartDesign Canvas and will not be present in the exported SmartDesign component Tcl description.

See Also
Tcl Command Documentation Conventions

sd_delete_pin_group
Tcl command; deletes a pin group from an instance in a SmartDesign component.

sd_delete_pin_group
-\-
-\-sd_name smartdesign_component_name
-instance_name instance_name
-group_name group_name

Arguments
-\-sd_name smartdesign_component_name
Specifies the name of the SmartDesign component. It is mandatory.
-\-group_name group_name
Specifies the name of the pin group to be deleted. It is mandatory.
-\-instance_name instance_name
Specifies the name of the instance from which the group pin needs to be deleted. It is mandatory.

Examples
sd_delete_pin_group -sd_name {TOP} -instance_name {COREAXI4INTERCONNECT_C0_0} -group_name {Group}

See Also
Tcl Command Documentation Conventions

sd_delete_pin_slices
Tcl command; deletes SmartDesign top level port slices or instance pin slices.

sd_create_pin_slices
-\-
-\-sd_name smartdesign_component_name
-pin_name port_or_pin_name
-pin_slices port_or_pin_slices

Arguments
-\-sd_name smartdesign_component_name
Specifies the name of the SmartDesign component. It is mandatory.
-\-pin_name port_or_pin_name
Specifies the name of the bus port or bus pin for which the slices must be deleted. It is mandatory.
-\-pin_slices port_or_pin_slices
Specifies the ranges of the port and/or pin slices to be deleted. It is mandatory.
Examples

sd_delete_pin_slices -sd_name {top} -pin_name {MACC_pa_0:p} -pin_slices {[21] [13] [28]} # deletes instance pin slices
sd_delete_pin_slices -sd_name {top} -pin_name {A} -pin_slices {[17:16] [15:1] [0]} # deletes top level port slices

Notes
This command is not required to build a SmartDesign component. This command maps to an interactive user action in the SmartDesign Canvas and will not be present in the exported SmartDesign component Tcl description.

See Also
Tcl Command Documentation Conventions

sd_delete_ports
Tcl command; deletes one or more ports from the SmartDesign component.

Arguments
- sd_name smartdesign_component_name
  Specifies the name of the SmartDesign component. It is mandatory.
- port_names port_names
  Specifies the names of the ports to be deleted. It is mandatory.

Examples
sd_delete_ports -sd_name {sd1} -port_names {REF_CLK_0}

Notes
This command will not work on multiple ports in this release. Support for multiple ports will be provided in the next Libero release. This command is not required to build a SmartDesign component. This command maps to an interactive user action in the SmartDesign Canvas and will not be present in the exported SmartDesign component Tcl description.

See Also
Tcl Command Documentation Conventions

sd_disconnect_instance
Tcl command; clears all the connections on an instance in a SmartDesign component.

Arguments
- sd_name smartdesign_component_name
  Specifies the name of the SmartDesign component. It is mandatory.
-instance_name instance_name

Specifies the name of the instance for which all the connections must be cleared. It is mandatory.

Examples

sd_disconnect_instance -sd_name {sd1} -instance_name {RAM1K18_1}

Notes

This command is not required to build a SmartDesign component. This command maps to an interactive user action in the SmartDesign Canvas and will not be present in the exported SmartDesign component Tcl description.

See Also

Tcl Command Documentation Conventions

ds_disconnect_pins

Tcl command; disconnects a list of SmartDesign top level ports and/or instance pins from the net they are connected to.

Arguments

- sd_name smartdesign_component_name
  Specifies the name of the SmartDesign component. It is mandatory.

- pin_names port_or_pin_or_slice_names
  Specifies the port, pin and/or slice names to be disconnected. It is mandatory. This command will fail if the ports, pins and/or slices do not exist.

Examples

sd_disconnect_pins -sd_name {topp} -pin_names {B_ren
  RAM1K20_0:B_ADRR[12]}
  sd_disconnect_pins -sd_name {SD1} -pin_names {AND2_0:B AND3_0:B AND3_0:A
  PF_XCVR_ERM_C0_0:LANE0_RX_READY}

Notes

This command is not required to build a SmartDesign component. This command maps to an interactive user action in the SmartDesign Canvas and will not be present in the exported SmartDesign component Tcl description.

See Also

Tcl Command Documentation Conventions

sd_duplicate_instance

Tcl command; creates a new instance in a SmartDesign with the same module/component as the original instance.

Arguments

- sd_name smartdesign_component_name
  Specifies the name of the SmartDesign component. It is mandatory.

- instance_name instance_name
  Specifies the name of the instance for which a new instance will be created. It is mandatory.

Examples

sd_duplicate_instance -sd_name {sd1} -instance_name {RAM1K18_1}

Notes

This command is not required to build a SmartDesign component. This command maps to an interactive user action in the SmartDesign Canvas and will not be present in the exported SmartDesign component Tcl description.
### sd_duplicate_instance

**Tcl command:**

```
arg1 arg2 arg3
```

**Arguments**

- `sd_name` `smartdesign_component_name`
  Specifies the name of the SmartDesign component. It is mandatory.
- `instance_name` `instance_name`
  Specifies the name of the instance to be duplicated. It is mandatory.
- `duplicate_instance_name` `duplicate_instance_name`
  Specifies the name of the duplicate instance. It is optional. If the `duplicate_instance_name` is not specified, it will be automatically generated as `<instance_name>-<index>` (index is an automatically generated integer starting at 0 such that the instance name is unique in the SmartDesign).

**Examples**

```
sd_duplicate_instance -sd_name {top} -instance_name {PF CCC C0 0}
sd_duplicate_instance -sd_name {top} -instance_name {SUB 0} -
  duplicate_instance_name {T1}
```

**Notes**

This command is not required to build a SmartDesign component. This command maps to an interactive user action in the SmartDesign Canvas and will not be present in the exported SmartDesign component Tcl description.

**See Also**

[Tcl Command Documentation Conventions](#)

### sd_hide_bif_pins

**Tcl command:**

```
arg1 arg2 arg3
```

**Arguments**

- `sd_name` `smartdesign_component_name`
  Specifies the name of the SmartDesign component. It is mandatory.
- `bif_pin_name` `name_of_the_bif_pin_or_port`
  Specifies the name of the Bus Interface pin for which the internal pins must be hidden. It is mandatory.
- `pin_names` `pins_or_ports_to_be_exposed`
  Specifies the bus interface internal pin/port names to be hidden. It is mandatory.

**Examples**

```
sd_hide_bif_pins -sd_name {sd1} -bif_pin_name {COREAXI4INTERCONNECT_C0_0:AXI4mmaster0} -
  pin_names {COREAXI4INTERCONNECT_C0_0:MASTER0_AWADDR}
sd_hide_bif_pins -sd_name {SD1} -bif_pin_name {CLKS_FROM_TXPLL_0} -pin_names {TX_PLL_LOCK_0}
```

**Notes**

This command will not hide multiple pins/ports in this release. Support to hide multiple pins/ports will be provided in the next Libero release. This command is not required to build a SmartDesign component. This command maps to an interactive user action in the SmartDesign Canvas and will not be present in the exported SmartDesign component Tcl description.
sdInstantiateComponent

Tcl command; instantiates a Libero SmartDesign component or a core component into another SmartDesign component.

sdInstantiateComponent
-sd_name smartdesign_component_name
-component_name component_module_name
[-instance_name instance_name]

Arguments

-sd_name smartdesign_component_name
Specifies the name of the SmartDesign component in which other components will be instantiated. It is mandatory.

-component_name component_module_name
Specifies the name of the component being instantiated in the SmartDesign component. It is mandatory.

Examples

sdInstantiateComponent -sd_name {sub} -component_name {sd1} -instance_name {sd1_0}
sdInstantiateComponent -sd_name {top} -component_name {PF_CCC_C0}

See Also

Tcl Command Documentation Conventions

sdInstantiateCore

Tcl command; instantiates a core from the catalog directly into a SmartDesign component (Direct Instantiation) without first having to create a component for the core. The file-set related to the core is generated only when the SmartDesign in which the core is instantiated is generated. The GUI equivalent of this command is not currently supported in Libero. To instantiate a core in a SmartDesign component in the GUI, you have to first create a component for the core.

sdInstantiateCore
-sd_name smartdesign_component_name \-core_vlnv vendor:library:name:version \[-instance_name instance_name]

Arguments

-sd_name smartdesign_component_name
Specifies the name of the SmartDesign component. It is mandatory.

-core_vlnv vendor:library:name:version
Specifies the version identifier of the core being instantiated in the SmartDesign component. It is mandatory.
-instance_name instance_name

Specifies the instance name of the core being instantiated in the SmartDesign. It is optional. By default, the instance name is <core_name>_index> (index is an automatically generated integer starting at 0 such that the instance name is unique in the SmartDesign).

Examples

sd_instantiate_core -sd_name {top} -core_vlnv {Actel:DirectCore:COREAXI4INTERCONNECT:2.5.100} -instance_name {COREAXI4INTERCONNECT_C0_0}

See Also
Tcl Command Documentation Conventions

sd_instantiate_hdl_core

Tcl command; instantiates a HDL+ core in a SmartDesign component. HDL+ core definition must be created on a HDL module before using this command.

sd_instantiate_hdl_core
-sd_name smartdesign_component_name
-hdl_core_name hdl_core_module_name
[-instance_name instance_name]

Arguments

-sd_name smartdesign_component_name
Specifies the name of the SmartDesign component. It is mandatory.
-hdl_core_name hdl_core_module_name
Specifies the name of the HDL+ core module being instantiated in the SmartDesign component. It is mandatory.
-instance_name instance_name
Specifies the instance name of the HDL+ core being instantiated in the SmartDesign. It is optional. By default, the instance name is <hdl_core_module_name>_index> (index is an automatically generated integer starting at 0 such that the instance name is unique in the SmartDesign).

Examples

sd_instantiate_hdl_core -sd_name {top} -hdl_core_name {temp} -instance_name {temp3}

See Also
Tcl Command Documentation Conventions

sd_instantiate_hdl_module

Tcl command; instantiates a HDL module in a SmartDesign component. The HDL file in which the HDL module is defined must be imported/linked before running this command.

sd_instantiate_hdl_module
-sd_name smartdesign_component_name \-hdl_module_name hdl_module_name \-hdl_file hdl_file \[-instance_name instance_name]

Arguments

-sd_name smartdesign_component_name
Specifies the name of the SmartDesign component. It is mandatory.
-hdl_module_name hdl_module_name
Specifies the name of the HDL module being instantiated in the SmartDesign component. It is mandatory.

**-hdl_file hdl_file**

Specifies the path of the HDL file in which the HDL module is defined. The HDL file path can be relative to project folder for imported files but the path has to be complete for linked files. It is mandatory.

**-instance_name instance_name**

Specifies the instance name of the HDL module. It is optional. By default, the instance name is <hdl_module_name>_<index> (index is an automatically generated integer starting at 0 such that the instance name is unique in the SmartDesign).

**Examples**

sd_instantiate_hdl_module -sd_name {top} -hdl_module_name {and1} -hdl_file {hdl\and1.v}

sd_instantiate_hdl_module -sd_name {top} -hdl_module_name {and_ex} -hdl_file {hdl\and_ex.v} -instance_name {test_hdl_hdl_module_name_plus1_1}

**See Also**

Tcl Command Documentation Conventions

### sd_instantiate_macro

Tcl command; instantiates a Microsemi primitive macro in a SmartDesign component.

```tcl
ds_instantiate_macro \
-sd_name smartdesign_component_name \
-macro_name macro_module_name | 
[-instance_name instance_name]
```

**Arguments**

**-sd_name smartdesign_component_name**

Specifies the name of the SmartDesign component. It is mandatory.

**-macro_name macro_module_name**

Specifies the name of the macro being instantiated in the SmartDesign component. It is mandatory.

**-instance_name instance_name**

Specifies the instance name of the macro. It is optional. By default, the instance name is <macro name>_<index> (index is an automatically generated integer starting at 0 such that the instance name is unique in the SmartDesign).

**Examples**

sd_instantiate_macro -sd_name {TOP} -macro_name {MX2} -instance_name {MX2_0}

sd_instantiate_macro -sd_name {TOP} -macro_name {MACC_PA}

**See Also**

Tcl Command Documentation Conventions

### sd_invert_pins

Tcl command; inverts one or more top level ports or instance level pins in a SmartDesign.

```tcl
ds_invert_pins \
-sd_name smartdesign_component_name \
-pin_names port_or_pin_names
```
Arguments

- sd_name smartdesign_component_name
  Specifies the name of the SmartDesign component. It is mandatory.
- pin_names port_or_pin_names
  Specifies the port or pin names to be inverted. It is mandatory. This parameter can take multiple values. This command will fail if the port/pin does not exist.

Examples

sd_invert_pins -sd_name {main} -pin_names {A}
sd_invert_pins -sd_name {main} -pin_names {MX2_1:S MX2_1:Y A B}

See Also
Tcl Command Documentation Conventions

sd_mark_pins_unused
Tcl command; marks one or more SmartDesign instance level output pins as unused. When an output pin is marked as unused, no Design Rule Check (DRC) warning will be printed for floating output pins while generating the SmartDesign.

sd_mark_pins_unused
- sd_name smartdesign_component_name
- pin_names port_or_pin_names

Arguments

- sd_name smartdesign_component_name
  Specifies the name of the SmartDesign component. It is mandatory.
- pin_names port_or_pin_names
  Specifies the names of the instance pins to be marked as unused. It is mandatory.

Examples

sd_mark_pins_unused -sd_name {top} -pin_names {PF_CCC_C0_0:PLL_LOCK_0}

Notes
This command will not work on multiple pins in this release. Support for multiple pins will be provided in the next Libero release.

See Also
Tcl Command Documentation Conventions

sd_remove_pins_from_group
Tcl command; removes one or more pins from a pin group on an instance in a SmartDesign.

sd_remove_pins_from_group
- sd_name smartdesign_component_name
- instance_name instance_name
- group_name group_name
- pin_names pin_names

Arguments

- sd_name smartdesign_component_name
Specifies the name of the SmartDesign component. It is mandatory.
- `instance_name instance_name`

Specifies the name of the instance on which the pin group is present. It is mandatory.
- `group_name group_name`

Specifies the name of the pin group from which pins need to be removed. It is mandatory.
- `pin_names pin_names`

Specifies the list of pin names to be removed from the pin group. It is mandatory.

Examples

```
sd_remove_pins_from_group -sd_name {TOP} -instance_name {COREAXI4INTERCONNECT_C0_0} -group_name {Group} -pin_names {ARESETN ACLK}
```

See Also

Tcl Command Documentation Conventions

### sd_rename_instance

Tcl command; renames an instance in a SmartDesign component. This command can be used to rename any type of instances (instances of other SmartDesigns components, core components, HDL modules, HDL+ cores and Microsemi macros) in a SmartDesign.

```
sd_rename_instance \\
-sd_name component_name \\
-current_instance_name instance_name \\
-new_instance_name new_instance_name
```

#### Arguments

- `sd_name component_name`
  Specifies the name of the SmartDesign component in which the instance name has to be renamed. It is mandatory.
- `current_instance_name instance_name`
  Specifies the name of the instance to be renamed. It is mandatory.
- `new_instance_name new_instance_name`
  Specifies the new instance name. It is mandatory.

#### Examples

```
sd_rename_instance -sd_name {top} -current_instance_name {DFN1_0} -new_instance_name {DFN1_new}
```

#### Notes

This command is not required to build a SmartDesign component. This command maps to an interactive user action in the SmartDesign Canvas and will not be present in the exported SmartDesign component Tcl description.

See Also

Tcl Command Documentation Conventions

### sd_rename_pin_group

Tcl command; renames a pin group on an instance in a SmartDesign component.
sd_rename_pin_group

sd_rename_pin_group
-\sd_name smartdesign_component_name
-\instance_name instance_name
-\current_group_name current_pin_group_name
-\new_pin_group_name new_pin_group_name

Arguments

-\sd_name smartdesign_component_name
  Specifies the name of the SmartDesign component. It is mandatory.
-\instance_name instance_name
  Specifies the name of the instance on which the pin group is present. It is mandatory.
-\current_group_name current_pin_group_name
  Specifies the name of the pin group to be renamed. It is mandatory.
-\new_group_name new_group_name
  Specifies the new name of the pin group. It is mandatory.

Examples

sd_rename_pin_group -\sd_name \{TOP\} -\instance_name \{COREAXIINTERCONNECT\_C0\_0\} -\current_group_name \{Group\} -\new_group_name \{MyNewGroup\}

See Also

Tcl Command Documentation Conventions

sd_rename_port

Tcl command; renames a SmartDesign port.

sd_rename_port
-\sd_name smartdesign_component_name
-\current_port_name port_name
-\new_port_name new_port_name

Arguments

-\sd_name smartdesign_component_name
  Specifies the name of the SmartDesign component. It is mandatory.
-\current_port_name port_name
  Specifies the name of the port to be renamed in the SmartDesign component. It is mandatory. Note that only port names can be renamed, and not port types (scalar ports cannot be renamed as bus ports and vice versa).
-\new_port_name new_port_name
  Specifies the new name of the specified port. It is mandatory.

Examples

sd_rename_port -\sd_name \{top\} -\library \{work\} -\current_port_name \{c1\} -\new_port_name \{c2\}

Notes

This command is not required to build a SmartDesign component. This command maps to an interactive user action in the SmartDesign Canvas and will not be present in the exported SmartDesign component Tcl description.
sd_save_core_instance_config

Tcl command; this command is used to save the core instance configuration specified using one or more 'sd_configure_core_instance' commands. This command is typically used after configuring a core instance in a SmartDesign, to save that core instance's configuration.

```bash
sd_save_core_instance_config
- sd_name smartdesign_component_name
- instance_name core_instance_name
```

**Arguments**

- `sd_name smartdesign_component_name`
  Specifies the name of the SmartDesign component. It is mandatory.

- `instance_name core_instance_name`
  Specifies the name of the core instance in the SmartDesign for which the configuration must be saved. It is mandatory.

**Examples**

sd_save_core_instance_config -sd_name {SD1} -instance_name {COREFIFO_0}

**See Also**

Tcl Command Documentation Conventions

sd_show_bif_pins

Tcl command; exposes one or more internal scalar or bus pins/ports of a Bus Interface pin/port. A Bus Interface pin/port is usually a group of normal scalar or bus pins/ports grouped together and used to connect instances that have similar interfaces. The internal pins/ports underneath the Bus Interface pin/port may have to be exposed in some cases to connect to some logic in the design.

```bash
sd_show_bif_pins
- sd_name smartdesign_component_name
- bif_pin_name name_of_the_bif_pin_or_port
- pin_names pins_or_ports_to_be_exposed
```

**Arguments**

- `sd_name smartdesign_component_name`
  Specifies the name of the SmartDesign component. It is mandatory.

- `bif_pin_name name_of_the_bif_pin_or_port`
  Specifies the name of the Bus Interface pin/port for which the internal pins/ports need to be exposed. It is mandatory.

- `pin_names pins_or_ports_to_be_exposed`
  Specifies the names of the Bus Interface internal pins/ports to be exposed. It is mandatory.

**Examples**

sd_show_bif_pins -sd_name {TOP} -bif_pin_name {COREAXI4INTERCONNECT_C0_0:AXI4mmaster0} -pin_names {COREAXI4INTERCONNECT_C0_0:MASTER0_AWADDR}
sd_show_bif_pins -sd_name {SD1} -bif_pin_name {CLKS_FROM_TXPLL_0} -pin_names {TX_PLL_LOCK_0}

**Notes**

This command will not expose multiple pins/ports in this release. Support to expose multiple scalar or bus pins/ports will be provided in the next Libero release.

**See Also**

Tcl Command Documentation Conventions

---

**sd_update_instance**

Tcl command; updates an instance in a SmartDesign with its latest definition. This command is useful when the interface (port-list) of the component/module instantiated in a SmartDesign has changed. This command can be used to update any type of instance such as instances of other SmartDesign components, core components, HDL modules and HDL+ cores in a SmartDesign.

```
sd_update_instance \
    -sd_name smartdesign_component_name \
    -instance_name instance_name
```

**Arguments**

- `sd_name smartdesign_component_name`
  Specifies the name of the SmartDesign component. It is mandatory.
- `instance_name`
  Specifies the name of the instance to be updated. It is mandatory.

**Examples**

```
sd_update_instance -sd_name {top} -instance_name {CORESMIP_C0_0}
```

**Notes**

This command is not required to build a SmartDesign component. This command maps to an interactive user action in the SmartDesign Canvas and will not be present in the exported SmartDesign component Tcl description.

**See Also**

Tcl Command Documentation Conventions
HDL Tcl Commands

create_hdl_core

This Tcl command is used to create a core component from an HDL core.

```
create_hdl_core
-module {module_name} \
-file {file_path} \
-library {library_name} \
-package {package_name}
```

Arguments

- `module {module_name}`
  Specify the module name for which you want to create a core component. This is a mandatory argument.
- `file {file_path}`
  Specify the file path of the module from which you create a core component. This is a mandatory argument.
- `library {library_name}`
  Specify the library name from which you want to create a HDL core. This is an optional argument.
- `package {package_name}`
  Specify the package name from which you want to create a core component. This is an optional argument.

Example

```
create_hdl_core -file {./HDL_CORE_TEST/hdl/hdl_core.v} -module {test_hdl_core}
```

See Also

Tcl Command Documentation Conventions

hdle_core_add_bif

This Tcl command adds a bus interface to an HDL core.

```
hdl_core_add_bif \
-hdl_core_name {hdl_core_name} \
-bif_definition {Name:Vendor:Library:Role} \
-bif_name {bus_interface_name} \
[-signal_map {signal_map}]
```

Arguments

- `module {module_name}`
  Specify the HDL core name to which the bus interface needs to be added. This is a mandatory argument.
- `bif_definition {Name:Vendor:Library:Role}`
  Specify the Bus Interface Definition Name, Vendor, Library and Bus Role of the core in the format [N:V:L:R]. This is a mandatory argument.
- `bif_name {bus_interface_name}`
  Specify the bus interface port name being added to the HDL core. This is a mandatory argument.
-signal_map {signal_map}

This argument is used to specify the signal map of the bus interface. This is an optional argument.

Example

dhdl_core_add_bif -hdl_core_name {test_hdl_core} -bif_definition {AHB:AMBA:AMBA2:master} -bif_name {BIF_1}

See Also
Tcl Command Documentation Conventions

hdl_core_assign_bif_signal
Maps a bus interface signal definition name to an HDL core module port name.

Arguments

-hdl_core_name {hdl_core_name}  
Specify the HDL core name to which the bus interface signal needs to be added. This is a mandatory argument.

-bif_name {bus_interface_name}  
Specify the bus interface name for which you want to map a core signal. This is a mandatory argument.

-bif_signal_name {bif_signal_name}  
Specify the bus interface signal name that you want to map with the core signal name. This is a mandatory argument.

-core_signal_name {core_signal_name}  
Specify the core signal name for which you want to map the bus interface signal name. This is a mandatory argument.

Example

dhdl_core_assign_bif_signal -hdl_core_name {test_hdl_core} -bif_name {BIF_1} -bif_signal_name {HWRITE} -core_signal_name {myHRESULT}

See Also
Tcl Command Documentation Conventions

hdl_core_delete_parameters
This Tcl command deletes parameters from a HDL core definition.

Arguments

-hdl_core_name {hdl_core_name}  
Specify the HDL core name from which you want to delete parameters. This is a mandatory argument.

-parameters {parameter_list}  

Specify the list of parameters from a HDL core. This is typically done to remove parameters from the list of parameters that was automatically extracted using the `hdl_core_extract_ports_and_params` command. This is a mandatory argument.

**Example**

```tcl
hdl_core_delete_parameters -hdl_core_name {test_hdl_core} -parameters {WIDTH}
```

**See Also**

[Tcl Command Documentation Conventions](#)

### `hdl_core_extract_ports_and_params`

This Tcl command automatically extracts ports and generic parameters from an HDL core module description.

```tcl
hdl_core_extract_ports_and_params \
-hdl_core_name {hdl_core_name}
```

**Arguments**

- `-hdl_core_name hdl_core_name`
  
  Specifies the HDL core name from which you want to extract signal names and generic parameters. This is a mandatory argument.

**Example**

```tcl
hdl_core_extract_ports_and_params -hdl_core_name {test_hdl_core}
```

**See Also**

[Tcl Command Documentation Conventions](#)

### `hdl_core_remove_bif`

Remove an existing bus interface from an HDL core.

```tcl
hdl_core_remove_bif \
-hdl_core_name {hdl_core_name} \
-bif_name {bus_interface_name}
```

**Arguments**

- `-module module_name`
  
  Specify the HDL core name from which the bus interface needs to be removed. This is a mandatory argument.

- `-bif_name bus_interface_name`
  
  Specify the bus interface name that needs to be removed from the HDL core. This is a mandatory argument.

**Example**

```tcl
hdl_core_remove_bif -hdl_core_name {mod1} -bif_name {BIF_1}
```

**See Also**

[Tcl Command Documentation Conventions](#)
**hdl_core_rename_bif**

**Rename an existing bus interface port of a HDL core.**

<table>
<thead>
<tr>
<th>Command</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>hdl_core_rename_bif</td>
<td>Rename an existing bus interface port of a HDL core.</td>
</tr>
<tr>
<td>-hdl_core_name</td>
<td>Specify the HDL core name for which the bus interface needs to be renamed.</td>
</tr>
<tr>
<td>-current_bif_name</td>
<td>Specify the bus old bus interface name that needs to be renamed for the HDL core.</td>
</tr>
<tr>
<td>-new_bif_name</td>
<td>Specify the new bus interface name that needs to be updated for the HDL core.</td>
</tr>
</tbody>
</table>

**Arguments**

- **-hdl_core_name** *{hdl_core_name}*
  Specify the HDL core name for which the bus interface needs to be renamed. This is a mandatory argument.

- **-current_bif_name** *{current_bus_interface_name}*
  Specify the bus old bus interface name that needs to be renamed for the HDL core. This is a mandatory argument.

- **-new_bif_name** *{new_bus_interface_name}*
  Specify the new bus interface name that needs to be updated for the HDL core. This is a mandatory argument.

**Example**

```tcl
hdl_core_rename_bif -hdl_core_name {test_hdl_plus} -current_bif_name {BIF_2} -new_bif_name {BIF_3}
```

**See Also**

[Tcl Command Documentation Conventions](#)

**hdl_core_unassign_bif_signal**

**Unmap an existing bus interface signal from a bus interface.**

<table>
<thead>
<tr>
<th>Command</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>hdl_core_unassign_bif_signal</td>
<td>Unmap an existing bus interface signal from a bus interface.</td>
</tr>
<tr>
<td>-hdl_core_name</td>
<td>Specify the HDL core name from which the bus interface signal needs to be deleted.</td>
</tr>
<tr>
<td>-bif_name</td>
<td>Specify the bus interface name for which you want to unassign a core signal.</td>
</tr>
<tr>
<td>-bif_signal_name</td>
<td>Specify the bus interface signal name for which you want to unassign a core signal.</td>
</tr>
</tbody>
</table>

**Arguments**

- **-hdl_core_name** *{hdl_core_name}*
  Specify the HDL core name from which the bus interface signal needs to be deleted. This is a mandatory argument.

- **-bif_name** *{bus_interface_name}*
  Specify the bus interface name for which you want to unassign a core signal. This is a mandatory argument.

- **-bif_signal_name** *{bus_interface_signal_name}*
  Specify the bus interface signal name for which you want to unassign a core signal. This argument is mandatory.

**Example**

```tcl
hdl_core_unassign_bif_signal -hdl_core_name {test_hdl_plus} -bif_name {BIF_2} -bif_signal_name {PENABLE}
```

**See Also**

[Tcl Command Documentation Conventions](#)
remove_hdl_core

This Tcl command removes an HDL core component from the current project.

```tcl
remove_hdl_core \
-hdl_core_name {hdl_core_name}
```

Arguments

-hdl_core_name {hdl_core_name}

Specify the module name from which you want to delete a core component. This is a mandatory argument.

Example

```tcl
remove_hdl_core -hdl_core_name {test_hdl_core}
```

See Also

Tcl Command Documentation Conventions
**Command Tools**

**CONFIGURE_CHAIN**

CONFIGURE_CHAIN is a command tool used in run_tool. The command `run_tool -name {CONFIGURE_CHAIN}` takes a script file that contains specific Tcl commands and passes them to FlashPro Express for execution.

```tcl
run_tool -name {CONFIGURE_CHAIN} -script {fpro_cmds.tcl}
```

*fpro_cmds.tcl* is a Tcl script that contains specific Tcl commands to configure JTAG chain. For details on JTAG chain programming Tcl commands, refer to the Tcl commands section in the Libero SoC Online Help.

Do not include any project-management commands such as open_project, save_project, or close_project in this *fpro_cmds.tcl* script file. The `run_tool -name {CONFIGURE_CHAIN}` command generates these project-management commands for you.

**Note:** For a new Libero project without a JTAG chain, executing this command causes Libero to first add the existing design device to the JTAG chain and then execute the commands from the script. If, for example, the script *fpro_cmds.tcl* contains commands to add four devices, executing the command `run_tool -name {CONFIGURE_CHAIN} -script {fpro_cmds.tcl}` will create a JTAG chain of the Libero design device and the four devices. For existing Libero projects that already have a JTAG chain, the command is executed on the existing JTAG chain.

**Example**

```tcl
run_tool -name {CONFIGURE_CHAIN} -script {d:/fpro_cmds.tcl}
```

#Example *fpro_cmds.tcl* command file for the –script parameter

```tcl
add_actel_device \
  -file {./sd_prj/sp_g3/designer/impl1/sd1.stp} \ 
  -name {dev1}
enable_device -name {MPF300TS_ES} -enable 0
add_non_actel_device \
  -ir 2 \ 
  -tck 1.00 \ 
  -name {Non-Microsemi Device}
add_non_actel_device \
  -ir 2 \ 
  -tck 1.00 \ 
  -name {Non-Microsemi Device (2)}
remove_device -name {Non-Microsemi Device}
set_device_to_highz -name {MPF300TS_ES} -highz 1
add_actel_device \
  -device {MPF300TS_ES} \ 
  -name {MPF300TS_ES (3)}
select_libero_design_device -name {MPF300TS_ES (3)}
```

**Return**

Returns 0 on success and 1 on failure.
**CONFIGURE_PROG_OPTIONS**

CONFIGURE_PROG_OPTIONS is a command tool used in configure_tool. Configure_tool -name (CONFIGURE_PROG_OPTIONS) sets the programming options.

```tcl
configure_tool -name {CONFIGURE_PROG_OPTIONS} 
-params {design_version:<value>} 
-params {silicon_signature:<value>}
```

The following table lists the parameter names and values.

<table>
<thead>
<tr>
<th>Name</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>design_version</td>
<td>Integer {0 through 65535}</td>
<td>Sets the design version. It must be greater than the Back level version in SPM Update Policy.</td>
</tr>
<tr>
<td>silicon_signature</td>
<td>Hex {&lt;max length 8 Hex characters&gt;}</td>
<td>32-bit (8 hex characters) silicon signature to be programmed into the device. This field can be read from the device using the JTAG USERCODE instruction.</td>
</tr>
</tbody>
</table>

**Example**

```tcl
configure_tool -name {CONFIGURE_PROG_OPTIONS} 
-params {design_version:255} 
-params {silicon_signature:abcdef}
```

**Return**

Returns 0 on success and 1 on failure.

---

**GENERATEPROGRAMMINGFILE**

GENERATEPROGRAMMINGFILE is a command tool used in the configure_tool and run_tool commands. The configure_tool -name (GENERATEPROGRAMMINGFILE) Tcl command configures tool options. The run_tool Tcl command runs the specified tool with the options specified in configure_tool.

```tcl
configure_tool \ 
- name {GENERATEPROGRAMMINGFILE} \ 
- params {program_fabric: true|false} \ 
- params {program_security: true|false} \ 
- params {program_snvm: true|false}
run_tool -name {GENERATEPROGRAMMINGFILE}
```

The following tables list the parameter names and values.
configure_tool –name {GENERATEPROGRAMMINGFILE} parameter:value pair

<table>
<thead>
<tr>
<th>Name</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>program_fabric</td>
<td>true</td>
<td>false</td>
</tr>
<tr>
<td>program_security</td>
<td>true</td>
<td>false</td>
</tr>
<tr>
<td>program_snvm</td>
<td>true</td>
<td>false</td>
</tr>
</tbody>
</table>

run_tool –name {GENERATEPROGRAMMINGFILE}

This command takes no parameters.

IO_PROGRAMMING_STATE

IO_PROGRAMMING_STATE is a command tool used in the configure_tool Tcl command. The configure_tool –name {IO_PROGRAMMING_STATE} Tcl command loads the I/O State information from a file during programming. The file used for loading the I/O State information during programming is specified in a parameter to the command. Refer to the Specify I/O States During Programming Dialog Box for details.

```tcl
configure_tool -name {IO_PROGRAMMING_STATE} -params
{ios_file:absolute_path_to_i/o_state_information_file}
```

Example

```tcl
configure_tool -name {IO_PROGRAMMING_STATE} -params
{ios_file:d:\sd_prj\tony_sf2\designer\sd1\sd1.ios}
```

Return

Returns 0 on success and 1 on failure.

PLACEROUTE

To place and route a design in Libero SoC, you must first configure the PLACEROUTE tool with the configure_tool command and then execute the PLACEROUTE tool with the run_tool command.

configure_tool

```tcl
configure_tool -name {PLACEROUTE} [-params [{name:value }]+]
```

Parameters

<table>
<thead>
<tr>
<th>Name</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TDPR</td>
<td>true</td>
<td>false</td>
</tr>
<tr>
<td>Name</td>
<td>Value</td>
<td>Description</td>
</tr>
<tr>
<td>-----------------</td>
<td>--------------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>PDPR</td>
<td>true</td>
<td>false</td>
</tr>
<tr>
<td>IOREG_COMBINING</td>
<td>true</td>
<td>false</td>
</tr>
<tr>
<td>GB_DEMOTION</td>
<td>true</td>
<td>false</td>
</tr>
<tr>
<td>EFFORT_LEVEL</td>
<td>true</td>
<td>false</td>
</tr>
<tr>
<td>INCRPLACEANDROUTE</td>
<td>true</td>
<td>false</td>
</tr>
<tr>
<td>REPAIR_MIN_DELAY</td>
<td>true</td>
<td>false</td>
</tr>
<tr>
<td>NUM_MULTI_PASSES</td>
<td>1-25</td>
<td></td>
</tr>
<tr>
<td>START_SEED_INDEX</td>
<td>1-100</td>
<td></td>
</tr>
<tr>
<td>MULTI_PASS_LAYOUT</td>
<td>true</td>
<td>false</td>
</tr>
<tr>
<td>MULTI_PASS_CRITERIA</td>
<td>SLOWEST_CLOCK</td>
<td>SPECIFIC_CLOCK</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SPECIFIC_CLOCK</td>
<td>Clock_Name</td>
<td>Applies only when MULTI_PASS_CRITERIA is set to SPECIFIC_CLOCK. It specifies the</td>
</tr>
<tr>
<td>Name</td>
<td>Value</td>
<td>Description</td>
</tr>
<tr>
<td>---------------------</td>
<td>---------</td>
<td>-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>name</td>
<td></td>
<td>name of the clock in the design used for Timing Violation Measurement.</td>
</tr>
</tbody>
</table>
| DELAY_ANALYSIS      | max | min | Used only when MULTI_PASS_CRITERIA is set to “VIOLATIONS”. Specifies the type of timing violations (slacks) to be examined. The default is ‘max’.  
• max: Use timing violations (slacks) obtained from maximum delay analysis  
• min: Use timing violations (slacks) obtained from minimum delay analysis. |
| STOP_ON_FIRST_PASS  | true | false | 1 | 0 | Applies only when MULTI_PASS_CRITERIA is set to “VIOLATIONS”. It stops performing remaining passes if all timing constraints have been met (when there are no negative slacks reported in the timing violations report).  
Note: The type of timing violations (slacks) used is determined by the ‘DELAY_ANALYSIS’ parameter. |
| SLACK_CRITERIA      | WORST_SLACK TOTAL_NEGATIVE_SLACK | Applies only when MULTI_PASS_CRITERIA is set to VIOLATIONS. Specifies how to evaluate the timing violations (slacks). The default is WORST_SLACK.  
• WORST_SLACK: The largest amount of negative slack (or least amount of positive slack if all constraints are met) for each pass is identified and then the largest value out of all passes will determine the best pass. This is the default.  
• TOTAL_NEGATIVE_SLACK: The sum of negative slacks from the first 100 paths for each pass in the Timing Violation report is identified. The largest value out of all passes will determine the best pass. If no negative slacks exist for a pass, then use the worst slack to evaluate that pass.  
Note: The type of timing violations (slacks) used is determined by the ‘DELAY_ANALYSIS’ parameter. |
| RGB_COUNT           | 1-18   | Allows an entity to override the placer’s RGB/RCLK bandwidth constraint. This option is useful for Block Creation.                                                                                       |

**Return Value**

Returns 0 on success and 1 on failure.

**run_tool**

run_tool -name (PLACEROUTE)
Parameters

None

Return Value

Returns 0 on success and 1 on failure.

Example

```tcl
configure_tool -name {PLACEROUTE} \
  -params {EFFORT_LEVEL:true} \
  -params {GB_DEMOTION:true} \
  -params {INCRPLACEANDROUTE:false} \
  -params {IOREG_COMBINING:false} \
  -params {MULTI_PASS_CRITERIA:VIOLATIONS} \
  -params {MULTI_PASS_LAYOUT:false} \
  -params {NUM_MULTI_PASSES:5} \
  -params {PDPR:false} \
  -params {REPAIR_MIN_DELAY:true} \
  -params {REPLICATION:false} \
  -params {RGB_COUNT:18} \
  -params {SLACK_CRITERIA:WORST_SLACK} \
  -params {SPECIFIC_CLOCK:} \
  -params {START_SEED_INDEX:1} \
  -params {STOP_ON_FIRST_PASS:false} \
  -params {TDPR:true} \
  -params {USE_RAM_MATH_INTERFACE_LOGIC:false}
run_tool -name {PLACEROUTE}
```

PROGRAMDEVICE

PROGRAMDEVICE is a command tool used in configure_tool and run_tool. Configure_tool allows you to configure the tool’s parameters and values prior to executing the tool. Run_tool executes the tool with the configured parameters.

To program the design in Libero SoC, you must first configure the PROGRAMDEVICE tool with configure_tool command and then execute the PROGRAMDEVICE command with the run_tool command.

Use the commands to configure your programming action and the programming procedures associated with the program action.

```tcl
configure_tool -name {PROGRAMDEVICE} \
  -params {prog_action:params_value} \
  -params {prog_optional_procedures:params_value} \
  -params {skip_recommended_procedures:params_value}
run_tool -name {PROGRAMDEVICE}
```

**configure_tool –name {PROGRAMDEVICE} parameter:value pair**

<table>
<thead>
<tr>
<th>Name</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>prog_action</td>
<td>String { PROGRAM</td>
<td>VERIFY</td>
</tr>
<tr>
<td></td>
<td>PROGRAM – Programs all selected family features: FPGA Array, targeted eNVM clients and security settings.</td>
<td></td>
</tr>
</tbody>
</table>
### PolarFire FPGA Tcl Commands Reference Guide

<table>
<thead>
<tr>
<th>Name</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>CATION</td>
<td>VERIFY_DIGEST}</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>prog_optional_procedures</td>
<td>Depends on the action from the prog_action parameter.</td>
<td>This parameter is optional. It is only required when the user wants to enable optional procedure.</td>
</tr>
<tr>
<td>skip_recommended_procedures</td>
<td>Depends on the action from the prog_action parameter.</td>
<td>This parameter is optional. It is used to deselect recommended procedures.</td>
</tr>
</tbody>
</table>

### run_tool –name {PROGRAMDEVICE} Parameter:value pair

<table>
<thead>
<tr>
<th>Name</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>None</td>
<td>None</td>
</tr>
</tbody>
</table>

### Example

```tcl
configure_tool \  
  -name {PROGRAMDEVICE} \  
  -params {prog_action:VERIFY_DIGEST} \  
  -params {prog_optional_procedures:DO_ENABLE_USER_PUBLIC_KEY} \  
  -params {skip_recommended_procedures:DO_ENABLE_FABRIC DO_ENABLE_SNVM}
```

```tcl
configure_tool -name {PROGRAMDEVICE} -params {prog_action:DEVICE_INFO}
run_tool -name {PROGRAMDEVICE} #Takes no parameters
```

### Return

`configure_tool -name {PROGRAMDEVICE}` returns 0 on success and 1 on failure.

`run_tool -name {PROGRAMDEVICE}` returns 0 on success and 1 on failure.
**PROGRAM_SPI_FLASH_IMAGE**

This Tcl command used in configure_tool and run_tool to program SPI Flash Image with configured parameters.

```
configure_tool \
-params {spi_flash_prog_action: PROGRAM_SPI_FLASH}
run_tool \
-params {spi_flash_prog_action: PROGRAM_SPI_FLASH}
```

**PROGRAMMER_INFO**

PROGRAMMER_INFO is a command tool used in configure_tool. Configure_tool -name {PROGRAMMER_INFO} sets the programmer settings, similar to the way FlashPro commands set the programmer settings. This command supports all five programmers: FlashPro3, FlashPro4, FlashPro5, FlashPro and FlashPro Lite.

```
configure_tool -name {PROGRAMMER_INFO} \
-params [{name: value}]
```

The following tables list the parameter names and values.

### configure_tool –name {PROGRAMMER_INFO} Parameter:value (FlashPro5)

<table>
<thead>
<tr>
<th>Name</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>flashpro5_clk_mode</td>
<td>String {free_running_clk</td>
<td>discrete_clocking}</td>
</tr>
<tr>
<td>flashpro5_force_freq</td>
<td>String {OFF</td>
<td>ON}</td>
</tr>
<tr>
<td>flashpro5_freq</td>
<td>Integer (Hertz)</td>
<td>For FlashPro5 Programmer only.</td>
</tr>
<tr>
<td>flashpro5_vpump</td>
<td>String {ON</td>
<td>OFF}</td>
</tr>
</tbody>
</table>

### configure_tool –name {PROGRAMMER_INFO} Parameter:value (FlashPro4)

<table>
<thead>
<tr>
<th>Name</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>flashpro4_clk_mode</td>
<td>String {free_running_clk</td>
<td>discrete_clocking}</td>
</tr>
<tr>
<td>flashpro4_force_freq</td>
<td>String {OFF</td>
<td>ON}</td>
</tr>
<tr>
<td>flashpro4_freq</td>
<td>Integer (Hertz)</td>
<td>For FlashPro4 Programmer only.</td>
</tr>
<tr>
<td>flashpro4_vpump</td>
<td>String {ON</td>
<td>OFF}</td>
</tr>
</tbody>
</table>

### configure_tool –name {PROGRAMMER_INFO} parameter:value (FlashPro3)

<table>
<thead>
<tr>
<th>Name</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>flashpro3_clk_mode</td>
<td>String {free_running_clk</td>
<td>discrete_clocking}</td>
</tr>
<tr>
<td>Name</td>
<td>Value</td>
<td>Description</td>
</tr>
<tr>
<td>-----------------</td>
<td>---------------------</td>
<td>-------------------------------------------------</td>
</tr>
<tr>
<td>flashpro3_force_freq</td>
<td>String {OFF</td>
<td>ON}</td>
</tr>
<tr>
<td>flashpro3_freq</td>
<td>Integer (Hertz)</td>
<td>For FlashPro3 Programmer only.</td>
</tr>
<tr>
<td>flashpro3_vpump</td>
<td>String {ON</td>
<td>OFF}</td>
</tr>
</tbody>
</table>

**configure_tool –name {PROGRAMMER_INFO} Parameter:value (FlashPro)**

<table>
<thead>
<tr>
<th>Name</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>flashpro_drive_trst</td>
<td>String {OFF</td>
<td>ON}</td>
</tr>
<tr>
<td>flashpro_force_freq</td>
<td>String {OFF</td>
<td>ON}</td>
</tr>
<tr>
<td>flashpro_force_vddp</td>
<td>String {ON</td>
<td>OFF}</td>
</tr>
<tr>
<td>flashpro_freq</td>
<td>Integer (Hertz)</td>
<td>For FlashPro Programmer only.</td>
</tr>
<tr>
<td>flashpro_vddl</td>
<td>String {ON</td>
<td>OFF}</td>
</tr>
<tr>
<td>flashpro_vddp</td>
<td>String {2.5V</td>
<td>3.3V}</td>
</tr>
<tr>
<td>flashpro_vpn</td>
<td>String {ON</td>
<td>OFF}</td>
</tr>
<tr>
<td>flashpro_vpp</td>
<td>String {ON</td>
<td>OFF}</td>
</tr>
</tbody>
</table>

For a detailed description of the parameters and values, refer to [Programmer Settings](#) in the Libero Online Help.

**Examples**

For FlashPro3 programmer

```bash
configure_tool –name {PROGRAMMER_INFO}\n   -params {flashpro3_clk_mode:free_running_clk}\n   -params {flashpro3_force_freq:OFF}\n   -params {flashpro3_freq:400000}\n   -params {flashpro3_vpump:ON}
```

For FlashPro4 programmer

```bash
configure_tool –name {PROGRAMMER_INFO}\n   -params {flashpro4_clk_mode:free_running_clk}\n   -params {flashpro4_force_freq:OFF}\n   -params {flashpro4_freq:400000}\n   -params {flashpro4_vpump:ON}
```

For FlashPro5 programmer

```bash
configure_tool –name {PROGRAMMER_INFO}\n   -params {flashpro5_clk_mode:free_running_clk}\n   -params {flashpro5_force_freq:OFF}\n   -params {flashpro5_freq:400000}\n   -params {flashpro5_vpump:ON}
```
For FlashPro programmer

```tcl
configure_tool -name {PROGRAMMER_INFO}\n  -params {flashpro_drive_trst:OFF}\n  -params {flashpro_force_freq:ON}\n  -params {flashpro_force_vddp:ON}\n  -params {flashpro_freq:400000}\n  -params {flashpro_vddl:ON}\n  -params {flashpro_vddp:2.5}\n  -params {flashpro_vpp:ON}\n  -params {flashpro_vpn:ON}
```

**Return**

Returns 0 on success and 1 on failure.

**SPM**

To configure security using Tcl, you must use the `configure_tool` Tcl command to pass the SPM configuration parameters.

```tcl
configure_tool -name {SPM}
  -params {name: value}
  [-params {name: value}]+  
```

**configure_tool –name {SPM} parameter:value pair**

**Note:** true | 1 will select the checkbox in the SPM UI

<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>back_level_protection</td>
<td>bool</td>
<td>false</td>
<td>true</td>
</tr>
<tr>
<td>back_level_update_version</td>
<td>Integer</td>
<td>0 - 65535</td>
<td></td>
</tr>
<tr>
<td>debug_passkey</td>
<td>hex</td>
<td>64 hex characters</td>
<td>Value of DPK; Debug Policy</td>
</tr>
<tr>
<td>disable_authenticate_action</td>
<td>bool</td>
<td>false</td>
<td>true</td>
</tr>
<tr>
<td>disable_autoprog_iap_services</td>
<td>bool</td>
<td>false</td>
<td>true</td>
</tr>
<tr>
<td>disable_debug_jtag_boundary_scan</td>
<td>bool</td>
<td>false</td>
<td>true</td>
</tr>
<tr>
<td>disable_debug_read_temp_volt</td>
<td>bool</td>
<td>false</td>
<td>true</td>
</tr>
<tr>
<td>disable_debug_ujtag</td>
<td>bool</td>
<td>false</td>
<td>true</td>
</tr>
<tr>
<td>disable_ext_zeroization</td>
<td>bool</td>
<td>false</td>
<td>true</td>
</tr>
<tr>
<td>Name</td>
<td>Type</td>
<td>Value</td>
<td>Description</td>
</tr>
<tr>
<td>-------------------------------------------</td>
<td>-------</td>
<td>-------------------</td>
<td>-----------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>disable_external_digest_check</td>
<td>bool</td>
<td>false</td>
<td>true</td>
</tr>
<tr>
<td>disable_jtag</td>
<td>bool</td>
<td>false</td>
<td>true</td>
</tr>
<tr>
<td>disable_program_action</td>
<td>bool</td>
<td>false</td>
<td>true</td>
</tr>
<tr>
<td>disable_puf_emulation</td>
<td>bool</td>
<td>false</td>
<td>true</td>
</tr>
<tr>
<td>disable_smartdebug_debug</td>
<td>bool</td>
<td>false</td>
<td>true</td>
</tr>
<tr>
<td>disable_smartdebug_live_probe</td>
<td>bool</td>
<td>false</td>
<td>true</td>
</tr>
<tr>
<td>disable_smartdebug_snvm</td>
<td>bool</td>
<td>false</td>
<td>true</td>
</tr>
<tr>
<td>disable_spi_slave</td>
<td>bool</td>
<td>false</td>
<td>true</td>
</tr>
<tr>
<td>disable_user_encryption_key_1</td>
<td>bool</td>
<td>false</td>
<td>true</td>
</tr>
<tr>
<td>disable_user_encryption_key_2</td>
<td>bool</td>
<td>false</td>
<td>true</td>
</tr>
<tr>
<td>disable_user_encryption_key_3</td>
<td>bool</td>
<td>false</td>
<td>true</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Note: UEK3 is only available for M2S060, M2GL060, M2S090, M2GL090, M2S150, and M2GL150 devices. All other devices will set this to false by default. See the SmartFusion2 SoC FPGA and IGLOO2 FPGA Security Best Practices User Guide for details. Key Mode Policy</td>
</tr>
<tr>
<td>disable_verify_action</td>
<td>bool</td>
<td>false</td>
<td>true</td>
</tr>
<tr>
<td>security_factory_access</td>
<td>string</td>
<td>open</td>
<td>disabled</td>
</tr>
</tbody>
</table>
### Table: Parameter Names, Types, Values, and Descriptions

<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>security_key_mode</td>
<td>string</td>
<td>custom</td>
<td>default</td>
</tr>
<tr>
<td>user_encryption_key_1</td>
<td>hex</td>
<td>64 hex characters</td>
<td>Value of UEK1</td>
</tr>
<tr>
<td>user_encryption_key_2</td>
<td>hex</td>
<td>64 hex characters</td>
<td>Value of UEK2</td>
</tr>
<tr>
<td>user_passkey_1</td>
<td>hex</td>
<td>64 hex characters</td>
<td>Value of Flashlock/UPK1</td>
</tr>
<tr>
<td>user_passkey_2</td>
<td>hex</td>
<td>64 hex characters</td>
<td>Value of UPK2</td>
</tr>
</tbody>
</table>

### Example

```tcl
configure_tool \
  -name {SPM} \
  -params {back_level_protection: false} \
  -params {back_level_update_version: 32} \
  -params {disable_smartdebug_live_probe: false} \
  -params {disable_smartdebug_snvm: false} \
  -params {disable_user_encryption_key_1: false} \
  -params {disable_user_encryption_key_2: false} \
```

### Return

Returns 0 on success and 1 on failure.

### SYNTHESIZE

SYNTHESIZE is a command tool used in configure_tool and run_tool. Configure_tool is a general-purpose Tcl command that allows you to configure a tool’s parameters and values prior to executing the tool. The run_tool Tcl command then executes the specified tool with the configured parameters.

To synthesize your design in Libero SoC, you first configure the synthesize tool with the configure_tool command and then execute the command with the run_tool command.

```tcl
configure_tool -name {SYNTHESIZE} \
  -params {name: value} \
  [-params {name: value}] \
run_tool -name {SYNTHESIZE}
```

The following tables list the parameter names and values.
configure_tool –name {SYNTHESIZE} parameter:value pair

<table>
<thead>
<tr>
<th>Name</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLOCK_ASYNC</td>
<td>Integer</td>
<td>Specifies the threshold value for asynchronous pin promotion to a global net. The default is 12.</td>
</tr>
<tr>
<td>CLOCK_GLOBAL</td>
<td>Integer</td>
<td>Specifies the threshold value for Clock pin promotion. The default is 2.</td>
</tr>
<tr>
<td>CLOCK_DATA</td>
<td>Integer value between 1000 and 200,000.</td>
<td>Specifies the threshold value for data pin promotion. The default is 5000.</td>
</tr>
<tr>
<td>RAM_OPTIMIZED_FOR_POWER</td>
<td>Boolean {true</td>
<td>false</td>
</tr>
<tr>
<td>RETIMING</td>
<td>Boolean {true</td>
<td>false</td>
</tr>
<tr>
<td>AUTO_COMPILE_POINT</td>
<td>Boolean {true</td>
<td>false</td>
</tr>
<tr>
<td>SYNPLIFY_OPTIONS</td>
<td>String</td>
<td>Specifies additional synthesis-specific options. Options specified by this parameter override the same options specified in the user Tcl file if there is a conflict.</td>
</tr>
<tr>
<td>SYNPLIFY_TCL_FILE</td>
<td>String</td>
<td>Specifies the absolute or relative path name to the user Tcl file containing synthesis-specific options.</td>
</tr>
<tr>
<td>BLOCK_MODE</td>
<td>Boolean {true</td>
<td>false</td>
</tr>
<tr>
<td>BLOCK_PLACEMENT_CONFLICTS</td>
<td>String {ERROR</td>
<td>KEEP</td>
</tr>
</tbody>
</table>
**PolarFire FPGA Tcl Commands Reference Guide**

<table>
<thead>
<tr>
<th>Name</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BLOCK_ROUTING_CONFLICTS</td>
<td>String {ERROR</td>
<td>KEEP</td>
</tr>
<tr>
<td>PA4_GB_COUNT</td>
<td>Integer</td>
<td>The number of available global nets is reported. Minimum for all dies is &quot;0&quot;. Default and Maximum values are die-dependent: 005/010 die: Default = Max = 8 025/050/060/090/150 die: Default=Max=16 RT4G075/RT4G150: Default=24, Max=48.</td>
</tr>
<tr>
<td>PA4_GB_MAX_RCLKINT_INSERTION</td>
<td>Integer</td>
<td>Specifies the maximum number of global nets that could be demoted to row-globals. Default is 16, Min is 0 and Max is 50.</td>
</tr>
<tr>
<td>PA4_GB_MIN_GB_FANOUT_TO_USE_RCLKINT</td>
<td>Integer</td>
<td>Specifies the Minimum fanout of global nets that could be demoted to row-globals. Default is 300. Min is 25 and Max is 5000.</td>
</tr>
<tr>
<td>SEQSHIFT_TO_URA_M</td>
<td>Boolean {0,1}</td>
<td>Specifies whether the Sequential-Shift Registers are to be mapped to Registers or 64x12 RAMs. If set to 1 (the default), the logic mapping is to Registers. If set to 0, the logic mapping is to Registers.</td>
</tr>
<tr>
<td>LANGUAGE_SYSTEM_VLOG</td>
<td>Boolean {true</td>
<td>false}</td>
</tr>
<tr>
<td>LANGUAGE_VERILOG_2001</td>
<td>Boolean {true</td>
<td>false}</td>
</tr>
</tbody>
</table>

**run_tool --name {SYNTHESIZE}**

**Example**

```
configure_tool --name {SYNTHESIZE} --params {BLOCK_MODE:false}\        
--params {BLOCK_PLACEMENT_CONFLICTS:ERROR} --params \ 
(BLOCK_ROUTING_CONFLICTS:ERROR) --params {CLOCK_ASYNC:12}\        
--params {CLOCK_DATA:5010} --params {CLOCK_GLOBAL:2} --params \ 
--params {PA4_GB_MAX_RCLKINT_INSERTION:16} --params \ 
(PA4_GB_MIN_GB_FANOUT_TO_USE_RCLKINT:299) --params \ 
(RAM_OPTIMIZED_FOR_POWER:false) --params {RETIMING:false} \ 
--params {AUTO_COMPILE_POINT:true} --params {SYNPLIFY_OPTIONS:
```
```
set_option -run_prop_extract 1;
set_option -maxfan 10000;
set_option -clock_globalthreshold 2;
set_option -async_globalthreshold 12;
set_option -globalthreshold 5000;
set_option -low_power_ram_decomp 0;\}
-params {SYNPLIFY_TCL_FILE:C:/Users/user1/Desktop/tclflow/synthesis/test.tcl}
```

```
run_tool -name {SYNTHESIZE} #Takes no parameters
```

**Return**

```
configure_tool -name {SYNTHESIZE}

Returns 0 on success and 1 on failure.
```

```
run_tool -name {SYNTHESIZE}

Returns 0 on success and 1 on failure.
```

**VERIFYPOWER**

VERIFYPOWER is a command tool used in run_tool. The command run_tool passes a script file that contains power-specific Tcl commands to the VERIFYPOWER command and executes it.

```
run_tool -name {VERIFYPOWER} -script {power_analysis.tcl}
```

where

<power_analysis.tcl> is a script that contains power-specific Tcl commands. You can include power-specific Tcl commands to generate power reports. See the sample power_analysis Tcl Script below for details.

**Return**

Returns 0 on success and 1 on failure.

**Example**

```
run_tool -name {VERIFYPOWER} -script {<power_analysis.tcl>}
```

**Sample power_analysis Tcl Script <power_analysis.tcl>**

The following example changes SmartPower operating condition settings from the default to 40C junction temperature and 1.25V VDD.

It then creates a report called A4P5000_uSRAM_POWER_64X18_power_report.txt.

```
# Change from pre-defined temperature and voltage mode (COM,IND,MIL) to SmartPower custom
smartpower_set_temperature_opcond -use "design"
smartpower_set_voltage_opcond -voltage "VDD" -use "design"

# Set the custom temperature to 40C ambient temperature.
smartpower_temperature_opcond_set_design_wide -typical 40 -best 40 -worst 40

# Set the custom voltage to 1.25V
smartpower_voltage_opcond_set_design_wide -voltage "VDD" -typical 1.25 -best 1.25 -worst 1.25
```

**VERIFYTIMING**

VERIFYTIMING is a command tool used in run_tool. Run_tool passes a script file that contains timing-specific Tcl commands to the VERIFYTIMING command and executes it.

```
run_tool -name {VERIFYTIMING} -script {timing.tcl}
```

where
<timing.tcl> is a script that contains SmartTime-specific Tcl commands. You can include SmartTime-specific Tcl commands to create user path sets and to generate timing reports. See sample the Sample SmartTime Tcl Script below for details.

Example

```
run_tool -name {VERIFYTIMING} -script {<timing.tcl>}
```

Return

Returns 0 on success and 1 on failure.

Sample SmartTime Tcl Script `<timing.tcl>`

```
# Create user path set from B_reg
create_set -name from_B_reg \ 
  -source {B_reg[*]:CLK} \ 
  -sink (*)

# Create user set from A, B, C
create_set -name from_in_ports \ 
  -source {A B C} \ 
  -sink (*)

# Generate Timing Reports
report \ 
  -type timing \ 
  -analysis min \ 
  -format text \ 
  -max_paths 10 \ 
  -print_paths yes \ 
  -max_expanded_paths 10 \ 
  -include_user_sets yes \ 
  min_timing.rpt

# Export SDC
write_sdc -scenario {Primary} exported.sdc

#save the changes
save
```

SIMULATE

Use the run_tool command to run simulation with your default simulation tool.

```
#Run Pre-synthesis simulation
run_tool -name {SIM_PRESYNTH}

#Run Post-synthesis simulation
run_tool -name {SIM_POSTSYNTH}
```

Return Value

Returns 0 on success and 1 on failure.
SmartTime Tcl Commands

create_set
Tcl command; creates a set of paths to be analyzed. Use the arguments to specify which paths to include. To create a set that is a subset of a clock domain, specify it with the -clock and -type arguments. To create a set that is a subset of an inter-clock domain set, specify it with the -source_clock and -sink_clock arguments. To create a set that is a subset (filter) of an existing named set, specify the set to be filtered with the -parent_set argument.

```
create_set -name <name> -parent_set <name> -type <set_type> -clock <clock name> -source_clock <clock name> -sink <port/pin pattern>
```

Arguments

- **-name <name>**
  Specifies a unique name for the newly created path set.
- **-parent_set <name>**
  Specifies the name of the set to filter from.
- **-clock <clock_name>**
  Specifies that the set is to be a subset of the given clock domain. This argument is valid only if you also specify the -type argument.
- **-type <value>**
  Specifies the predefined set type on which to base the new path set. You can only use this argument with the -clock argument, not by itself.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>reg_to_reg</td>
<td>Paths between registers in the design</td>
</tr>
<tr>
<td>async_to_reg</td>
<td>Paths from asynchronous pins to registers</td>
</tr>
<tr>
<td>reg_to_async</td>
<td>Paths from registers to asynchronous pins</td>
</tr>
<tr>
<td>external_recovery</td>
<td>The set of paths from inputs to asynchronous pins</td>
</tr>
<tr>
<td>external_removal</td>
<td>The set of paths from inputs to asynchronous pins</td>
</tr>
<tr>
<td>external_setup</td>
<td>Paths from input ports to registers</td>
</tr>
<tr>
<td>external_hold</td>
<td>Paths from input ports to registers</td>
</tr>
<tr>
<td>clock_to_out</td>
<td>Paths from registers to output ports</td>
</tr>
</tbody>
</table>

- **-in_to_out**
  Specifies that the set is based on the "Input to Output" set, which includes paths that start at input ports and end at output ports.
- **-source_clock <clock_name>**
  Specifies that the set will be a subset of an inter-clock domain set with the given source clock. You can only use this option with the -sink_clock argument.
-sink_clock <clock_name>
Specifies that the set will be a subset of an inter-clock domain set with the given sink clock. You can only use this option with the -source_clock argument.

-source <port/pin_pattern>
Specifies a filter on the source pins of the parent set. If you do not specify a parent set, this option filters all pins in the current design.

-sink <port/pin_pattern>
Specifies a filter on the sink pins of the parent set. If you do not specify a parent set, this option filters all pins in the current design.

Examples

create_set -name { my_user_set } -source { C* } -sink { D* }  
create_set -name { my_other_user_set } -parent_set { my_user_set } -source { CL* } 
create_set -name { adder } -source { ALU_CLOCK } -type { REG_TO_REG } -sink { ADDER*}  
create_set -name { another_set } -source_clock { EXTERN_CLOCK } -sink_clock { MY_GEN_CLOCK }

expand_path
Tcl command; displays expanded path information (path details) for paths. The paths to be expanded are identified by the parameters required to display these paths with list_paths. For example, to expand the first path listed with list_paths -clock {MYCLOCK} -type {register_to_register}, use the command expand_path -clock {MYCLOCK} -type {register_to_register}. Path details contain the pin name, type, net name, cell name, operation, delay, total delay, and edge as well as the arrival time, required time, and slack. These details are the same as details available in the SmartTime Expanded Path window.

Arguments

-index value
Specify the index of the path to be expanded in the list of paths. Default is 1.

-analysis {max | min}
Specify whether the timing analysis is done is max-delay (setup check) or min-delay (hold check). Valid values: max or min.

-format {csv | text}
Specify the list format. It can be either text (default) or csv (comma separated values). The former is suited for display the latter for parsing.

-set name
Displays a list of paths from the named set. You can either use the -set option to specify a user set by its name or use both -clock and -type to specify a set.

-clock clock name
Displays the set of paths belonging to the specified clock domain. You can either use this option along with -type to specify a set or use the -set option to specify the name of the set to display.

-type set_type
Specifies the type of paths in the clock domain to display in a list. You can only use this option with the -clock option. You can either use this option along with -clock to specify a set or use the -set option to specify a set name.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>reg_to_reg</td>
<td>Paths between registers in the design</td>
</tr>
<tr>
<td>external_setup</td>
<td>Path from input ports to registers</td>
</tr>
<tr>
<td>external_hold</td>
<td>Path from input ports to registers</td>
</tr>
<tr>
<td>clock_to_out</td>
<td>Path from registers to output ports</td>
</tr>
<tr>
<td>reg_to_async</td>
<td>Path from registers to asynchronous pins</td>
</tr>
<tr>
<td>external_recovery</td>
<td>Set of paths from inputs to asynchronous pins</td>
</tr>
<tr>
<td>external_removal</td>
<td>Set of paths from inputs to asynchronous pins</td>
</tr>
<tr>
<td>async_to_reg</td>
<td>Path from asynchronous pins to registers</td>
</tr>
</tbody>
</table>

-from_clock clock_name
Displays a list of timing paths for an inter-clock domain set belonging to the source clock specified. You can only use this option with the -to_clock option, not by itself.

-to_clock clock_name
Displays a list of timing paths for an inter-clock domain set belonging to the sink clock specified. You can only use this option with the -from_clock option, not by itself.

-analysis name
Specifies the analysis for the paths to be listed. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>maxdelay</td>
<td>Maximum delay analysis</td>
</tr>
<tr>
<td>mindelay</td>
<td>Minimum delay analysis</td>
</tr>
</tbody>
</table>

-index list_of_indices
Specifies which paths to display. The index starts at 1 and defaults to 1. Only values lower than the max_paths option will be expanded.

-format value
Specifies the file format of the output. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>text</td>
<td>ASCII text format</td>
</tr>
<tr>
<td>csv</td>
<td>Comma separated value file format</td>
</tr>
</tbody>
</table>

Examples

Note: The following example returns a list of five paths:

puts [expand_path -clock { myclock } -type {reg_to_reg }]


puts [expand_path -clock {myclock} -type {reg_to_reg} -index { 1 2 3 } -format text]

See Also
list_paths

list_paths

Tcl command; returns a list of the n worst paths matching the arguments. The number of paths returned can be changed using the set_options -limit_max_paths <value> command.

```
list_paths
-analysis <max | min>
-format <csv | text>
-set <name>
-clock <clock name>
-type <set_type>
-from_clock <clock name>
-to_clock <clock name>
-in_to_out
-from <port/pin pattern>
-to <port/pin pattern>
```

Arguments

-**-analysis** <max | min>
  Specifies whether the timing analysis is done for max-delay (setup check) or min-delay (hold check). Valid values are: max or min.

-**-format** <text | csv>
  Specifies the list format. It can be either text (default) or csv (comma separated values). Text format is better for display and csv format is better for parsing.

-**-set** <name>
  Returns a list of paths from the named set. You can either use the -set option to specify a user set by its name or use both -clock and -type to specify a set.

-**-clock** <clock name>
  Returns a list of paths from the specified clock domain. This option requires the -type option.

-**-type** <set_type>
  Specifies the type of paths to be included. It can only be used along with -clock. Valid values are:
  -reg_to_reg -- Paths between registers
  -external_setup -- Path from input ports to data pins of registers
  -external_hold -- Path from input ports to data pins of registers
  -clock_to_out -- Path from registers to output ports
  -reg_to_async -- Path from registers to asynchronous pins of registers
  -external_recovery -- Path from input ports to asynchronous pins of registers
  -external_removal -- Path from input ports to asynchronous pins of registers
  -async_to_reg -- Path from asynchronous pins to registers
  -from_clock <clock name>

  Used along with -to_clock to get the list of paths of the inter-clock domain between the two clocks.

-**-to_clock** <clock name>
  Used along with -from_clock to get the list of paths of the inter-clock domain between the two clocks.

-**-in_to_out**
  Used to get the list of path between input and output ports.

-**-from** <port/pin pattern>
  ```
Filter the list of paths to those starting from ports or pins matching the pattern.
- to <port/pin pattern>
Filter the list of paths to those ending at ports or pins matching the pattern.

Example

The following command displays the list of register to register paths of clock domain clk1:
puts [ list_paths -clock clk1 -type reg_to_reg ]

See Also
create_set
expand_path
set_options

read_sdc

The read_sdc Tcl command evaluate an SDC file, adding all constraints to the specified scenario (or the current/default one if none is specified). Existing constraints are removed if -add is not specified.

Arguments

- add
  Specifies that the constraints from the SDC file will be added on top of the existing ones, overriding them in case of a conflict. If not used, the existing constraints are removed before the SDC file is read.
- scenario scenario_name
  Specifies the scenario to add the constraints to. The scenario is created if none exists with this name.
- netlist (user | optimized)
  Specifies whether the SDC file contains object defined at the post-synthesis netlist (user) level or physical (optimized) netlist (used for timing analysis).
- pin_separator (: | /)
  Specify the pin separator used in the SDC file. It can be either ‘:’ or ‘/’.
  file name
  Specify the SDC file name.

Example

The following command removes all constraints from the current/default scenario and adds all constraints from design.sdc file to it:
read_sdc design.sdc

See Also
write_sdc
remove_set

Tcl command; removes a set of paths from analysis. Only user-created sets can be deleted.

remove_set -name name

Parameters

-name name
Specifies the name of the set to delete.

Example

The following command removes the set named my_set:

remove_set -name my_set

See Also
create_set

report

Tcl command; specifies the type of reports to generate and what to include in the reports.

report -type (timing | timing_violations | datasheet | bottleneck | constraints_coverage | combinational_loops)
  -analysis <max_or_min>\n  -format (csv|text)
  <filename>
  timing options
  -max_parallel_paths <number>
  -max_paths <number>
  -print_summary (yes|no)
  -use_slack_threshold (yes|no)
  -slack_threshold <double>
  -print_paths (yes|no)
  -max_expanded_paths <number>
  -include_user_sets (yes|no)
  -include_clock_domains (yes|no)
  -select_clock_domains <clock name list>
  -limit_max_paths (yes|no)
  -include_pin_to_pin (yes|no)
  bottleneck options
  -cost_type (path_count|path_cost)
  -max_instances <number>
  -from <port/pin pattern>
  -to <port/pin pattern>
  -set_type <set_type>
  -set_name <set name>
  -clock <clock name>
  -from_clock <clock name>
  -to_clock <clock name>
  -in_to_out

Arguments

-type
<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>timing</td>
<td>Timing Report</td>
</tr>
<tr>
<td>timing_violations</td>
<td>Timing Violation Report</td>
</tr>
<tr>
<td>datasheet</td>
<td>Datasheet Report</td>
</tr>
<tr>
<td>bottleneck</td>
<td>Bottleneck Report</td>
</tr>
<tr>
<td>constraints_coverage</td>
<td>Constraints Coverage Report</td>
</tr>
<tr>
<td>combinational_loops</td>
<td>Combinational Loops Report</td>
</tr>
</tbody>
</table>

```
-value
```

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>max</td>
<td>Timing report considers maximum analysis (default).</td>
</tr>
<tr>
<td>min</td>
<td>Timing report considers minimum analysis.</td>
</tr>
<tr>
<td>text</td>
<td>Generates a text report (default).</td>
</tr>
<tr>
<td>csv</td>
<td>Generates the report in a comma-separated value format which you can import into a spreadsheet.</td>
</tr>
</tbody>
</table>

```
-filename
```

Specifies the file name for the generated report.

**Timing Options and Values**

<table>
<thead>
<tr>
<th>Parameter/Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>-max_parallel_paths &lt;number&gt;</td>
<td>Specifies the max number of parallel paths. Parallel paths are timing paths with the same start and end points.</td>
</tr>
<tr>
<td>-max_paths &lt;number&gt;</td>
<td>Specifies the max number of paths to display for each set. This value is a positive integer value greater than zero. Default is 100.</td>
</tr>
<tr>
<td>-print_summary &lt;yes</td>
<td>no&gt;</td>
</tr>
<tr>
<td>-use_slack_threshold &lt;yes</td>
<td>no&gt;</td>
</tr>
<tr>
<td>-slack_threshold &lt;double&gt;</td>
<td>Specifies the threshold value to consider when reporting path slacks. This value is in nanoseconds (ns). By default, there is no threshold (all slacks reported).</td>
</tr>
<tr>
<td>-print_paths (yes</td>
<td>no)</td>
</tr>
</tbody>
</table>
### Parameter/Value

<table>
<thead>
<tr>
<th>Parameter/Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>-max_expanded_paths &lt;number&gt;</td>
<td>Specifies the max number of paths to expand per set. This value is a positive integer value greater than zero. Default is 100.</td>
</tr>
<tr>
<td>-include_user_sets (yes</td>
<td>no)</td>
</tr>
<tr>
<td>-include_clock_domains (yes</td>
<td>no)</td>
</tr>
<tr>
<td>-select_clock_domains &lt;clock_name_list&gt;</td>
<td>Defines the clock domain to be considered in the clock domain section. The domain list is a series of strings with domain names separated by spaces. Both the summary and the path sections in the timing report display only the listed clock domains in the clock_name_list.</td>
</tr>
<tr>
<td>-limit_max_paths (yes</td>
<td>no)</td>
</tr>
<tr>
<td>-include_pin_to_pin (yes</td>
<td>no)</td>
</tr>
</tbody>
</table>

### Bottleneck Options and Values

<table>
<thead>
<tr>
<th>Parameter/Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>-cost_type &lt;path_count</td>
<td>path_cost&gt;</td>
</tr>
<tr>
<td>-max_instances &lt;number&gt;</td>
<td>Specifies the maximum number of instances to be reported. Default is 10.</td>
</tr>
<tr>
<td>-from &lt;port/pin pattern&gt;</td>
<td>Reports only instances that lie on violating paths that start at locations specified by this option.</td>
</tr>
<tr>
<td>-to &lt;port/pin pattern&gt;</td>
<td>Reports only instances that lie on violating paths that end at locations specified by this option.</td>
</tr>
<tr>
<td>-clock &lt;clock name&gt;</td>
<td>This option allows pruning based on a given clock domain. Only instances that lie on these violating paths are reported.</td>
</tr>
<tr>
<td>-set_name &lt;set name&gt;</td>
<td>Displays the bottleneck information for the named set. You can either use this option or use both -clock and -type. This option allows pruning based on a given set. Only paths that lie within the named set will be considered towards bottleneck.</td>
</tr>
</tbody>
</table>
| -set_type <set_type>                | This option can only be used in combination with the -clock option, and not by itself. The options allows you to filter which type of paths should be considered towards the bottleneck:  
  - reg_to_reg - Paths between registers in the design  
  - async_to_reg - Paths from asynchronous pins to registers  
  - reg_to_async - Paths from registers to asynchronous pins |
### Parameter/Value

<table>
<thead>
<tr>
<th>Parameter/Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>external_recovery</td>
<td>The set of paths from inputs to asynchronous pins</td>
</tr>
<tr>
<td>external_removal</td>
<td>The set of paths from inputs to asynchronous pins</td>
</tr>
<tr>
<td>external_setup</td>
<td>Paths from input ports to registers</td>
</tr>
<tr>
<td>external_hold</td>
<td>Paths from input ports to registers</td>
</tr>
<tr>
<td>clock_to_out</td>
<td>Paths from registers to output ports</td>
</tr>
</tbody>
</table>

- **from_clock <clock name>**
  Reports only bottleneck instances that lie on violating timing paths of the inter-clock domain that starts at the source clock specified by this option. This option can only be used in combination with `-to_clock`.

- **to_clock <clock name>**
  Reports only instances that lie on violating paths that end at locations specified by this option.

- **in_to_out**
  Reports only instances that lie on violating paths that begin at input ports and end at output ports.

### Example

The following example generates a timing violation report named timing_viol.txt. The report considers an analysis using maximum delays and does not filter paths based on slack threshold. It reports two paths per section and one expanded path per section:

```
report -type timing_violations \
-analysis max -use_slack_threshold no \
-limit_max_paths -yes \
-max_paths 2 \
-max_expanded_paths 1\n
timing_viol.txt
```

### Save

Tcl command; saves all changes made prior to this command. This includes changes made on constraints, options and sets.

```
save
```

### Arguments

None

### Example

The following script sets the maximum number of paths reported by list_paths to 10, reads an SDC file, and save both the option and the constraints into the design project:

```
set_options -limit_max_paths 10
read_sdc somefile.sdc
save
```
set_options

SmartTime-specific Tcl command; sets options for timing analysis. Some options will also affect timing-driven place-and-route. The same parameters can be changed in the SmartTime Options dialog box in the SmartTime GUI.

**Arguments**

- **max_opcond value**
  Sets the operating condition to use for Maximum Delay Analysis.
  The acceptable Values for max_opcode for PolarFire is shown in the below table. Default is slow_lv_lt.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>slow_lv_lt</td>
<td>Use slow_lv_lt conditions for Maximum Delay Analysis</td>
</tr>
<tr>
<td>slow_hv_lt</td>
<td>Use slow_hv_lt conditions for Maximum Delay Analysis</td>
</tr>
<tr>
<td>fast_hv_lt</td>
<td>Use fast_hv_lt conditions for Maximum Delay Analysis</td>
</tr>
</tbody>
</table>

- **min_opcond value**
  Sets the operating condition to use for Minimum Delay Analysis.
  The acceptable Values for min_opcode for PolarFire is shown in the below table. Default is fast_hv_lt.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>fast_hv_lt</td>
<td>Use fast_hv_lt conditions for Maximum Delay Analysis</td>
</tr>
<tr>
<td>slow_hv_lt</td>
<td>Use slow_hv_lt conditions for Maximum Delay Analysis</td>
</tr>
<tr>
<td>slow_lv_lt</td>
<td>Use slow_lv_lt conditions for Maximum Delay Analysis</td>
</tr>
</tbody>
</table>

- **interclockdomain_analysis value**
  Enables or disables inter-clock domain analysis. Default is yes.
<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>yes</td>
<td>Enables inter-clock domain analysis</td>
</tr>
<tr>
<td>no</td>
<td>Disables inter-clock domain analysis</td>
</tr>
</tbody>
</table>

-use_bibuf_loopbacks value

Instructs the timing analysis whether to consider loopback path in bidirectional buffers (D->Y, E->Y) as false-path (no). Default is yes; i.e., loopback are false paths.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>yes</td>
<td>Enables loopback in bibufs</td>
</tr>
<tr>
<td>no</td>
<td>Disables loopback in bibufs</td>
</tr>
</tbody>
</table>

-enable_recovery_removal_checks value

Enables recovery checks to be included in max-delay analysis and removal checks in min-delay analysis. Default is yes.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>yes</td>
<td>Enables recovery and removal checks</td>
</tr>
<tr>
<td>no</td>
<td>Disables recovery and removal checks</td>
</tr>
</tbody>
</table>

-break_at_async value

Specifies whether or not timing analysis is allowed to cross asynchronous pins (clear, reset of sequential elements). Default is no.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>yes</td>
<td>Enables breaking paths at asynchronous ports</td>
</tr>
<tr>
<td>no</td>
<td>Disables breaking paths at asynchronous ports</td>
</tr>
</tbody>
</table>

-filter_when_slack_below value

Specifies a minimum slack value for paths reported by list_paths. Not set by default.

-filter_when_slack_above value

Specifies a maximum slack value for paths reported by list_paths. Not set by default.

-remove_slack_filters

Removes the slack minimum and maximum set using -filter_when_slack_below and filter_when_slack_above.

-limit_max_paths value

Specifies the maximum number of paths reported by list_paths. Default is 100.

-expand_clock_network value

Specify whether or not clock network details are reported in expand_path. Default is yes.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>yes</td>
<td>Enables expanded clock network information in paths</td>
</tr>
<tr>
<td>Value</td>
<td>Description</td>
</tr>
<tr>
<td>---------</td>
<td>-------------------------------------------------------</td>
</tr>
<tr>
<td>no</td>
<td>Disables expanded clock network information in paths</td>
</tr>
</tbody>
</table>

- **expand_parallel_paths** *value*
  Specify the number of parallel paths (paths with the same ends) to include in expand_path. Default is 1.

- **analysis_scenario** *value*
  Specify the constraint scenario to be used for timing analysis. Default is Primary, the default scenario.

- **tdpr_scenario** *value*
  Specify the constraint scenario to be used for timing-driven place-and-route. Default is Primary, the default scenario.

- **reset**
  Reset all options to the default values, except those for analysis and TDPR scenarios, which remain unchanged.

### Examples

The following script commands the timing engine to use best operating conditions for both max-delay analysis and min-delay analysis:

```tcl
set_options -max_opcond {best} -min_opcond {best}
```

The following script changes the scenario used by timing-driven place-and-route and saves the change in the Libero project for place-and-route tools to see the change.

```tcl
set_options -tdpr_scenario {My_TDPR_Scenario}
```

### See Also

- `save`
**SmartPower Tcl Commands**

**smartpower_add_new_scenario**

Tcl command; creates a new scenario.

```
smartpower_add_new_scenario -name {value} -description {value} -mode {value}
```

**Arguments**

- `-name {value}`
  Specifies the name of the new scenario.
- `-description {value}`
  Specifies the description of the new scenario.
- `-mode {<operating mode>:<duration>}+`
  Specifies the mode(s) and duration(s) for the specified scenario.

**Examples**

This example creates a new scenario called myscenario:
```
smartpower_add_new_scenario -name "MyScenario" -mode "Custom_1:50.00"
"Custom_2:25.00" -mode "Active:25.00"
```

**See Also**

Tcl documentation conventions

**smartpower_add_pin_in_domain**

Tcl command; adds a pin into a clock or set domain.

```
smartpower_add_pin_in_domain -pin_name {pin_name} -pin_type {value} -domain_name {domain_name} -domain_type {value}
```

**Arguments**

- `-pin_name {pin_name}`
  Specifies the name of the pin to add to the domain.
- `-pin_type {value}`
  Specifies the type of the pin to add. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>clock</td>
<td>The pin to add is a clock pin</td>
</tr>
<tr>
<td>data</td>
<td>The pin to add is a data pin</td>
</tr>
</tbody>
</table>

- `-domain_name {domain_name}`
  Specifies the name of the domain in which to add the specified pin.
- `-domain_type {value}`
  Specifies the type of domain in which to add the specified pin. The following table shows the acceptable values for this argument:
### Value

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>clock</td>
<td>The domain is a clock domain</td>
</tr>
<tr>
<td>set</td>
<td>The domain is a set domain</td>
</tr>
</tbody>
</table>

### Notes

- The `domain_name` must be a name of an existing domain.
- The `pin_name` must be a name of a pin that exists in the design.

### Examples

The following example adds a clock pin to an existing Clock domain:

```
smartpower_add_pin_in_domain -pin_name {XCMP3/U0/U1:Y} -pin_type {clock} -domain_name {clk1} -domain_type {clock}
```

The following example adds a data pin to an existing Set domain:

```
smartpower_add_pin_in_domain -pin_name {XCMP3/U0/U1:Y} -pin_type {data} -domain_name {myset} -domain_type {set}
```

### See Also

- [Tcl documentation conventions](#)
- [smartpower_remove_pin_of_domain](#)

### smartpower_battery_settings

This SmartPower Tcl command sets the battery capacity in SmartPower. The battery capacity is used to compute the battery life of your design.

```
smartpower_battery_settings `-capacity `decimal value```

#### Parameters

- `-capacity `decimal value``
  - Value must be a positive decimal.
  - This parameter is mandatory.

#### Exceptions

None

#### Returns

This command does not return a value.

#### Usage

The following table lists the parameters for the command, their types, and the values they can be set to.

<table>
<thead>
<tr>
<th>smartpower_battery_settings</th>
<th>Type</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>capacity</td>
<td>Decimal</td>
<td>Positive decimal</td>
<td>Specify the battery capacity in mA*Hours</td>
</tr>
</tbody>
</table>
Example

This example sets the battery capacity to 1800 mA * Hours.

smartpower_battery_settings -capacity {1800}

smartpower_change_clock_statistics

Tcl command; changes the default frequencies and probabilities for a specific domain.

smartpower_change_clock_statistics -domain_name {value} -clocks_freq {value} -clocks_proba {value} -registers_freq {value} -registers_proba {value} -set_reset_freq {value} -set_reset_proba {value} -primaryinputs_freq {value} -primaryinputs_proba {value} -combinational_freq {value} -combinational_proba {value}

Arguments

-domain_name {value}
Specifies the domain name in which to initialize frequencies and probabilities.

clocks_freq {value}
Specifies the user input frequency in Hz, KHz, or MHz for all clocks.

clocks_proba {value}
Specifies the user input probability in % for all clocks.

-registers_freq {value}
Specifies the user input frequency (in Hz, KHz, or MHz) or the toggle rate (in %). If the unit is not provided and toggle rate is active, the value is handled as a toggle rate; if toggle rate is not active, the value is handled as a frequency.

-registers_proba {value}
Specifies the user input probability in % for all registers.

-set_reset_freq {value}
Specifies the user input frequency (in Hz, KHz, or MHz) or the toggle rate (in %). If the unit is not provided and toggle rate is active, the value is handled as a toggle rate; if toggle rate is not active, the value is handled as a frequency.

-set_reset_proba {value}
Specifies the user input probability in % for all set/reset nets.

-primaryinputs_freq {value}
Specifies the user input frequency (in Hz, KHz, or MHz) or the toggle rate (in %). If the unit is not provided and toggle rate is active, the value is handled as a toggle rate; if toggle rate is not active, the value is handled as a frequency.

-primaryinputs_proba {value}
Specifies the user input probability in % for all primary inputs.

-combinational_freq {value}
Specifies the user input frequency (in Hz, KHz, or MHz) or the toggle rate (in %). If the unit is not provided and toggle rate is active, the value is handled as a toggle rate; if toggle rate is not active, the value is handled as a frequency.

-combinational_proba {value}
Specifies the user input probability in % for all combinational combinational output.

Note: This command is associated with the functionality of Initialize frequencies and probabilities dialog box.

Examples

The following example initializes all clocks with:

smartpower_change_clock_statistics -domain_name {my_domain} -clocks_freq {10 MHz} -clocks_proba {20} -registers_freq {10 MHz} -registers_proba {20} -set_reset_freq {10}
smartpower_change_setofpin_statistics

Tcl command; changes the default frequencies and probabilities for a specific set.

```
smartpower_change_setofpin_statistics -domain_name {value} -data_freq {value} -data_proba {value}
```

**Arguments**

- **-domain_name {value}**
  Specifies the domain name in which to initialize data frequencies and probabilities.
- **-data_freq {value}**
  Specifies the user input data frequency in Hz, KHz, or MHz for all sets of pins.
- **-data_proba {value}**
  Specifies the user input data probability in % for all sets of pins.

**Notes**

This command is associated with the functionality of **Initialize frequencies and probabilities** dialog box.

**Examples**

The following example initializes all clocks with:

```
smartpower_change_setofpin_statistics -domain_name {my_domain} -data_freq {10 MHz} -data_proba {20}
```

**See Also**

Tcl documentation conventions

---

smartpower_commit

Tcl command; saves the changes to the design file.

```
smartpower_commit
```

**Arguments**

None

**Examples**

```
smartpower_commit
```

**See Also**

Tcl documentation conventions

---

smartpower_compute_vectorless

This Tcl command executes a vectorless analysis of the current operating mode.
Arguments

None

Example

smartpower_compute_vectorless

See Also

Tcl Command Documentation Conventions

smartpower_create_domain

Tcl command; creates a new clock or set domain.

smartpower_create_domain -domain_type {value} -domain_name {domain_name}

Arguments

-domain_type {value}

Specifies the type of domain to create. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>clock</td>
<td>The domain is a clock domain</td>
</tr>
<tr>
<td>set</td>
<td>The domain is a set domain</td>
</tr>
</tbody>
</table>

-domain_name {domain_name}

Specifies the name of the new domain.

Notes

The domain name cannot be the name of an existing domain.
The domain type must be either clock or set.

Examples

The following example creates a new clock domain named "clk2":
smartpower_create_domain -domain_type {clock} -domain_name {clk2}
The following example creates a new set domain named "myset":
smartpower_create_domain -domain_type {set} -domain_name {myset}

See Also

Tcl documentation conventions
smartpower_remove_domain

smartpower_edit_scenario

Tcl command; edits a scenario.

smartpower_edit_scenario -name {value} -description {value} -mode {value} -new_name {value}

Arguments

-name {value}
Specifies the name of the scenario.
-\( \text{description} \) {\text{value}}
Specifies the description of the scenario.
-\( \text{mode} \) {<\text{operating mode}>:<\text{duration}>}
Specifies the mode(s) and duration(s) for the specified scenario.
-\( \text{new\_name} \) {\text{value}}
Specifies the new name for the scenario

**Examples**

This example edits the name of myscenario to finalscenario:
```
smartpower_edit_scenario -name myscenario -new_name finalscenario
```

**See Also**

[Tcl documentation conventions](#)

### smartpower_import_vcd

This SmartPower Tcl command imports into SmartPower a VCD file generated by a simulation tool. SmartPower extracts the frequency and probability information from the VCD.

```
import_vcd -file "\text{VCD file}" [-opmode "\text{mode name}" ] [-with\_vectorless "\text{TRUE} \mid \text{FALSE}" ] [-partial\_parse"\text{TRUE} \mid \text{FALSE}" ] [-start\_time "\text{decimal value}" ] [-end\_time "\text{decimal value}" ] [-auto\_detect\_top\_level\_name "\text{TRUE} \mid \text{FALSE}" ] [-top\_level\_name "\text{top level name}" ] [-glitch\_filtering"false \mid auto \mid true"] [-glitch\_threshold "\text{integer value}" ] [-stop\_time "\text{decimal value}" ]
```

**Parameters**

-\( \text{file} \) "\text{VCD file}"  
  Value must be a file path. This parameter is mandatory.
-\( \text{opmode} \) "\text{mode name}"  
  Value must be a string. This parameter is optional.
-\( \text{with\_vectorless} \) "\text{TRUE} \mid \text{FALSE}"
  Value must be a boolean. This parameter is optional.
-\( \text{partial\_parse} \) "\text{TRUE} \mid \text{FALSE}"
  Value must be a boolean. This parameter is optional.
-\( \text{start\_time} \) "\text{decimal value}"  
  Value must be a positive decimal. This parameter is optional.
-\( \text{end\_time} \) "\text{decimal value}"  
  Value must be a positive decimal. This parameter is optional.
-\( \text{auto\_detect\_top\_level\_name} \) "\text{TRUE} \mid \text{FALSE}"
  Value must be a boolean. This parameter is optional.
-\( \text{top\_level\_name} \) "\text{top level name}"  
  Value must be a string. This parameter is optional.
-\( \text{glitch\_filtering} \) "false \mid auto \mid true"
  Value must be one of false \mid auto \mid true. This parameter is optional.
-\( \text{glitch\_threshold} \) "\text{integer value}"
  Value must be a positive integer. This parameter is optional.
Exceptions
None

Returns
This command does not return a value.

Usage
This section lists all the parameters for the command, their types, and the values they can be set to. The default value is always listed first.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Type</th>
<th>Values</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>smartpower_import_vcd</td>
<td>String</td>
<td>Path to a VCD file</td>
<td>Path to a VCD file.</td>
</tr>
<tr>
<td>file</td>
<td>String</td>
<td>String</td>
<td>Path to a VCD file.</td>
</tr>
<tr>
<td>opmode</td>
<td>String</td>
<td>Operating mode name “Active” by default</td>
<td>Operating mode in which the VCD will be imported. If the mode doesn’t exist, it will be created.</td>
</tr>
<tr>
<td>with_vectorless</td>
<td>Boolean</td>
<td>TRUE</td>
<td>FALSE</td>
</tr>
<tr>
<td>partial_parse</td>
<td>Boolean</td>
<td>FALSE</td>
<td>TRUE</td>
</tr>
<tr>
<td>start_time</td>
<td>Decimal</td>
<td>positive decimal nanoseconds (ns)</td>
<td>Specify the starting timestamp of the VCD extraction in ns. It must be lower than the specified end_time. It must be lower than the last timestamp in the VCD file.</td>
</tr>
<tr>
<td>end_time</td>
<td>Decimal</td>
<td>positive decimal nanoseconds (ns)</td>
<td>Specify the end timestamp of the VCD extraction in ns. It must be higher than the specified start_time.</td>
</tr>
<tr>
<td>auto_detect_top_level_name</td>
<td>Boolean</td>
<td>TRUE</td>
<td>FALSE</td>
</tr>
<tr>
<td>top_level_name</td>
<td>Boolean</td>
<td>Full hierarchical name</td>
<td>Specify the full hierarchical name of the instance of the design in the VCD file.</td>
</tr>
<tr>
<td>glitch_filtering</td>
<td>Boolean</td>
<td>Auto</td>
<td>FALSE</td>
</tr>
</tbody>
</table>
PolarFire FPGA Tcl Commands Reference Guide

<table>
<thead>
<tr>
<th>smartpower_import_vcd</th>
<th>Type</th>
<th>Values</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>glitch_threshold</td>
<td>Integer</td>
<td>Positive integer</td>
<td>Specify the threshold in ps below which glitches are filtered out.</td>
</tr>
</tbody>
</table>

**Examples**

The Tcl command below imports the power.vcd file generated by the simulator into SmartPower:

```
smartpower_import_vcd -file "../../../simulation/power.vcd"
```

The Tcl command below extracts information between 1ms and 2ms in the simulation, and stores the information into a custom mode:

```
smartpower_import_vcd -file "../../../simulation/power.vcd" -partial_parse TRUE -start_time 1000000 -end_time 2000000 -opmode "power_1ms_to_2ms"
```

**smartpower_init_do**

Tcl command; initializes the frequencies and probabilities for clocks, registers, set/reset nets, primary inputs, combinational outputs, enables and other sets of pins, and selects a mode for initialization.

```
smartpower_init_do -with {value} -opmode {value} -clocks {value} -registers {value} -set_reset {value} -primaryinputs {value} -combinational {value} -enables {value} -othersets {value}
```

**Arguments**

- **-with {value}**
  
  This sets the option of initializing frequencies and probabilities with vectorless analysis or with fixed values. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>vectorless</td>
<td>Initializes frequencies and probabilities with vectorless analysis</td>
</tr>
<tr>
<td>fixed</td>
<td>Initializes frequencies and probabilities with fixed values</td>
</tr>
</tbody>
</table>

- **-opmode {value}**
  
  Optional; specifies the mode in which to initialize frequencies and probabilities. The value must be Active or Flash*Freeze.

- **-clocks {value}**
  
  This sets the option of initializing frequencies and probabilities for all clocks. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>true</td>
<td>Initializes frequencies and probabilities for all clocks</td>
</tr>
<tr>
<td>false</td>
<td>Does not initialize frequencies and probabilities for all clocks</td>
</tr>
</tbody>
</table>

- **-registers {value}**
  
  This sets the option of initializing frequencies and probabilities for all registers. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>true</td>
<td>Initializes frequencies and probabilities for all registers</td>
</tr>
</tbody>
</table>
### -set_reset {value}

This sets the option of initializing frequencies and probabilities for all set/reset nets. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>true</td>
<td>Initializes frequencies and probabilities for all set/reset nets</td>
</tr>
<tr>
<td>false</td>
<td>Does not initialize frequencies and probabilities for all set/reset nets</td>
</tr>
</tbody>
</table>

### -primaryinputs{value}

This sets the option of initializing frequencies and probabilities for all primary inputs. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>true</td>
<td>Initializes frequencies and probabilities for all primary inputs</td>
</tr>
<tr>
<td>false</td>
<td>Does not initialize frequencies and probabilities for all primary inputs</td>
</tr>
</tbody>
</table>

### -combinational {value}

This sets the option of initializing frequencies and probabilities for all combinational outputs. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>true</td>
<td>Initializes frequencies and probabilities for all combinational outputs</td>
</tr>
<tr>
<td>false</td>
<td>Does not initialize frequencies and probabilities for all combinational outputs</td>
</tr>
</tbody>
</table>

### -enables {value}

This sets the option of initializing frequencies and probabilities for all enable sets of pins. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>true</td>
<td>Initializes frequencies and probabilities for all enable sets of pins</td>
</tr>
<tr>
<td>false</td>
<td>Does not initialize frequencies and probabilities for all enable sets of pins</td>
</tr>
</tbody>
</table>

### -othersets {value}

This sets the option of initializing frequencies and probabilities for all other sets of pins. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>true</td>
<td>Initializes frequencies and probabilities for all other sets of pins</td>
</tr>
<tr>
<td>false</td>
<td>Does not initialize frequencies and probabilities for all other sets of pins</td>
</tr>
</tbody>
</table>
### smartpower_init_set_clocks_options

Tcl command; initializes the clock frequency options of all clock domains.

**Examples**

The following example initializes all clocks with:

```tcl
smartpower_init_do -with {vectorless} -opmode {my_mode} -clocks {true} -registers {true} -asynchronous {true} -primaryinputs {true} -combinational {true} -enables {true} -othersets {true}
```

**Arguments**

- **-with_clock_constraints {value}**
  
  This sets the option of initializing the clock frequencies with frequency constraints from SmartTime. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>true</td>
<td>Sets initialize clock frequencies with clock constraints ON</td>
</tr>
<tr>
<td>false</td>
<td>Sets initialize clock frequencies with clock constraints OFF</td>
</tr>
</tbody>
</table>

- **-with_default_values {value}**
  
  This sets the option of initializing the clock frequencies with a user input default value. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>true</td>
<td>Sets initialize clock frequencies with default values ON</td>
</tr>
<tr>
<td>false</td>
<td>Sets initialize clock frequencies with default values OFF</td>
</tr>
</tbody>
</table>

- **-freq {value}**

  Specifies the user input frequency in Hz, KHz, or MHz.

- **-duty_cycle {value}**

  Specifies the user input duty cycles in %.

**Notes**

This command is associated with the functionality of [Initialize frequencies and probabilities](#) dialog box.
Examples

The following example initializes all clocks after executing `smartpower_init_do` with `-clocks {true}`:
```
smartpower_init_set_clocks_options -with_clock_constraints {true} -with_default_values {true} -freq {10 MHz} -duty_cycle (20)
```

See Also

[Tcl documentation conventions](#)

smartpower_init_set_combinational_options

Tcl commands; initializes the frequency and probability of all combinational outputs.
```
smartpower_init_set_combinational_options -freq {value} -proba {value}
```

Arguments

- `-freq {value}`
  Specifies the user input frequency (in Hz, KHz, or MHz) or the toggle rate (in %). If the unit is not provided and toggle rate is active, the value is handled as a toggle rate; if toggle rate is not active, the value is handled as a frequency.
- `-proba {value}`
  Specifies the user input probability in %.

Notes

This command is associated with the functionality of [Initialize frequencies and probabilities](#) dialog box.

Examples

The following example initializes all combinational signals after executing `smartpower_init_do` with `-combinational {true}`:
```
smartpower_init_set_combinational_options -freq {10 MHz} -proba (20)
```

See Also

[Tcl documentation conventions](#)

smartpower_init_set_enables_options

Tcl command; initializes the clock frequency of all enable clocks with the initialization options.
```
smartpower_init_set_enables_options -freq {value} -proba {value}
```

Arguments

- `-freq {value}`
  Specifies the user input frequency (in Hz, KHz, or MHz).
- `-proba {value}`
  Specifies the user input probability in %.

Notes

This command is associated with the functionality of [Initialize frequencies and probabilities](#) dialog box.
Examples

The following example initializes all clocks after executing `smartpower init do` with -enables {true}:

```
smartpower_init_set_enables_options -freq 10 MHz -proba 20
```

See Also

- [Tcl documentation conventions](#)

**smartpower_init_set_primaryinputs_options**

Tcl command; initializes the frequency and probability of all primary inputs.

```
smartpower_init_set_primaryinputs_options -freq {value} -proba {value}
```

**Arguments**

- `-freq {value}`
  Specifies the user input frequency (in Hz, KHz, or MHz) or the toggle rate (in %). If the unit is not provided and toggle rate is active, the value is handled as a toggle rate; if toggle rate is not active, the value is handled as a frequency.

- `-proba {value}`
  Specifies the user input probability in %.

**Notes**

This command is associated with the functionality of [Initialize frequencies and probabilities](#) dialog box.

Examples

The following example initializes all primary inputs after executing `smartpower init do` with -primaryinputs {true}:

```
smartpower_init_set_primaryinputs_options -freq 10 MHz -proba 20
```

See Also

- [Tcl documentation conventions](#)

**smartpower_init_set_registers_options**

Tcl command; initializes the frequency and probability of all register outputs.

```
smartpower_init_set_registers_options -freq {value} -proba {value}
```

**Arguments**

- `-freq {value}`
  Specifies the user input frequency (in Hz, KHz, or MHz) or the toggle rate (in %). If the unit is not provided and toggle rate is active, the value is handled as a toggle rate; if toggle rate is not active, the value is handled as a frequency.

- `-proba {value}`
  Specifies the user input probability in %.

**Notes**

This command is associated with the functionality of [Initialize frequencies and probabilities](#) dialog box.
Exceptions

None

Examples

The following example initializes all register outputs after executing `smartpower_init_do` with `-registrations {true}:
```
smartpower_init_set_registers_options -freq {10 MHz} -proba {20}
```

See Also

Tcl documentation conventions

smartpower_init_setofpins_values

Tcl command; initializes the frequency and probability of all sets of pins.
```
smartpower_init_setofpins_values -domain_name {name} -freq {value} -proba {value}
```

Arguments

- `-domain_name {name}`
  Specifies the set of pins that will be initialized. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IOsEnableSet</td>
<td>Specifies that the IOsEnableSet set of pins will be initialized</td>
</tr>
<tr>
<td>MemoriesEnableSet</td>
<td>Specifies that the MemoriesEnableSet set of pins will be initialized</td>
</tr>
</tbody>
</table>

- `-freq {value}`
  Specifies the user input frequency in Hz, MHz, or KHz.

- `-proba {value}`
  Specifies the user input probability in %.

Notes

This command is associated with the functionality of Initialize frequencies and probabilities dialog box.

Examples

The following example initializes all primary inputs after executing `smartpower_init_do` with `-othersets {true}:
```
smartpower_init_setofpins_values -domain_name {IOsEnableSet} -freq {10 MHz} -proba {20}
```

See Also

Tcl documentation conventions

smartpower_remove_all_annotations

Tcl command; removes all initialization annotations for the specified mode.
```
smartpower_remove_all_annotations -opmode {value}
```
Arguments

- omode \{value\}

Removes all initialization annotations for the specified mode, where value must be Active or Flash*Freeze.

Notes

This command is associated with the functionality of Initialize frequencies and probabilities dialog box.

Examples

The following example initializes all clocks with omode Acitve:

smartpower_remove_all_annotations -opmode \{Active\}

See Also

Tcl documentation conventions

smartpower_remove_file

Tcl command; removes a VCD file from the specified mode or all operating mode. Frequency and probability information of signals annotated by the VCD are set back to the default value.

<table>
<thead>
<tr>
<th>Argument</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>-file {value}</td>
<td>Specifies the file to be removed. This is mandatory.</td>
</tr>
<tr>
<td>-format {value}</td>
<td>Specifies that the type to be removed is a VCD file. This is mandatory.</td>
</tr>
<tr>
<td>[-opmode {value}]</td>
<td>Specifies the operating mode. This is optional. The following table shows the acceptable values for this argument:</td>
</tr>
<tr>
<td>Value</td>
<td>Description</td>
</tr>
<tr>
<td>-----------------</td>
<td>----------------------------------</td>
</tr>
<tr>
<td>Active</td>
<td>The operating mode is set to active</td>
</tr>
<tr>
<td>Static (PolarFire)</td>
<td>The operating mode is set to Static</td>
</tr>
<tr>
<td>Flash*Freeze</td>
<td>The operating mode is set to Flash*Freeze</td>
</tr>
</tbody>
</table>

Examples

This example removes the file test.vcd from the Active mode.

smartpower_remove_file -file "test.vcd" -format VCD -opmode "Active"

This example removes the VCD file power1.vcd from all operating modes:

smartpower_remove_file -file "power1.vcd" -format VCD

See Also

Tcl documentation conventions
smartpower_remove_scenario
Tcl command; removes a scenario from the current design.

```tcl
smartpower_remove_scenario -name {value}
```

**Arguments**

- `-name {value}`
  Specifies the name of the scenario.

**Examples**

This example removes a scenario from the current design:

```tcl
smartpower_remove_scenario -name myscenario
```

**See Also**

Tcl documentation conventions

---

smartpower_report_power
Tcl command; creates a Power report, which enables you to determine if you have any power consumption problems in your design. It includes information about the global device and SmartPower preferences selection, and hierarchical detail (including gates, blocks, and nets), with a block-by-block, gate-by-gate, and net-by-net power summary SmartPower results.

```tcl
smartpower_report_power\[-powerunit {value}] \[-frequnit {value}] \[-opcond {value}] \[-opmode {value}] \[-toggle {value}] \[-power_summary {value}] \[-rail_breakdown{value}] \[-type_breakdown{ value}] \[-clock_breakdown{value}] \[-thermal_summary {value}] \[-battery_life {value}] \[-opcond_summary {value}] \[-clock_summary {value}] \[-style {value}] \[-sortorder {value}] \[-sortby {value}] \[-instance_breakdown {value}] \[-power_threshold {value}] \[-min_power {number}] \[-max_instance {integer >= 0}] \[-activity_sortorder {value}] \[-activity_sortby {value}] \[-activity_summary {value}] \[-frequency_threshold {value}] \[-filter_pin {value}] \[-min_frequency {value}] \[-max_pin {value}] \[-enablerates_sortorder {value}] \[-enablerates_sortby {value}] \[-enablerates_summary {value}]
```
Arguments

-powerunit {value}
Specifies the unit in which power is set. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>W</td>
<td>The power unit is set to watts</td>
</tr>
<tr>
<td>mW</td>
<td>The power unit is set to milliwatts</td>
</tr>
<tr>
<td>uW</td>
<td>The power unit is set to microwatts</td>
</tr>
</tbody>
</table>

-frequnit {value}
Specifies the unit in which frequency is set. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hz</td>
<td>The frequency unit is set to hertz</td>
</tr>
<tr>
<td>kHz</td>
<td>The frequency unit is set to kilohertz</td>
</tr>
<tr>
<td>MHz</td>
<td>The frequency unit is set to megahertz</td>
</tr>
</tbody>
</table>

-opcond {value}
Specifies the operating condition. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>worst</td>
<td>The operating condition is set to worst case</td>
</tr>
<tr>
<td>typical</td>
<td>The operating condition is set to typical case</td>
</tr>
<tr>
<td>best</td>
<td>The operating condition is set to best case</td>
</tr>
</tbody>
</table>

-opmode {value}
Specifies the operating mode. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Active</td>
<td>The operating mode is set to Active</td>
</tr>
<tr>
<td>Standby</td>
<td>The operating mode is set to Standby</td>
</tr>
<tr>
<td>Flash*Freeze</td>
<td>The operating mode is set to Flash*Freeze</td>
</tr>
</tbody>
</table>

-toggle {value}
Specifies the toggle. The following table shows the acceptable values for this argument:
<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>true</td>
<td>The toggle is set to true</td>
</tr>
<tr>
<td>false</td>
<td>The toggle is set to false</td>
</tr>
</tbody>
</table>

```
power_summary {value}
```
Specifies whether to include the power summary, which shows the static and dynamic values in the report. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>true</td>
<td>Includes the power summary in the report</td>
</tr>
<tr>
<td>false</td>
<td>Does not include the power summary in the report</td>
</tr>
</tbody>
</table>

```
rail_breakdown {value}
```
Specifies whether to include the breakdown by rail summary in the report. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>true</td>
<td>Includes the breakdown by rail summary in the report</td>
</tr>
<tr>
<td>false</td>
<td>Does not include the breakdown by rail summary in the report</td>
</tr>
</tbody>
</table>

```
type_breakdown {value}
```
Specifies whether to include the breakdown by type summary in the report. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>true</td>
<td>Includes the breakdown by type summary in the report</td>
</tr>
<tr>
<td>false</td>
<td>Does not include the breakdown by type summary in the report</td>
</tr>
</tbody>
</table>

```
lock_breakdown {value}
```
Specifies whether to include the breakdown by clock domain in the report. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>true</td>
<td>Includes the breakdown by clock domain summary in the report</td>
</tr>
<tr>
<td>false</td>
<td>Does not include the breakdown by clock domain summary in the report</td>
</tr>
</tbody>
</table>

```
thermal_summary {value}
```
Specifies whether to include the thermal summary in the report. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>true</td>
<td>Include the thermal summary in the report</td>
</tr>
<tr>
<td>false</td>
<td>Do not include the thermal summary in the report</td>
</tr>
</tbody>
</table>
### Value Description

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>true</td>
<td>Includes the thermal summary in the report</td>
</tr>
<tr>
<td>false</td>
<td>Does not include the thermal summary in the report</td>
</tr>
</tbody>
</table>

**-battery_life {value}**

Specifies whether to include the battery life summary in the report. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>true</td>
<td>Includes the battery life summary in the report</td>
</tr>
<tr>
<td>false</td>
<td>Does not include the battery life summary in the report</td>
</tr>
</tbody>
</table>

**-opcond_summary {value}**

Specifies whether to include the operating conditions summary in the report. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>true</td>
<td>Includes the operating conditions summary in the report</td>
</tr>
<tr>
<td>false</td>
<td>Does not include the operating conditions summary in the report</td>
</tr>
</tbody>
</table>

**-clock_summary {value}**

Specifies whether to include the clock domains summary in the report. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>true</td>
<td>Includes the clock summary in the report</td>
</tr>
<tr>
<td>false</td>
<td>Does not include the clock summary in the report</td>
</tr>
</tbody>
</table>

**-style {value}**

Specifies the format in which the report will be exported. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Text</td>
<td>The report will be exported as Text file</td>
</tr>
<tr>
<td>CSV</td>
<td>The report will be exported as CSV file</td>
</tr>
</tbody>
</table>

**-sortby {value}**

Specifies how to sort the values in the report. The following table shows the acceptable values for this argument:
### Value Description

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>power values</td>
<td>Sorts based on the power values</td>
</tr>
<tr>
<td>alphabetical</td>
<td>Sorts in an alphabetical order</td>
</tr>
</tbody>
</table>

**-sortorder {value}**

Specifies the sort order of the values in the report. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ascending</td>
<td>Sorts the values in ascending order</td>
</tr>
<tr>
<td>descending</td>
<td>Sorts the values in descending order</td>
</tr>
</tbody>
</table>

**-instance_breakdown {value}**

Specifies whether to include the breakdown by instance in the report. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>true</td>
<td>Includes the breakdown by instance in the report</td>
</tr>
<tr>
<td>false</td>
<td>Does not include the breakdown by instance in the report</td>
</tr>
</tbody>
</table>

**-power_threshold {value}**

This specifies whether to include only the instances that consume power above a certain minimum value. When this command is set to true, the `-min_power` argument must also be used to specify that only the instances that consume power above this minimum power value are the ones that are included in the report. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>true</td>
<td>Includes the power threshold in the report</td>
</tr>
<tr>
<td>false</td>
<td>Does not include the power threshold in the report</td>
</tr>
</tbody>
</table>

**-filter_instance {value}**

This specifies whether to have a limit on the number of instances to include in the Power report. When this command is set to true, the `-max_instance` argument must also be used to specify the maximum number of instances to be included into the Power report. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>true</td>
<td>Indicates that you want to have a limit on the number of instances to include in the Power report</td>
</tr>
<tr>
<td>false</td>
<td>Indicates that you do not want to have a limit on the number of instances to include in the Power report</td>
</tr>
</tbody>
</table>

**-min_power {number}**
Specifies which block to expand based on the minimum power value of a block.

```
-max_instance {integer >= 0}
```

Sets the maximum number of instances to a specified integer greater than or equal to 0 (zero). This will limit the maximum number of instances to be included in the Power report.

```
-activity_sortorder {value}
```

Specifies the sort order for the activity summary. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ascending</td>
<td>Sorts the values in ascending order</td>
</tr>
<tr>
<td>descending</td>
<td>Sorts the values in descending order</td>
</tr>
</tbody>
</table>

```
-activity_sortby {value}
```

Specifies how to sort the values for the activity summary. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>pin name</td>
<td>Sorts based on the pin name</td>
</tr>
<tr>
<td>net name</td>
<td>Sorts based on the net name</td>
</tr>
<tr>
<td>domain</td>
<td>Sorts based on the clock domain</td>
</tr>
<tr>
<td>frequency</td>
<td>Sorts based on the clock frequency</td>
</tr>
<tr>
<td>source</td>
<td>Sorts based on the clock frequency source</td>
</tr>
</tbody>
</table>

```
-activity_summary {value}
```

Specifies whether to include the activity summary in the report. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>true</td>
<td>Includes the activity summary in the report</td>
</tr>
<tr>
<td>false</td>
<td>Does not include the activity summary in the report</td>
</tr>
</tbody>
</table>

```
-frequency_threshold {value}
```

Specifies whether to add a frequency threshold. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>true</td>
<td>Adds a frequency threshold</td>
</tr>
<tr>
<td>false</td>
<td>Does not add a frequency threshold</td>
</tr>
</tbody>
</table>

```
-filter_pin {value}
```

Specifies whether to filter by maximum number of pins. The following table shows the acceptable values for this argument:
### Value Description

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>true</td>
<td>Filters by maximum number of pins</td>
</tr>
<tr>
<td>false</td>
<td>Does not filter by maximum number of pins</td>
</tr>
</tbody>
</table>

- **-min_frequency** `{value}`
  
  Sets the minimum frequency to `{decimal value [unit (Hz | KHz | MHz)]}`.

- **-max_pin** `{value}`
  
  Sets the maximum number of pins.

- **-enablerates_sortorder** `{value}`
  
  Specifies the sort order for the probabilities summary. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ascending</td>
<td>Sorts the values in ascending order</td>
</tr>
<tr>
<td>descending</td>
<td>Sorts the values in descending order</td>
</tr>
</tbody>
</table>

- **-enablerates_sortby** `{value}`
  
  Specifies how to sort the values for the probabilities summary. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>pin name</td>
<td>Sorts based on the pin name</td>
</tr>
<tr>
<td>net name</td>
<td>Sorts based on the net name</td>
</tr>
<tr>
<td>domain</td>
<td>Sorts based on the clock domain</td>
</tr>
<tr>
<td>frequency</td>
<td>Sorts based on the clock frequency</td>
</tr>
<tr>
<td>source</td>
<td>Sorts based on the clock frequency source</td>
</tr>
</tbody>
</table>

- **-enablerates_summary** `{value}`
  
  Specifies whether to include the probabilities summary in the report. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>true</td>
<td>Includes the activity summary in the report</td>
</tr>
<tr>
<td>false</td>
<td>Does not include the activity summary in the report</td>
</tr>
</tbody>
</table>

- **-with_annotation_coverage** `{value}`
  
  Specifies whether to include the annotation coverage summary in the report. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>true</td>
<td>Includes the annotation coverage summary in the report</td>
</tr>
</tbody>
</table>

Value | Description
--- | ---
false | Does not include the annotation coverage summary in the report

{filename}
Specifies the name of the report.

**Notes**
- The following arguments have been removed. Running the script will trigger a warning message: Warning: Invalid argument: -argname "argvalue" Ignored. Ignore the warning.
  - annotated_pins {value}
  - stat_pow {value}
  - dyn_pow {value}
- Flash*Freeze, Sleep, and Shutdown are available only for certain families and devices.
- Worst and Best are available only for certain families and devices.

**Examples**
This example generates a Power report named report.rpt.
```tcl
smartpower_report_power -powerunit "uW" -frequnit "MHz" -opcond "Typical" -opmode "Active" -toggle "TRUE" -rail_breakdown "TRUE" -battery_life "TRUE" -style "Text" -power_summary "TRUE" -activity_sortby "Source" text_report.txt
```

**smartpower_set_mode_for_analysis**
Tcl command; sets the mode for cycle-accurate power analysis.
```tcl
smartpower_set_mode_for_analysis -mode {value}
```

**Arguments**
- **-mode {value}**
  Specifies the mode for cycle-accurate power analysis.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Active</td>
<td>The operating mode is set to Active</td>
</tr>
<tr>
<td>Standby</td>
<td>The operating mode is set to Standby</td>
</tr>
<tr>
<td>Flash*Freeze</td>
<td>The operating mode is set to Flash*Freeze</td>
</tr>
</tbody>
</table>

**Examples**
The following example sets the mode for analysis to active:
```tcl
smartpower_set_mode_for_analysis -mode {active}
```

**See Also**
- [Tcl documentation conventions](#)
smartpower_set_mode_for_pdpr

This SmartPower Tcl command sets the operating mode used by the Power Driven Place and Route (PDPR) tool during power optimization.

smartpower_set_mode_for_pdpr -opmode {value}

Parameters

- **opmode** {value}
  Value must be a valid operating mode.
  This parameter is mandatory.
  Sets the operating mode for your power driven place and route.

Exceptions

None

Return Value

This command does not return a value.

Examples

This example sets the Active mode as the operating mode for Power Driven Place and Route.

```tcl
set_mode_for_pdpr -opmode "Active"
```

This example creates a custom mode and set it to be used by Power Driven Place and Route (PDPR).

```tcl
smartpower_add_new_custom_mode -name "MyCustomMode" 
  -description "for PDPR" -base_mode "Active"
smartpower_set_mode_for_pdpr -opmode "MyCustomMode"
```

See Also

Tcl Command Documentation Conventions

smartpower_set_operating_condition

Tcl command; sets the operating conditions used in SmartPower to one of the pre-defined types.

smartpower_set_operating_condition -opcond {value}

Arguments

- **opcond** {value}
  Specifies the value of the operating condition. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>best</td>
<td>Sets the operating conditions to best</td>
</tr>
<tr>
<td>typical</td>
<td>Sets the operating conditions to typical</td>
</tr>
<tr>
<td>worst</td>
<td>Sets the operating conditions to worst</td>
</tr>
</tbody>
</table>


Examples

This example sets the operating conditions to best:

```
smartpower_set_operating_condition -opcond {best}
```

See Also

Tcl documentation conventions

smartpower_set_operating_conditions

Tcl command: sets the operating conditions used in SmartPower.

```
smartpower_set_operating_conditions "still_air | 1.0_mps | 2.5_mps | custom" -heatsink "None | custom | 10mm_Low_Profile | 15mm_Medium_Profile | 20mm_High_Profile" -boardmodel "None_Conservative | JEDEC_2s2p" [-teta_ja "decimal value"] [-teta_sa "decimal value"]
```

Arguments

-still_air {value}

Specifies the value for the still air operating condition. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0_mps</td>
<td>Sets the operating conditions to best</td>
</tr>
<tr>
<td>2.5_mps</td>
<td>Sets the operating conditions to typical</td>
</tr>
<tr>
<td>custom</td>
<td>Sets the operating conditions to worst</td>
</tr>
</tbody>
</table>

-heatsink {value}

Specifies the value of the operating condition. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>none</td>
<td>No heat sink</td>
</tr>
<tr>
<td>custom</td>
<td>Sets a custom heat sink size</td>
</tr>
<tr>
<td>10mm_Low_Profile</td>
<td>10 mm heat sink</td>
</tr>
<tr>
<td>15mm_Low_Profile</td>
<td>15 mm heat sink</td>
</tr>
<tr>
<td>20mm_High_Profile</td>
<td>20 mm heat sink</td>
</tr>
</tbody>
</table>

-boardmodel {value}

Specifies your board model. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>None_Conservative</td>
<td>No board model, conservative routing</td>
</tr>
<tr>
<td>JEDEC_2s2p</td>
<td>JEDEC 2s2p board model</td>
</tr>
</tbody>
</table>

-teta_ja {decimal_value}

-
Optional; sets your teta ja value; must be a positive decimal
-teta_sa {decimal_value}
Optional; sets your teta sa value; must be a positive decimal.

Examples

This example sets the operating conditions to best:
set_operating_conditions -airflow "still_air" -heatsink "None" -boardmodel "None_Conservative"

See Also
Tcl documentation conventions

smartpower_set_process
Tcl command; sets the process used in SmartPower to one of the pre-defined types.

smartpower_set_process -process {value}

Arguments

-process {value}
Specifies the value of the operating condition. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Typical</td>
<td>Sets the process for SmartPower to typical</td>
</tr>
<tr>
<td>Maximum</td>
<td>Sets the process for SmartPower to maximum</td>
</tr>
</tbody>
</table>

Examples

This example sets the operating conditions to typical:
smartpower_set_process -process {Typical}

See Also
Tcl documentation conventions

smartpower_set_scenario_for_analysis
Tcl command; sets the scenario for cycle-accurate power analysis.

smartpower_set_scenario_for_analysis -scenario {value}

Arguments

-scenario {value}
Specifies the mode for cycle-accurate power analysis.

Examples

The following example sets the scenario for analysis to my_scenario:
smartpower_set_scenario_for_analysis -scenario {my_scenario}
See Also
Tcl documentation conventions

smartpower_set_temperature_opcond
Tcl command; sets the temperature in the operating conditions to one of the pre-defined types.

smartpower_set_temperature_opcond -use{value}

Arguments
- use{value}
  Specifies the temperature in the operating conditions. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>oprange</td>
<td>Sets the temperature in the operating conditions as specified in your Project Settings.</td>
</tr>
<tr>
<td>design</td>
<td>Sets the temperature in the operating conditions as specified in the SmartPower design-wide operating range. Applies to SmartPower only.</td>
</tr>
<tr>
<td>mode</td>
<td>Sets the temperature in the operating conditions as specified in the SmartPower mode-specific operating range. Applies to SmartPower only.</td>
</tr>
</tbody>
</table>

Examples
This example sets the temperature in the operating conditions as specified in the custom mode-settings:
smartpower_set_temperature_opcond -use{mode}

See Also
Tcl documentation conventions

smartpower_set_voltage_opcond
Tcl command; sets the voltage in the operating conditions.

smartpower_set_voltage_opcond -voltage{value} -use{value}

Arguments
- voltage{value}
  Specifies the voltage supply in the operating conditions. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>Sets the voltage operating conditions for VDD</td>
</tr>
<tr>
<td>VDD18</td>
<td>Sets the voltage operating conditions for VDD18</td>
</tr>
<tr>
<td>Value</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>--------------------------------------------------</td>
</tr>
<tr>
<td>VDDAUX</td>
<td>Sets the voltage operating conditions for VDDAUX</td>
</tr>
<tr>
<td>VDDI 1.1</td>
<td>Sets the voltage operating conditions for VDDI 1.1</td>
</tr>
<tr>
<td>VDDI 1.2</td>
<td>Sets the voltage operating conditions for VDDI 1.2</td>
</tr>
<tr>
<td>VDDI 1.35</td>
<td>Sets the voltage operating conditions for VDDI 1.35</td>
</tr>
<tr>
<td>VDDI 1.5</td>
<td>Sets the voltage operating conditions for VDDI 1.5</td>
</tr>
<tr>
<td>VDDI 1.8</td>
<td>Sets the voltage operating conditions for VDDI 1.8</td>
</tr>
<tr>
<td>VDDI 2.5</td>
<td>Sets the voltage operating conditions for VDDI 2.5</td>
</tr>
<tr>
<td>VDDI 3.3</td>
<td>Sets the voltage operating conditions for VDDI 3.3</td>
</tr>
<tr>
<td>VDD25</td>
<td>Sets the voltage operating conditions for VDD25</td>
</tr>
<tr>
<td>VDDA</td>
<td>Sets the voltage operating conditions for VDDA</td>
</tr>
<tr>
<td>VDDA25</td>
<td>Sets the voltage operating conditions for VDDA25</td>
</tr>
</tbody>
</table>

-`use(value)`

Specifies the voltage in the operating conditions for each voltage supply. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>oprange</td>
<td>Sets the voltage in the operating conditions as specified in your <a href="#">Project Settings</a>.</td>
</tr>
<tr>
<td>design</td>
<td>Sets the voltage in the operating conditions as specified in the SmartPower design-wide operating range. Applies to SmartPower only.</td>
</tr>
<tr>
<td>mode</td>
<td>Sets the voltage in the operating conditions as specified in the SmartPower mode-specific operating range. Applies to SmartPower only.</td>
</tr>
</tbody>
</table>

### Examples

This example sets the VCCA as specified in the SmartPower mode-specific settings:

```
smartpower_set_voltage_opcond -voltage{vcca} -use{mode}
```

### See Also

[Tcl documentation conventions](#)

[smartpower_temperature_opcond_set_design_wide](#)

Tcl command; sets the temperature for SmartPower design-wide operating conditions.
smartpower_temperature_opcond_set_design_wide -best{value} -typical{value} -worst{value} -thermal_mode{value}

Arguments

- **best{value}**
  Specifies the best temperature (in degrees Celsius) used for design-wide operating conditions.

- **typical{value}**
  Specifies the typical temperature (in degrees Celsius) used for design-wide operating conditions.

- **worst{value}**
  Specifies the worst temperature (in degrees Celsius) used for design-wide operating conditions.

- **thermal_mode{value}**
  Specifies the mode in which the junction temperature is computed. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ambient</td>
<td>The junction temperature will be iteratively computed with total static power</td>
</tr>
<tr>
<td>opcond</td>
<td>The junction temperature will be given as one of the operating condition range values specified in the device selection</td>
</tr>
</tbody>
</table>

Examples

This example sets the temperature for design-wide operating conditions to Best 20, Typical 30, and Worst 60:

```
smartpower_temperature_opcond_set_design_wide -best{20} -typical{30} -worst{60}
```

See Also

[Tcl documentation conventions](#)

smartpower_temperature_opcond_set_mode_specific

Tcl command; sets the temperature for SmartPower mode-specific operating conditions.

```
smartpower_temperature_opcond_set_mode_specific -opmode{value} -thermal_mode{value} -best{value} -typical{value} -worst{value} -thermal_mode{value}
```

Arguments

- **opmode {value}**
  Specifies the operating mode. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Active</td>
<td>The operating mode is set to Active</td>
</tr>
<tr>
<td>Static</td>
<td>The operating mode is set to Static</td>
</tr>
<tr>
<td>Flash*Freeze</td>
<td>The operating mode is set to Flash*Freeze</td>
</tr>
</tbody>
</table>

- **thermal_mode{value}**
Specifies the mode in which the junction temperature is computed. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ambient</td>
<td>The junction temperature will be iteratively computed with total static power</td>
</tr>
<tr>
<td>opcond</td>
<td>The junction temperature will be given as one of the operating condition range values specified in the device selection</td>
</tr>
</tbody>
</table>

- `best{value}`
  Specifies the best temperature (in degrees Celsius) for the selected mode.
- `typical{value}`
  Specifies the typical temperature (in degrees Celsius) for the selected mode.
- `worst{value}`
  Specifies the worst temperature (in degrees Celsius) for the selected mode.

**Examples**

This example sets the temperature for mode-specific operating conditions for mode1:

```
smartpower_temperature_opcond_set_mode_specific -mode{mode1} -best{20} -typical{30} -worst{60}
```

**See Also**

[Tcl documentation conventions](#)

**smartpower_voltage_opcond_set_design_wide**

Tcl command; sets the voltage settings for SmartPower design-wide operating conditions.

```
smartpower_voltage_opcond_set_design_wide -voltage{value} -best{value} -typical{value} -worst{value}
```

**Arguments**

- `voltage{value}`
  Specifies the voltage supply in the operating conditions. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>Sets the voltage operating conditions for VDD</td>
</tr>
<tr>
<td>VDDI 2.5</td>
<td>Sets the voltage operating conditions for VDDI 2.5</td>
</tr>
<tr>
<td>VPP</td>
<td>Sets the voltage operating conditions for VPP</td>
</tr>
<tr>
<td>VCCA</td>
<td>Sets the voltage operating conditions for VCCA</td>
</tr>
<tr>
<td>VCCI 3.3</td>
<td>Sets the voltage operating conditions for VCCI 3.3</td>
</tr>
<tr>
<td>VCCI 2.5</td>
<td>Sets the voltage operating conditions for VCCI 2.5</td>
</tr>
<tr>
<td>VCCI 1.8</td>
<td>Sets the voltage operating conditions for VCCI 1.8</td>
</tr>
</tbody>
</table>
## Value Description

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCCI 1.5</td>
<td>Sets the voltage operating conditions for VCCI 1.5</td>
</tr>
<tr>
<td>VCC33A</td>
<td>Sets the voltage operating conditions for VCC33A</td>
</tr>
<tr>
<td>VCCDA</td>
<td>Sets the voltage operating conditions for VCCDA</td>
</tr>
</tbody>
</table>

- **best**{value}
  Specifies the best voltage used for design-wide operating conditions.

- **typical**{value}
  Specifies the typical voltage used for design-wide operating conditions.

- **worst**{value}
  Specifies the worst voltage used for design-wide operating conditions.

### Examples

This example sets VCCA for design-wide to best 20, typical 30 and worst 40:

```tcl
smartpower_voltage_opcond_set_design_wide -voltage(VCCA) -best(20) -typical(30) -worst(40)
```

### See Also

- [Tcl documentation conventions](#)

### smartpower_voltage_opcond_set_mode_specific

Tcl command; sets the voltage settings for SmartPower mode-specific use operating conditions.

```tcl
smartpower_voltage_opcond_set_mode_specific -opmode{value} -voltage{value} -best{value} -typical{value} -worst{value}
```

### Arguments

- **opmode** {value}
  Use this option to specify the mode from which the operating conditions are extracted to generate the report.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Active</td>
<td>The operating mode is set to Active</td>
</tr>
<tr>
<td>Static</td>
<td>The operating mode is set to Static</td>
</tr>
<tr>
<td>Flash*Freeze</td>
<td>The operating mode is set to Flash*Freeze</td>
</tr>
</tbody>
</table>

- **voltage**{value}
  Specifies the voltage in the operating conditions. The following table shows the acceptable values for this argument:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>Sets the voltage operating conditions for VDD</td>
</tr>
</tbody>
</table>
### Value | Description
--- | ---
VDD18 | Sets the voltage operating conditions for VDD18
VDDAUX | Sets the voltage operating conditions for VDDAUX
VDDI 1.1 | Sets the voltage operating conditions for VDD 1.1
VDDI 1.2 | Sets the voltage operating conditions for VDDI 1.2
VDDI 1.35 | Sets the voltage operating conditions for VDDI 1.35
VDDI 1.5 | Sets the voltage operating conditions for VDDI 1.5
VDDI 1.8 | Sets the voltage operating conditions for VDDI 1.8
VDDI 2.5 | Sets the voltage operating conditions for VDDI 2.5
VDDI 3.3 | Sets the voltage operating conditions for VDDI 3.3
VDD25 | Sets the voltage operating conditions for VDD25
VDDA | Sets the voltage operating conditions for VDDA
VDDA25 | Sets the voltage operating conditions for VDDA25

- **-best(value)**
  Specifies the best voltage used for mode-specific operating conditions.
- **-typical(value)**
  Specifies the typical voltage used for mode-specific operating conditions.
- **-worst(value)**
  Specifies the worst voltage used for mode-specific operating conditions.

**Examples**

This example sets the voltage for the static mode and sets best to 20, typical to 30 and worst to 40:
```
smartpower_voltage_opcond_set_mode_specific -opmode{active} -voltage{VCCA} -best{20} -typical{30} -worst{40}
```

**See Also**

[Tcl documentation conventions](#)
Programming and Configuration Tcl Commands

configure_design_initialization_data

This Tcl command sets the parameter values needed for generating initialization data.

<table>
<thead>
<tr>
<th>configure_design_initialization_data</th>
</tr>
</thead>
<tbody>
<tr>
<td>-second_stage_start_address {&lt;valid_snvm_address&gt;}</td>
</tr>
<tr>
<td>-third_stage_start_address {&lt;valid_address_for_third_stage_memory_type&gt;}</td>
</tr>
<tr>
<td>-third_stage_memory_type {&lt;UPROM</td>
</tr>
<tr>
<td>-third_stage_spi_clock_divider {1</td>
</tr>
<tr>
<td>-init_timeout {&lt;int_between_1_and_128_seconds&gt;}</td>
</tr>
</tbody>
</table>

Arguments

- second_stage_start_address
  String parameter for the start address of the second stage initialization client.
  Specified as a 32-bit hexadecimal string.
  The first stage client is always placed in sNVM, so it must be a valid sNVM address aligned on a page boundary.
  There are 221 sNVM pages and each page is 256 bytes long, so the address will be between 0 and DC00.

Notes:

Although the actual size of each page is 256 bytes, only 252 bytes are available to the user.

The first stage initialization client is always added to SNVM at 0xDC00 (page 220). So the valid addresses for the second stage initialization client are 0x0 (page 0) to 0xDB00 (page 219).

- third_stage_start_address
  String parameter for the start address of the third stage initialization client.
  Specified as a 32-bit hexadecimal string, and must be one of the following:
  — valid sNVM address aligned on a page boundary
  — valid UPROM address aligned on a block boundary
  — valid SPIFLASH address

- third_stage_memory_type
  The memory where the third stage initialization client will be placed.
  The value can be UPROM, SNVM, or SPIFLASH_NONAUTH. The default is UPROM.
  This parameter determines the valid value for parameter ‘third_stage_start_address’.

- third_stage_spi_clock_divider
  The value can be 1, 2, 4, or 6. The default value is 1.

- init_timeout
  Timeout value in seconds. Initialization is aborted if it does not complete before timeout expires.
  The value can be between 1 and 128. The default value is 128.

Example

configure_design_initialization_data
- second_stage_start_address 200 \n- third_stage_start_address 400 \n
-third_stage_memory_type UPROM \ 
-third_stage_spi_clock_divider 4 \ 
-init_timeout 120

See Also

generate_design_initialization_data

configure_ram

This Tcl command uses the RAM configuration file to configure RAM.

```tcl
configure_ram
-cfg file <RAM configuration file>
```

Arguments

- `cfg_file file`
  `file` is a valid configuration file to configure RAM.

set_client (for RAM)

```tcl
set_client \ 
-logical_instance_name {} \ 
-content_type {MEMORY_FILE | INITIALIZE_WITH_ZERO} \ 
-memory_file_format {} \ 
-memory_file {} \ 
-content_type_changed {1}
```

Arguments

- `logical_instance_name`
  Hierarchical instance name of the logical RAM that the client will initialize.

- `content_type`
  The `content_type` can be MEMORY_FILE or INITIALIZE_WITH_ZERO.
  MEMORY_FILE – Client will be initialized with content from the memory file.
  INITIALIZE_WITH_ZERO – Client will be initialized with zeros.

- `memory_file_format` 
  For RAM blocks from PF_SRAM_AHBL_AXI core, the supported file format is “INTEL_HEX”. For all others, the supported file formats are “INTEL_HEX” and “MOTOROLA_S”.

- `memory_file`
  Path of the imported memory file. This can be absolute, or relative to the project.

- `content_type_changed {1}`
  If client information is modified by the user in Fabric RAMs, the value must be “1”.

Example

The following example shows the set_client Tcl command for RAM.

```tcl
set_client \ 
-logical_instance_name {TOP/SD1_0/dplsramcomp1_0} \ 
-content_type {MEMORY_FILE} \ 
-memory_file_format {} \ 
-memory_file 
{D:/local_z_folder/work/libero_projects/g5/mint_gfad_spi_done/ram_client_1.hex} \ 
-content_type_changed {1}
```
configure_snvm

Tcl command; configures sNVM from the specified configuration file.

```
configure_snvm -cfg_file  file
```

Arguments

- `cfg_file file`
  `file` is a valid configuration file to configure sNVM.

See Also

Configure sNVM

Sample sNVM Configuration File

```
set_plain_text_client \
-client_name {pt_A} \
-number_of_bytes 64 \
-content_type {MEMORY_FILE} \
-content_file_format {Microsemi-Binary 8/16/32 bit} \
-content_file {C:/local_z_folder/work/memory files/binary8X16.mem} \
-start_page 0 \
-use_for_simulation 0 \
-reprogram 1 \
-use_as_rom 0

set_plain_text_client \
-client_name {pt_client} \
-number_of_bytes 64 \
-content_type {MEMORY_FILE} \
-content_file_format {Microsemi-Binary 8/16/32 bit} \
-content_file {C:/local_z_folder/work/memory files/binary32X16.mem} \
-start_page 2 \
-use_for_simulation 0 \
-reprogram 1 \
-use_as_rom 0

set_plain_text_client \
-client_name {pt_client_16bit} \
-number_of_bytes 32 \
-content_type {MEMORY_FILE} \
-content_file_format {Microsemi-Binary 8/16/32 bit} \
-content_file {C:/local_z_folder/work/memory files/binary16X16.mem} \
-start_page 1 \
-use_for_simulation 0 \
-reprogram 1 \
-use_as_rom 0

set_plain_text_client \
-client_name {INIT_STAGE_1_SNVM_CLIENT} \
-number_of_bytes 504 \
-content_type {MEMORY_FILE} \
-content_file_format {Microsemi-Binary 8/16/32 bit} \
-content_file {designer\top\top_init_stage_1_snvm.mem} \
-start_page 219 \
```
configure_spiflash

This Tcl command configures SPI Flash Memory from the specified SPI Flash Memory configuration file.

```
configure_spiflash -cfg_file file
```

**Arguments**

```
-cfg_file file
```

Specify a valid configuration file to configure SPI Flash.

*file* is the SPI Flash Memory configuration file. *file* can be an absolute path to the SPI Flash Memory configuration file or it can be a path relative to a Tcl file that includes the command. After running this command, the new configuration is saved as a project spiflash.cfg file.

**See Also**

Configure SPI Flash

**Sample SPI Flash Configuration File**

```
set_auto_update_mode {0}
set_manufacturer {Macronix}
set_client \n  -client_name {vzcx} \n  -client_type {FILE_SPI} \n  -content_type {MEMORY_FILE} \n  -content_file {..\..\..\..\..\..\memory files\spi_bitstream.spi} \n  -start_address {2561} \n  -client_size {388} \n  -program {1}

set_client \n  -client_name {golden} \n  -client_type {FILE_SPI_GOLDEN} \n  -content_type {MEMORY_FILE} \
```
-content_file {C:\local_z_folder\work\memory files\spi_bitstream.spi} \ 
-start_address {1042} \ 
-client_size {389} \ 
-program {1}

set_client \ 
-client_name {INIT_STAGE_3_SPI_CLIENT} \ 
-client_type {INIT} \ 
-content_type {MEMORY_FILE} \ 
-content_file {C:\local_z_folder\work\libero_projects\g5\SNVM_TEST_top_uic.bin} \ 
-start_address {4096} \ 
-client_size {4124} \ 
-program {1}

SPM_OTP

Configures the parameters for SPM_OTP.

| configure_tool | -name SPM_OTP | [-params permanently_disable_debugging 0 | 1] | [-params permanently_disable_dpk 0 | 1] | [-params permanently_disable_factory_access 0 | 1] | [-params permanently_disable_prog_interfaces 0 | 1] | [-params permanently_disable_upk1 0 | 1] | [-params permanently_disable_upk2 0 | 1] | [-params permanently_write_protect_fabric 0 | 1] |

The following tables list the parameter names and values.

**configure_tool --name {SPM_OTP} parameter:value pair**

<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>permanently_disable_debugging</td>
<td>bool</td>
<td>false</td>
<td>true</td>
</tr>
<tr>
<td>permanently_disable_dpk</td>
<td>bool</td>
<td>false</td>
<td>true</td>
</tr>
<tr>
<td>permanently_disable_factory_access</td>
<td>bool</td>
<td>false</td>
<td>true</td>
</tr>
<tr>
<td>permanently_disable_prog_interfaces</td>
<td>bool</td>
<td>false</td>
<td>true</td>
</tr>
<tr>
<td>Name</td>
<td>Type</td>
<td>Value</td>
<td>Description</td>
</tr>
<tr>
<td>----------------------------------</td>
<td>---------</td>
<td>----------------------</td>
<td>---------------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>permanently_disable_upk1</td>
<td>bool</td>
<td>false</td>
<td>true</td>
</tr>
<tr>
<td>permanently_disable_upk2</td>
<td>bool</td>
<td>false</td>
<td>true</td>
</tr>
<tr>
<td>permanently_write_protect_fabric</td>
<td>bool</td>
<td>false</td>
<td>true</td>
</tr>
</tbody>
</table>

**Examples**

The following example specifies that SPM_OTP tool is configured to permanently disable user keys UPK1 and UPK2.

```
configure_tool \
  -name {SPM_OTP} \
  -params {permanently_disable_debugging:false} \
  -params {permanently_disable_dpdk:false} \
  -params {permanently_disable_factory_access:false} \
  -params {permanently_disable_prog_interfaces:false} \
  -params {permanently_disable_upk1:true} \
  -params {permanently_disable_upk2:true} \
  -params {permanently_write_protect_fabric:false}
```

The following example specifies that SPM_OTP tool is configured to permanently disable programming interfaces.

```
configure_tool \
  -name {SPM_OTP} \
  -params {permanently_disable_debugging:false} \
  -params {permanently_disable_dpdk:false} \
  -params {permanently_disable_factory_access:false} \
  -params {permanently_disable_prog_interfaces:true} \
  -params {permanently_disable_upk1:false} \
  -params {permanently_disable_upk2:false} \
  -params {permanently_write_protect_fabric:false}
```

**See Also**

remove_permanent_locks
configure_uprom

Tcl command; configures uPROM from the specified configuration file.

configure_uprom -cfg_file file

Arguments

- **cfg_file file**
  
  file is a valid configuration file to configure uPROM.

See Also

Configure uPROM

Sample uPROM Configuration File

```bash
set_data_storage_client \
  -client_name {client1_from_elsewhere} \
  -number_of_words 37 \
  -use_for_simulation {0} \
  -content_type {MEMORY_FILE} \
  -memory_file_format {Microsemi-Binary} \
  -memory_file {C:/local_z_folder/work/memory files/sar_86586_uprom.mem} \
  -base_address 1500
set_data_storage_client \
  -client_name {large_1} \
  -number_of_words 100 \
  -use_for_simulation {0} \
  -content_type {STATIC_FILL} \
  -base_address 5000
```

export_spiflash_image

This Tcl command exports a SPI Flash image file to a specified directory.

export_spiflash_image -file_name {name of file} -export_dir {absolute path to folder location}

Arguments

- **file_name name of file**
  
  The name of the image file.

- **export_dir absolute path to folder location**
  
  Folder/directory location.

See Also

Export Flash Image

generate_design_initialization_data

This Tcl command creates the memory files on disk, adds the initialization clients to the target memories, and writes the configuration files to disk.
This command also runs validation on the saved configuration files and writes out errors (if any) in the log. This command causes the UI of the Configure Design Initialization Data and Memories tool to refresh and show the latest configuration and validation errors (if any) in the tables.

This command takes no parameters.

```
generate_design_initialization_data
```
Example

generate_initialization_mem_files \
  -second_stage_start_address 200 \
  -third_stage_start_address 400 \
  -third_stage_memory_type UPROM \
  -third_stage_spi_clock_divider 6 \
  -init_timeout 120 \
  -custom_cfg_file {D:\test\my.txt}  

See Also

Design and Memory Initialization

remove_permanent_locks

Removes all the locks configured in SPM_OTP. This command can only be used when at least one lock is disabled using SPM_OTP.

Example

remove_permanent_locks

See Also

SPM_OTP

select_programmer

This Tcl command enables the specified programmer and disables all other connected programmers. This command is useful when multiple programmers are connected.

select_programmer -programmer_id {programmer_id} -host_name {host_name} -host_port {host_port}

Arguments

-programmer_id <programmer_id>
The programmer to be enabled. See Select Programmer.
-host_name <host_name>
The host name or IP address. This argument is required for a remote programmer and optional for a local programmer. For local programmer, if specified it must be "localhost".
-host_port <host_port>
This argument is required for a remote programmer and optional for a local programmer. If omitted, the default port is used (currently, the default is 80).

For a local host, both "localhost" and its port should be specified or omitted.

Note: The def variable "LOCAL_PROGRAM_DEBUG_SERVER_PORT" is used to set a different default local host port.

Examples

select_programmer -programmer_id (00557)
select_programmer -programmer_id (00557) \
  -host_name {localhost} \
  -host_port {80}
See Also

Select Programmer

**set_auto_update_mode**

This command enables or disables auto update.

```
set_auto_update_mode {0|1}
```

If `set_auto_update_mode` is 0, auto update is disabled. If `set_auto_update_mode` is 1, auto update is enabled.

**set_cipher_text_auth_client**

This Tcl command is added to the sNVM .cfg file that is given as the parameter to the configure_snvm command. Cipher-text Authenticated clients have 236 bytes available for user data in each page of sNVM.

```
set_cipher_text_auth_client
- client_name {<name>}
- number_of_bytes <number>
- content_type {MEMORY_FILE | STATIC_FILL}
- content_file_format {Microsemi-Binary 8/16/32 bit}
- content_file {<path>}
- start_page <number>
- use_for_simulation 0
- reprogram 0 | 1
- use_as_rom 0 | 1
```

**Arguments**

- **client_name**
  The name of the client. Needs to start with an alphabetic letter. Underscores and numerals are allowed at all positions other than the first.
- **number_of_bytes**
  The size of the client specified in bytes.
- **content_type**
  Source of data for the client. This can either be a memory file, or all zeros. Allowed values are MEMORY_FILE or STATIC_FILL
- **content_file_format**
  Only 'Microsemi-Binary 8/16/32 bit' is supported at this time.
- **content_file**
  Path of the memory file. This can be absolute, or relative to the project.
- **start_page**
  The page number in sNVM where data for this client will be placed.
- **use_for_simulation**
  Only value 0 is allowed.
- **reprogram**
  Boolean field; specifies whether the client will be programmed into the final design or not. Possible values are 0 or 1.
- **use_as_rom**
  Boolean field; specifies whether the client will allow only reads, or both read and writes. Possible values are 0 or 1.
Example

```tcl
set_cipher_text_auth_client \
-client_name {c} \ 
-number_of_bytes 12 \ 
-content_type {MEMORY_FILE} \ 
-content_file_format {Microsemi-Binary 8/16/32 bit} \ 
-content_file {D:/local_z_folder/work/memory_files/binary8x12.mem} \ 
-start_page 3 \ 
-use_for_simulation 0 \ 
-reprogram 1 \\
```

See Also

- `set_plain_text_client`
- `set_plain_text_auth_client`
- `set_usk_client`

set_client

This Tcl command specifies the client that will be added to SPI Flash Memory. This command is added to the SPI Flash Memory configuration file that is given as the parameter to the `configure_spiflash` command.

```tcl
set_client \ 
-client_name {} \ 
-client_type {FILE_SPI | FILE_SPI_GOLDEN | FILE_SPI_UPDATE | FILE_DATA_STORAGE_INTELHEX} \ 
-content_type {MEMORY_FILE | STATIC_FILL} \ 
-content_file {} \ 
-start_address {} \ 
-client_size {} \ 
-program {0|1}
```

Arguments

- `client_name`

The name of the client. Maximum of 32 characters, letters or numbers or "." or ".".

- `client_type`

The `-client_type` can be `FILE_SPI`, `FILE_SPI_GOLDEN`, `FILE_SPI_UPDATE` or `FILE_DATA_STORAGE_INTELHEX`.

- `content_type`

The `-content_type` can be `MEMORY_FILE` or `STATIC_FILL`.

- `content_file`

Absolute or relative path to the content memory file.

- `start_address`

The client start address. Note that some space is reserved for the SPI Flash Memory directory. Note: This is a decimal value of bytes.

- `client_size`

Client's size in bytes. If a content file is specified, the size must be equal to or larger than the file size. Note: this is a decimal value.
PolarFire FPGA Tcl Commands Reference Guide

Examples

The following examples show the `set_client` Tcl command for SPI Flash.

Absolute path

```
set_client
    -client_name {golden} \
    -client_type {FILE_SPI_GOLDEN} \n    -content_type {MEMORY_FILE} \n    -content_file {E:\top_design_ver_1.spi} \n    -start_address {1024} \n    -client_size {9508587} \n    -program {1}
```

```
set_client
    -client_name {ds} \
    -client_type {FILE_DATA_STORAGE_INTELHEX} \n    -content_type {MEMORY_FILE} \n    -content_file {E:\intel_hex.hex} \n    -start_address {9509611} \n    -client_size {128} \n    -program {1}
```

Relative path

```
set_client
    -client_name {golden} \
    -client_type {FILE_SPI_GOLDEN} \n    -content_type {MEMORY_FILE} \n    -content_file {\..\..\..\top_design_ver_1.spi} \n    -start_address {1024} \n    -client_size {9508587} \n    -program {1}
```

```
set_client
    -client_name {ds} \
    -client_type {FILE_DATA_STORAGE_INTELHEX} \n    -content_type {MEMORY_FILE} \n    -content_file {\..\..\..\intel_hex.hex} \n    -start_address {9509611} \n    -client_size {128} \n    -program {1}
```

**set_data_storage_client**

This Tcl command is added to the `.cfg` file, which will then be given as the parameter to the `configure_uprom` command.

```
set_data_storage_client
    -client_name {<name>} \
    -number_of_words {<number>} \
    -content_type {MEMORY_FILE | STATIC_FILL} \
    -memory_file_format {Microsemi-Binary} \
    -memory_file {<path>} \
    -base_address {<hexadecimal_string>} \
    -use_for_simulation {0} \
```

Arguments

- `-client_name`
  The name of the client. Must start with an alphabetic letter. Underscores and numerals are allowed at all positions other than the first.

- `-number_of_bytes`
The size of the client specified in number of words.

- **content_type**
  Source of data for the client. This can either be a memory file, or all zeros. Allowed values are
  MEMORY_FILE or STATIC_FILL.
  MEMORY_FILE – content memory file must be specified
  STATIC_FILL – client memory will be filled with 1s, no content memory file

- **memory_file_format**
  Only ‘Microsemi-Binary’ is supported at this time.

- **content_file**
  Path of the memory file. This can be absolute, or relative to the project.

- **base_address**
  Hexadecimal address where the first byte of user data will be placed.

- **use_for_simulation**
  Only value 0 is allowed.

**Example**

```tcl
set_data_storage_client \
  -client_name {client1_from_elsewhere_new_MMMMMMM} \ 
  -number_of_words 57 \ 
  -use_for_simulation {0} \ 
  -content_type {MEMORY_FILE} \ 
  -memory_file_format {Microsemi-Binary} \ 
  -memory_file {D:/local_z_folder/work/memory_files/sar_86586_uprom.mem} \ 
  -base_address 0
```

**set_manufacturer**

This command specifies the manufacturer for the SPI Flash device.

```tcl
set_manufacturer {MICRON | SPANSION | Macronix | Winbond }
```

The value for the `set_manufacturer` command must be one of the following:

- MICRON
- SPANSION
- Macronix
- Winbond

See the following table for details about the supported SPI Flash devices.

<table>
<thead>
<tr>
<th>Mfg Part Number</th>
<th>Memory Capacity</th>
<th>Manufacturer</th>
<th>Sector Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>MT25QL01GBBB8ESF-0SIT</td>
<td>1 GB</td>
<td>MICRON</td>
<td>4 KB</td>
</tr>
<tr>
<td>S25FL512SAGMF011</td>
<td>512 MB</td>
<td>SPANSION</td>
<td>256 KB</td>
</tr>
<tr>
<td>MX66L51235FMI-10G</td>
<td>512 MB</td>
<td>Macronix</td>
<td>4 KB</td>
</tr>
<tr>
<td>W25Q256FVFIG</td>
<td>256 MB</td>
<td>Winbond</td>
<td>4 KB</td>
</tr>
</tbody>
</table>

Note: Microsemi currently supports only the devices listed above.

**Note:** This version of the programmer does not support SPI Flash security. Device security options such as "Hardware Write Protect" should be disabled for the External SPI Flash device.
set_plain_text_auth_client

This Tcl command is added to the sNVM.cfg file that is given as the parameter to the configure_snvm command. Plain-text Authenticated clients have 236 bytes available for user data in each page of sNVM.

Arguments

- **client_name**
The name of the client. Needs to start with an alphabetic letter. Underscores and numerals are allowed at all positions other than the first.

- **number_of_bytes**
The size of the client specified in bytes.

- **content_type**
Source of data for the client. This can either be a memory file, or all zeros. Allowed values are MEMORY_FILE or STATIC_FILL

- **content_file_format**
Only ‘Microsemi-Binary 8/16/32 bit’ is supported at this time.

- **content_file**
Path of the memory file. This can be absolute, or relative to the project.

- **start_page**
The page number in sNVM where data for this client will be placed.

- **use_for_simulation**
Only value 0 is allowed.

- **reprogram**
Boolean field; specifies whether the client will be programmed into the final design or not. Possible values are 0 or 1.

- **use_as_rom**
Boolean field; specifies whether the client will allow only reads, or both read and writes. Possible values are 0 or 1.

Example

```
set_plain_text_auth_client \    
-client_name {b} \    
-number_of_bytes 12 \    
-content_type {MEMORY_FILE} \    
-content_file_format {Microsemi-Binary 8/16/32 bit} \    
-content_file {D:/local_z_folder/work/memory_files/binary8x12.mem} \    
-start_page 2 \
```
set_plain_text_client

This Tcl command is added to the sNVM .cfg file that is given as the parameter to the configure_snvm command.

Plain-text Non-Authenticated clients have 252 bytes available for user data in each page of sNVM.

Arguments

- **client_name**
  The name of the client. Needs to start with an alphabetic letter. Underscores and numerals are allowed at all positions other than the first.

- **number_of_bytes**
  The size of the client specified in bytes.

- **content_type**
  Source of data for the client. This can either be a memory file, or all zeros. Allowed values are MEMORY_FILE or STATIC_FILL

- **content_file_format**
  Only 'Microsemi-Binary 8/16/32 bit' is supported at this time.

- **content_file**
  Path of the memory file. This can be absolute, or relative to the project.

- **start_page**
  The page number in sNVM where data for this client will be placed.

- **use_for_simulation**
  Only value 0 is allowed.

- **reprogram**
  Boolean field; specifies whether the client will be programmed into the final design or not. Possible values are 0 or 1.

- **use_as_rom**
  Boolean field; specifies whether the client will allow only reads, or both read and writes. Possible values are 0 or 1.

Example

```
set_plain_text_client  
-client_name {a}  
-number_of_bytes 12  
-use_for_simulation 0  
-reprogram 1  
-use_as_rom 0
```
See Also

set_plain_text_auth_client
set_cipher_text_auth_client
set_usk_client

set_programming_interface

This Tcl command sets the programming interface.

```
set_programming_interface -interface {JTAG | SPI_SLAVE}
```

Arguments

```
set_programming_interface -interface {JTAG | SPI_SLAVE}
```
Specify the programming interface as JTAG or SPI_SLAVE. The default is JTAG.

See Also

Programming Connectivity and Interface

set_usk_client

This Tcl command is added to the sNVM .cfg file that is given as the parameter to the configure_snvm command. The USK client is required if sNVM has one or more clients of type ‘Authenticated’.

```
set_cipher_text_auth_client
- -start_page <number>
- -key <Hexadecimal string of size 24>
- -use_for_simulation 0 | 1
- -reprogram 0 | 1
```

Arguments

- start_page
  The page number in sNVM where data for this client will be placed.
- key
  A string of 24 hexadecimal characters.
- use_for_simulation
  Boolean field specifies whether the client will be used for simulation or not. Possible values are 0 or 1.
- reprogram
  Boolean field; specifies whether the client will be programmed into the final design or not. Possible values are 0 or 1.

Example

```
set_usk_client
- -start_page 4
- -key {D8C8831F3A2F72EDC569503F}
- -use_for_simulation 0
- -reprogram 1
```
See Also
set_plain_text_client
set_plain_text_auth_client
set_cipher_text_auth_client
# FlashPro Express Tcl Commands

## close_project

Closes the FlashPro Express project.

### Arguments

None

### Exceptions

None

### Example

```
close_project
```

## configure_flashpro3_prd

Changes FlashPro3 programmer settings.

### Arguments

- `vpump {ON|OFF}`
  
  Enables FlashPro programmer to drive VPUMP. Set to ON to drive VPUMP.

- `clk_mode {discrete_clk|free_running_clk}`

  Specifies free running or discrete TCK.

- `force_freq {ON|OFF}`

  Forces the FlashPro software to use the TCK frequency specified by the software rather than the TCK frequency specified in the programmer file.

- `freq {freq}`

  Specifies the TCK frequency in MHz.

### Exceptions

None

### Example

The following example sets the VPUMP option to ON, TCK to free running, and uses the TCK frequency specified in the programmer file (`force_freq` is set to OFF):

```
configure_flashpro3_prd -vpump {ON} -clk_mode {free_running_clk} -force_freq {OFF} -freq {4}
```

The following example sets VPUMP to ON, TCK to discrete, forces the FlashPro software to use the TCK frequency specified in the software (`-force_freq` is set to ON) at a frequency of 2 MHz:

```
configure_flashpro3_prd -vpump {ON} -clk_mode {discrete_clk} -force_freq {ON} -freq {2}
```
configure_flashpro4_prg

Changes FlashPro4 programmer settings.

```tcl
configure_flashpro4_prg [-vpump {ON|OFF}] [-clk_mode {discrete_clk|free_running_clk}] [-force_freq {ON|OFF}] [-freq {freq}]
```

**Arguments**

- **-vpump {ON|OFF}**
  Enables FlashPro4 programmer to drive VPUMP. Set to ON to drive VPUMP.
- **-clk_mode {discrete_clk|free_running_clk}**
  Specifies free running or discrete TCK.
- **-force_freq {ON|OFF}**
  Forces the FlashPro software to use the TCK frequency specified by the software rather than the TCK frequency specified in the programmer file.
- **-freq {freq}**
  Specifies the TCK frequency in MHz.

**Exceptions**

None

**Example**

The following example sets the VPUMP option to ON and uses a free running TCK at a frequency of 4 MHz (force_freq is set to OFF).

```tcl
configure_flashpro4_prg -vpump {ON} -clk_mode {free_running_clk} -force_freq {OFF} -freq {4}
```

The following example sets the VPUMP option to ON, uses a discrete TCK and sets force_freq to ON at 2 MHz.

```tcl
configure_flashpro4_prg -vpump {ON} -clk_mode {discrete_clk} -force_freq {ON} -freq {2}
```

configure_flashpro5_prg

Tcl command; changes FlashPro5 programmer settings.

```tcl
configure_flashpro5_prg [-vpump {ON|OFF}] [-clk_mode {free_running_clk}] [-programming_method {jtag | spi_slave}] [-force_freq {ON|OFF}] [-freq {freq}]
```

**Arguments**

- **-vpump {ON|OFF}**
  Enables FlashPro5 programmer to drive VPUMP. Set to ON to drive VPUMP. Default is ON.
- **-clk_mode {free_running_clk}**
  Specifies free running TCK. Default is free_running_clk.
- **-programming_method {jtag | spi_slave}**
  Specifies the programming method to use. Default is jtag.
  **Note:** spi_slave works only with SmartFusion2 and IGLOO2.
- **-force_freq {ON|OFF}**
  Forces the FlashPro software to use the TCK frequency specified by the software rather than the TCK frequency specified in the programmer file. Default is OFF.
- **-freq {freq}**
  Specifies the TCK frequency in MHz. Default is 4.
Exceptions
None

Example
The following example sets the VPUMP option to ON and uses a free running TCK at a frequency of 4 MHz (force_freq is set to OFF).

```tcl
configure_flashpro5_prg -vpump {ON} -clk_mode {free_running_clk} -force_freq {OFF} -freq {4}
```

The following example sets the VPUMP option to ON, uses a free running TCK and sets force_freq to ON at 2 MHz.

```tcl
configure_flashpro5_prg -vpump {ON} -clk_mode {free_running_clk} -force_freq {ON} -freq {2}
```

create_job_project
Tcl command; creates a Flashpro Express job using the programming job exported from Libero.

```tcl
create_job_project -job_project_location location -job_file path -overwrite 0|1
```

Arguments
- `job_project_location location`: Specifies the location for your FlashPro Express job project.
- `job_file path`: Path to the Libero job file that is used as input to create the Flashpro Express job project.
- `overwrite 0|1`: Set value to 1 to overwrite your existing job project.

Exceptions
None

Example
The following example creates a job project named test.job in the \fpexpress directory. It does not overwrite the existing job project.

```tcl
create_job_project \n-job_project_location {D:\fpexpress} \n-job_file {D:\test\designer\test\export\test.job} -overwrite 0\n```

dump_tcl_support
Unloads the list of supported FlashPro Express Tcl commands.

```tcl
dump_tcl_support -file {file}
```

Arguments
- `file {file}`

Exceptions
None
Example

The following example dumps your Tcl commands into the file 'tcldump.tcl'
dump_tcl_support -file {tcldump.tcl}

open_project

Opens a FlashPro Express project.

open_project -project {project}

Arguments

- project {project}
  Specifies the location and name of the project you wish to open.

Exceptions

None

Example

Opens the ‘FPPrj1.pro’ project from the FPProject1 directory
open_project -project {./FPProject1/FPPrj1.pro}

ping_prg

Pings one or more programmers.

ping_prg (-name {name})*

Arguments

- name {name}
  Specifies the programmer to be pinged. Repeat this argument for multiple programmers.

Exceptions

None

Example

The following example pings the programmers 'FP300085' and 'FP30086'.
ping_prg -name {FP300085} -name {FP300086}

refresh_prg_list

Refreshes the programmer list. This is most often used to have FlashPro or FlashPro Express detect a programmer that you have just connected.

refresh_prg_list

Arguments

None
Exceptions
None

Example
refresh_prg_list

remove_prg
Removes the programmer from the programmer list.

    remove_prg (-name {name})*

Arguments

    -name {name}*

    Specifies the programmer to be removed. You can repeat this argument for multiple programmers.

Exceptions
None

Example
The following example removes the programmer '03178' from the programmer list:
remove_prg (name {03178})*

run_selected_actions
Runs the selected action on the specified programmer and returns the exit code from the action. If no programmer name is specified, the action is run on all connected programmers. Only one exit code is returned, so return code cannot be used when action is run on more than one programmer. A programming file must be loaded.

    run_selected_actions [(-name {name})]*

Arguments

    -name {name}

    Optional argument that specifies the programmer name. You can repeat this argument for multiple programmers.

Exceptions
None

Example
The following example runs the selected actionS on the programmers 'FP300085' and 'FP300086'.
run_selected_actions -name {FP300085} -name {FP300086}

Example using return code:
if {[catch {run_selected_actions} return_val]} {puts "Error running Action"} else {puts "exit code $return_val"}

Example returning exit code to the command line (returns exit 99 on script failure, otherwise returns exit code from selected action):
if {[catch {run_selected_actions} return_val]}{exit 99} else {exit $return_val}
save_log

Saves the log file.

save_log -file {file}

Arguments

-file {file}
Specifies the log filename.

Exceptions

None

Example

The following example saves the log file with the name 'my_logfile1.log':
save_log -file {my_logfile1.log}

save_project

Saves the FlashPro Express project.

save_project

Arguments

None

Exceptions

None

Example

save_project

scan_chain_prg

In single mode, this command runs scan chain on a programmer.
In chain mode, this command runs scan and check chain on a programmer if devices have been added in the grid.

scan_chain_prg [(-name {name})+]

Arguments

-name {name}
Specifies the programmer name.

Exceptions

None

Example

The following example runs scan chain on a single programmer (single mode) named '21428':
scan_chain_prg -name {21428}

self_test_prg
Runs Self-Test on a programmer.

Arguments
- name {name}
  Specifies the programmer name. You can repeat this argument for multiple programmers.

Exceptions
None

Example
The following examples runs the self test on the programmer '30175':
self_test_prg (-name 30175)*

set_prg_name
Changes the user name of a programmer.

Arguments
- name {name}
  Identifies the old programmer name.
- new_name {new_name}
  Specifies the new programmer name.

Exceptions
None

Example
The following example changes the name of the programmer 'FP300086' to 'FP3Prg2':
set_prg_name -name {FP300086} -new_name {FP3Prg2}

set_programming_action
Selects the action for a device. The device name parameter must be specified only in chain programming mode. A programming file must be loaded. The device must be a Microsemi device.

Arguments
- name {name}
  Specifies the device name.
- action {action}
  Specifies the action.
Exceptions

Must be a Microsemi device

Example

The following example sets the programming action in single programming mode:

```
set_programming_action -action {PROGRAM}
```

And in chain programming mode:

```
set_programming_action -name {MyDevice1} -action {ERASE}
```

set_programming_file

Sets the programming file for a device. Either the `file` or the `no_file` flag must be specified. A programming file must be loaded. The device must be a Microsemi device.

```
set_programming_file [-name {name}] [-file {file}] [-no_file { }]
```

Arguments

- `-name {name}`
  Specifies the device name. This argument must be specified only in chain programming mode.
- `-file {file}`
  Specifies the programming file.
- `-no_file`
  Specifies to unload the current programming file.

Exceptions

Must be a Microsemi device.

Examples

In single programming mode:

```
set_programming_file -file {e:/design/pdb/TopA3P250.pdb}
```

In chain programming mode:

```
set_programming_file -name {MyDevice2} -file {e:/design/pdb/TopA3P250.pdb}
set_programming_file -name {MyDevice1} -no_file
SmartDebug Tcl Commands

SmartDebug Tcl Support

The following table lists the Tcl commands related to SmartDebug for PolarFire. Click the command to view more information.

<table>
<thead>
<tr>
<th>Command</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Probe</strong></td>
<td></td>
</tr>
<tr>
<td><code>add_probe_insertion_point</code></td>
<td>Adds probe points to be connected to user-specified I/Os for probe insertion flow.</td>
</tr>
<tr>
<td><code>add_to_probe_group</code></td>
<td>Adds the specified probe points to the specified probe group</td>
</tr>
<tr>
<td><code>create_probe_group</code></td>
<td>Creates a new probe group</td>
</tr>
<tr>
<td><code>delete_active_probe</code></td>
<td>Deletes either all or the selected active probes.</td>
</tr>
<tr>
<td><code>load_active_probe_list</code></td>
<td>Loads the list of probes from the file.</td>
</tr>
<tr>
<td><code>move_to_probe_group</code></td>
<td>Moves the specified probe points to the specified probe group</td>
</tr>
<tr>
<td><code>program_probe_insertion</code></td>
<td>Runs the probe insertion flow on the selected nets.</td>
</tr>
<tr>
<td><code>remove_probes</code></td>
<td>Deletes an added probe from the probe insertion UI.</td>
</tr>
<tr>
<td><code>set_live_probe</code></td>
<td>Set Live probe channels A and/or B to the specified probe point (or points).</td>
</tr>
<tr>
<td><code>select_active_probe</code></td>
<td>Manages the current selection of active probe points to be used by active probe READ operations.</td>
</tr>
<tr>
<td><code>read_active_probe</code></td>
<td>Reads active probe values from the device.</td>
</tr>
<tr>
<td><code>remove_from_probe_group</code></td>
<td>Move out the specified probe points from the group.</td>
</tr>
<tr>
<td><code>save_active_probe_list</code></td>
<td>Saves the list of active probes to a file.</td>
</tr>
<tr>
<td><code>select_active_probe</code></td>
<td>Manages the current selection of active probe points to be used by active probe READ operations.</td>
</tr>
<tr>
<td>Command</td>
<td>Action</td>
</tr>
<tr>
<td>-------------------------</td>
<td>------------------------------------------------------------------------</td>
</tr>
<tr>
<td><strong>Probes</strong></td>
<td></td>
</tr>
<tr>
<td><strong>ungroup</strong></td>
<td>Disassociates the probes as group.</td>
</tr>
<tr>
<td><strong>unset_live_probe</strong></td>
<td>Discontinues the debug function and clears live probe channels.</td>
</tr>
<tr>
<td><strong>write_active_probe</strong></td>
<td>Sets the target probe point on the device to the specified value.</td>
</tr>
<tr>
<td><strong>LSRAM</strong></td>
<td></td>
</tr>
<tr>
<td><strong>read_lsrarn</strong></td>
<td>Reads a specified block of large SRAM from the device.</td>
</tr>
<tr>
<td><strong>write_lsrarn</strong></td>
<td>Writes a seven bit word into the specified large SRAM location.</td>
</tr>
<tr>
<td><strong>uSRAM</strong></td>
<td></td>
</tr>
<tr>
<td><strong>read_usram</strong></td>
<td>Reads a uSRAM block from the device.</td>
</tr>
<tr>
<td><strong>write_usram</strong></td>
<td>Writes a seven bit word into the specified uSRAM location.</td>
</tr>
<tr>
<td><strong>Transceiver</strong></td>
<td></td>
</tr>
<tr>
<td><strong>loopback_mode</strong></td>
<td>Applies loopback to a specified lane.</td>
</tr>
<tr>
<td><strong>smartbert_test</strong></td>
<td>Starts and stops a Smart BERT test and resets error counter.</td>
</tr>
<tr>
<td><strong>static_pattern_transmit</strong></td>
<td>Starts and stops a Static Pattern Transmit.</td>
</tr>
<tr>
<td><strong>plot_eye</strong></td>
<td>Plots eye and exports eye plots.</td>
</tr>
<tr>
<td><strong>xcvr_read_register</strong></td>
<td>Reads SCB registers and their field values.</td>
</tr>
<tr>
<td><strong>xcvr_write_register</strong></td>
<td>Writes SCB registers and their field values.</td>
</tr>
<tr>
<td><strong>Additional Commands</strong></td>
<td></td>
</tr>
<tr>
<td><strong>event_counter</strong></td>
<td>Runs on signals that are assigned to channel A on the live probe, and displays the total events.</td>
</tr>
<tr>
<td><strong>export_smart_debu g_data</strong></td>
<td>Exports debug data for the SmartDebug application.</td>
</tr>
<tr>
<td><strong>fhp_control</strong></td>
<td>Provides FPGA Hardware Breakpoint (FHB) feature capability for SmartDebug.</td>
</tr>
<tr>
<td><strong>frequency_monitor</strong></td>
<td>Calculates the frequency of a signal that is assigned to live probe A.</td>
</tr>
<tr>
<td><strong>get_programmer_in fo</strong></td>
<td>Lists the IDs of all FlashPRO programmers connected to the machine.</td>
</tr>
<tr>
<td><strong>uprom_read_memory</strong></td>
<td>Reads uPROM memory block from the device.</td>
</tr>
</tbody>
</table>

**Standalone SmartDebug Commands**
<table>
<thead>
<tr>
<th>Command</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Probe</strong></td>
<td></td>
</tr>
<tr>
<td><code>construct_chain_automatically</code></td>
<td>Automatically starts chain construction for the specified programmer.</td>
</tr>
<tr>
<td><code>scan_chain_prd</code></td>
<td>In single mode, this Tcl command runs scan chain on a programmer. In chain mode, this Tcl command runs scan and check chain on a programmer if devices have been added in the grid.</td>
</tr>
<tr>
<td><code>enable_device</code></td>
<td>Enables or disables a device in the chain.</td>
</tr>
<tr>
<td><code>set_debug_programmer</code></td>
<td>Sets the debug programmer.</td>
</tr>
<tr>
<td><code>set_device_name</code></td>
<td>Sets the device name.</td>
</tr>
<tr>
<td><code>set_programming_file</code></td>
<td>Sets the programming file for a device.</td>
</tr>
<tr>
<td><code>set_programming_action</code></td>
<td>Selects the action for a device.</td>
</tr>
<tr>
<td><code>run_selected_actions</code></td>
<td>Runs the selected action for a device.</td>
</tr>
</tbody>
</table>

**add_probe_insertion_point**

This Tcl command adds probe points to be connected to user-specified I/Os for probe insertion flow.

```
add_probe_insertion_point -net net_name -driver driver -pin package_pin_name -port port name
```

**Arguments**

- `-net net_name`
  Name of the net used for probe insertion.
- `-driver driver`
  Driver of the net.
- `-pin package_pin_name`
  Package pin name (i.e. I/O to which the net will be routed during probe insertion).
- `-port port name`
  User-specified name for the probe insertion point.

**Example**

```
add_probe_insertion_point -net {count_out_c[0]} -driver {Counter_8bit_0_count_out[0]:Q} -pin {H5} -port {Probe_Insert0}
```

**add_to_probe_group**

Tcl command; adds the specified probe points to the specified probe group.
add_to_probe_group -name probe_name -group group_name

**Arguments**

- **-name probe_name**
  
  Specifies one or more probes to add.

- **-group group_name**
  
  Specifies name of the probe group.

**Example**

```
add_to_probe_group -name out[5]:out[5]:Q 
- name grp1.out[3]:out[3]:Q 
- name out.out[1].out[1]:Q 
- group my_new_grp
```

**construct_chain_automatically**

This Tcl command automatically starts chain construction for the specified programmer.

```
construct_chain_automatically -name {programmer_name}
```

**Arguments**

- **-name**
  
  Specify the device (programmer) name. This argument is mandatory.

**Example**

```
For a single programmer:

construct_chain_automatically -name {21428}
```

**See Also**

- `scan_chain_prg`
- `enable_device`
- `set_debug_programmer`
- `set_device_name`
- `set_programming_file`
- `set_programming_action`
- `run_selected_actions`

**create_probe_group**

Tcl command; creates a new probe group.

```
create_probe_group -name group_name
```

**Arguments**

- **-name group_name**
  
  Specifies the name of the new probe group.

PolarFire
Example

```tcl
create_probe_group -name my_new_grp
```

delete_active_probe

Tcl command; deletes either all or the selected active probes.

**Note:** You cannot delete an individual probe from the Probe Bus.

```tcl
delete_active_probe -all | -name probe_name
```

**Arguments**

- `-all`
  Deletes all active probe names.
- `-name probe_name`
  Deletes the selected probe names.

Example

```tcl
delete -all # deletes all active probe names
delete -name out[5]:out[5]:Q \
  -name my_grp1.out[1]:out[1]:Q  # deletes the selected probe names
delete -name my_grp1 \ 
  -name my_bus # deletes the group, bus and their members
```

enable_device

This Tcl command enables or disables a device in the chain. When the device is disabled, it is bypassed. The device must be a Microsemi device.

```tcl
enable_device -name {device_name} -enable {1 | 0}
```

**Arguments**

- `-name`
  Specify the device name. This argument is mandatory.
- `-enable`
  Specify the enable device. This argument is mandatory.

Example

```tcl
enable_device -name {MPF300 {T_ES|TS_ES}} -enable 1
```

**See Also**

- `construct_chain_automatically`
- `scan_chain_prg`
- `set_debug_programmer`
- `set_device_name`
- `set_programming_file`
- `set_programming_action`
- `run_selected_actions`
event_counter

The event_counter Tcl command runs on signals that are assigned to channel A on the live probe, and displays the total events. It can be run before or after setting the live probe signal to channel A. The user specifies the duration to run the event_counter command.

```
event_counter -run -stop -after duration_in_seconds
```

Arguments

- **run**
  Run event_counter.
- **stop**
  Stop event_counter.
- **after duration_in_seconds**
  Duration to stop event_counter. Specified by the user. This argument is required when `-stop` is specified.

Example

```
set_live_probe -probeA {count_out_c[0]:Counter_8bit_0_count_out[0]:Q} -probeB {}
event_counter -run
event_counter -stop -after 10
```

Output

```
Device ID Code = 2F8071CF
The 'read_id_code' command succeeded.
Live probes have been assigned.
Channel A: count_out_c[0]:Counter_8bit_0_count_out[0]:Q
Channel B: Not specified

The 'set_live_probe' command succeeded.

Event Counter = Activated
The 'event_counter' command succeeded.

Event Counter = Stopped
Total Events = 1603561
The 'event_counter' command succeeded.
The Execute Script command succeeded.
```

export_smart_debug_data

Tcl command; exports debug data for the SmartDebug application.

```
export_smart_debug_data [device_components] [bitstream_components] [-file_name {file}] [-export_dir {dir}] [-force_rtg4_otp 0 | 1]
```

The command corresponds to the Export SmartDebug Data tool in Libero. The command creates a file with the extension “ddc” that contains data based on selected options. This file is used by SmartDebug (standalone application) to create a new SmartDebug project, or it can be imported into a device in SmartDebug (standalone application).

- If you do not specify any design components, all components available in the design will be included by default except the bitstream components.
- The generate_bitstream parameter is required if you want to generate bitstream file and include it in the exported file.
  - You must specify the bitstream components you want to include in the generated bitstream file or all available components will be included.
If you choose to include bitstream, and the design has custom security, the custom security bitstream component must be included.

**Arguments**

*device_components*

The following device components can be selected. Specify "1" to include the component, and "0" if you do not want to include the component.

- probes <1|0>
- package_pins <1|0>
- memory_blocks <1|0>
- envm_data <1|0>
- security_data <1|0>
- chain <1|0>
- programmer_settings <1|0>
- ios_states <1|0>

*bitstream_components*

The following bitstream components can be selected. Specify "1" to include the component, and "0" if you do not want to include the component.

- generate_bitstream <1|0>
- bitstream_security <1|0>
- bitstream_fabric <1|0>
- bitstream_snvm <1|0>

- file_name *file*
  Name of exported file with extension "ddc".

- export_dir *dir*
  Location where DDC file will be exported. If omitted, design export folder will be used.

**Example**

The following examples shows the export_smart_debug_data command with all parameters.

```
export_smart_debug_data \
- file_name "Top" \
- export_dir "/" \
- probes 1 \
- package_pins 0 \
- memory_blocks 1 \
- security_data 1 \
- chain 1 \
- programmer_settings 1 \
- ios_states 1 \
- generate_bitstream 1 \
- bitstream_security 0 \
- bitstream_fabric 1 \
- bitstream_snvm 1
```

The following example shows the command with no parameters:

```
export_smart_debug_data
```

**fhb_control**

This Tcl command provides FPGA Hardware Breakpoint (FHB) feature capability for SmartDebug.

<table>
<thead>
<tr>
<th>Command</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>-halt</td>
<td>Halt the specified clock domain(s)</td>
</tr>
<tr>
<td>-run</td>
<td>Run the specified clock domain(s)</td>
</tr>
<tr>
<td>-step</td>
<td>Step the specified number of steps</td>
</tr>
<tr>
<td>-reset</td>
<td>Reset the specified clock domain(s)</td>
</tr>
<tr>
<td>-clock_domain</td>
<td>Specify the clock domain(s)</td>
</tr>
</tbody>
</table>
PolarFire FPGA Tcl Commands Reference Guide

- `arm_trigger -trigger_signal liveProbePoint -trigger_edge_select rising -delay value -clock_domain clkDomName(s)`
- `disarm_trigger -clock_domain clkDomName(s)/all`
- `capture_waveform number_of_steps -vcd_file target_file_name`
- `clock_domain_status -clock_domain clkDomName(s)/all`

Arguments

- **halt**
  Specifies to halt the clock.
  
  `-clock_domain clkDomName(s)/all`
  
  Specifies clock domain names to halt. Can be single or multiple clock domains, halted in order specified by user.

- **run**
  Specifies to run the clock.

  `-clock_domain clkDomName(s)`
  
  Specifies clock domain names to run. Can be single or multiple clock domains, releasing the user clock based on order specified.

- **step number_of_steps**
  Specifies to step the clock “number_of_steps” times. Minimum value is 1.

  `-clock_domain clkDomName(s)`
  
  Specifies clock domain names to step. Can be single or multiple clock domains.

- **reset**
  Specifies to reset FHB configuration for the specified clock domain.

  `-clock_domain clkDomName(s)`
  
  Specifies clock domain names to reset. Can be single or multiple clock domains.

- **arm_trigger**
  Specifies to arm FHB configuration for the specified clock domain.

  `-trigger_signal liveProbePoint`

  Set the trigger signal to arm the FHBs.

  `-trigger_edge_select rising`

  Specifies the trigger signal edge to arm the FHBs. FHBs will be armed on rising edge of trigger signal.

  `-delay value`

  `-clock_domain clkDomName(s)`

  Specifies clock domain names to be armed by the trigger signal. Can be single or multiple clock domains.

- **disarm_trigger**
  Specifies to disarm FHB configuration for the specified clock domain.

  `-clock_domain clkDomName(s)`

  Specifies clock domain names to be reset by the trigger signal. Can be single or multiple clock domains.

- **capture_waveform number_of_steps -vcd_file target_file_name**
  Specifies to capture waveform of all the added signals to active probes in the specified clock domain for number_of_steps.

  `-vcd_file target_file_name`

  Target file to save the data and see the waveform.

- **clock_domain_status -clock_domain clkDomName(s)/all**
  Specifies to read and display status of specified clock domain(s). Can be single or multiple clock domains.

Examples

```
fhb_control -halt -clock_domain {"FCCC_0/GL0_INST " "FCCC_0/GL1_INST" }
fhb_control -run -clock_domain {"FCCC_0/GL0_INST " "FCCC_0/GL1_INST" }
```
fhb_control -step -clock_domain {"FCCC_0/GL0_INST" "FCCC_0/GL1_INST" }
fhb_control -reset -clock_domain {"FCCC_0/GL0_INST" "FCCC_0/GL1_INST" }
fhb_control -arm_trigger -trigger_signal {q_0_c[14]:count_1_q[14]:Q}
  -trigger_edge_select {rising} -delay 0 -clock_domain {"FCCC_0/GL0_INST"}
fhb_control -disarm_trigger -trigger_signal {q_0_c[14]:count_1_q[14]:Q}
  -trigger_edge_select {rising} -delay 0 -clock_domain {"FCCC_0/GL0_INST"}
fhb_control -capture_waveform {10} -vcd_file {D:/wvf_location/waveform.vcd}
fhb_control -clock_domain_status -clock_domain {"FCCC_0/GL0_INST" "FCCC_0/GL1_INST" "FCCC_0/GL2_INST" }

frequency_monitor
The frequency_monitor Tcl command calculates the frequency of a signal that is assigned to live probe A.

run_frequency_monitor -signal signal_name -time duration

Arguments
- signal signal_name
  Specifies the signal name.
- time duration
  Specifies the duration to run the command. The value can be 0.1, 1, 5, 8, or 10.

Example
run_frequency_monitor -signal {count_out_c[7]:Counter_8bit_0_count_out[7]:Q} -time {5}

Output
Device ID Code = 2F8071CF
The 'read_id_code' command succeeded.
Frequency = 0.192716 MHz
The 'run_frequency_monitor' command succeeded.
The Execute Script command succeeded.

get_programmer_info
This Tcl command lists the IDs of all FlashPRO programmers connected to the machine.

get_programmer_info
This command takes no arguments.

Example
set a [get_programmer_info]

load_active_probe_list
Tcl command; loads the list of probes from the file.
load_active_probe_list -file file_path

Arguments
- file file_path
  The input file location.
Example

```
load_active_probe_list -file "/my_probes.txt"
```

**loopback_mode**

This Tcl command applies loopback to a specified lane.

```
loopback_mode -lane {Physical_Location} -apply -type {loopback_type}
```

**Arguments**

- `-lane {Physical_Location}`
  Specify the physical location of the lane.
- `-apply`
  Apply specified loopback to specified lane.
- `-type {loopback_type}`
  Specify the loopback type to apply.

**Examples**

```
loopback_mode -lane {Q3_LANE2} -apply -type {EQ-NearEnd}
loopback_mode -lane {Q3_LANE0} -apply -type {EQ-FarEnd}
loopback_mode -lane {Q0_LANE0} -apply -type {CDRFarEnd}
loopback_mode -lane {Q0_LANE1} -apply -type {NoLpbk}
loopback_mode -lane {Q1_LANE2} -apply -type {EQ-FarEnd}
loopback_mode -lane {Q1_LANE0} -apply -type {NoLpbk}
loopback_mode -lane {Q2_LANE2} -apply -type {EQ-FarEnd}
loopback_mode -lane {Q2_LANE3} -apply -type {CDRFarEnd}
```

**move_to_probe_group**

Tcl command; moves the specified probe points to the specified probe group.

**Note:** Probe points related to a bus cannot be moved to another group.

```
move_to_probe_group -name probe_name -group group_name
```

**Arguments**

- `-name probe_name`
  Specifies one or more probes to move.
- `-group group_name`
  Specifies name of the probe group.

**Example**

```
move_to_probe_group -name out[5]:out[5]:Q \
  -name grp1.out[3]:out[3]:Q \
  -group my_grp2
```

**optimize_dfe**

This Tcl command supports the Optimize DFE feature in SmartDebug.

```
optimize_dfe -dfe_algorithm <type of dfe algorithm> -lane <lane(s) configured in the design>
```
Arguments
-dfe_algorithm
This command executes Dfe Algorithm with type of dfe algorithm and lanes as input. Algorithm selection has two options:
software_based—executes DfeSs.tcl script
xcvr_based—executes internal Dfe Auto Calibration.
This argument is mandatory.
-lane
List of lane(s) configured in the design.
This argument is mandatory.

Examples
optimize_dfe -lane {"Q2_LANE0"}
-dfe_algorithm {software_based}
optimize_dfe -lane {"Q2_LANE0"}
-dfe_algorithm {xcvr_based}
optimize_dfe -lane {"Q2_LANE0" "Q0_LANE0"}
-dfe_algorithm {xcvr_based}

pcie_config_space
This Tcl command displays the value of the entered parameter in the SmartDebug log window and return the register:field value to the Tcl.

pcie_config_space -pcie_block_name {pcie_block_name} -param_name {param name}

Arguments
-pcie_block_name {pcie_block_name}
Complete logical hierarchy of the PCIE block whose status is to be read from the device. This parameter is mandatory.
-param_name {param name}
Parameter name to read from the device. This parameter is mandatory.

Example
pcie_config_space -pcie_block_name {sb_0/CM1_Subsystem/my_pcie_0} -param_name {neg_max_payload}

Output Display in SmartDebug window: 512 bytes
Return value to the tcl script: 0x2

pcie_ltssm_status
This Tcl command displays the current LTSSM state from the PLDA core in the SmartDebug log window and returns the register:field value to the Tcl.

pcie_ltssm_status -pcie_block_name {pcie_block_name}

Arguments
-pcie_block_name {pcie_block_name}
Complete logical hierarchy of the PCIE block whose status is to be read from the device. This parameter is mandatory.

Example
pcie_ltssm_status -pcie_block_name {sb_0/CM1_Subsystem/my_pcie_0}
polarFire FPGA Tcl Commands Reference Guide

Output Display in SmartDebug window: `Configuration.Linkwidth.start`
Return value to the tcl script: `0x2`

**plot_eye**

This Tcl command is used to plot eye and export eye plots.

```
plot eye -lane {lane_instance_name} -export_dir {location_path}
```

**Arguments**

- `-lane`
  Specify the lane instance name.
- `-export_dir`
  Specify the path to the location where the file is to be exported.

**Example**

```
plot_eye -lane {Q2_LANE0} - export_dir {E:\designs\G5\SERDES\ export.txt}
```

**program_probe_insertion**

This Tcl command runs the probe insertion flow on the selected nets.

```
program_probe_insertion
```

This command takes no arguments.

**read_active_probe**

Tcl command; reads active probe values from the device. The target probe points are selected by the `select_active_probe` command.

```
read_active_probe [-deviceName device_name] [-name probe_name] [-group_name bus_name | group_name] [-value_type b|h][-file file_path]
```

**Arguments**

- `-deviceName device_name`
  Parameter is optional if only one device is available in the current configuration.
- `-name probe_name`
  Instead of all probes, read only the probes specified. The probe name should be prefixed with bus or group name if the probe is in the bus or group.
- `-group_name bus_name | group_name`
  Instead of all probes, reads only the specified buses or groups specified here.
- `-value_type b|h`
  Optional parameter, used when the read value is stored into a variable as a string.
  - `b` = binary
  - `h` = hex
- `-file file_path`
  Optional. If specified, redirects output with probe point values read from the device to the specified file.

**Note:** When the user tries to read at least one signal from the bus/group, the complete bus or group is read. The user is presented with the latest value for all the signals in the bus/group.
**Example**

```tcl
read_active_probe -group_name {bus1}
read_active_probe -group_name {group1}
```

To save into variable:

```tcl
set a [read_active_probe -group_name {bus_name} -value_type h]  #save read data in hex string
```

If read values are stored into a variable without specifying value_type parameter, it saves values as a binary string by default.

**Example**

```tcl
set a [read_active_probe]  #sets variable a as binary string of read values after read_active_probe command.
```

### read_lsram

Tcl command; reads a specified block of large SRAM from the device.

#### Physical block

```tcl
read_lsram -name block_name -fileName file_name
```

**Arguments**

- `-name block_name`
  - Specifies the name for the target block.
- `-fileName file_name`
  - Optional; specifies the output file name for the data read from the device.

**Exceptions**

- Array must be programmed and active
- Security locks may disable this function

**Example**

Reads the LSRAM Block Fabric.Logic_0/U2/F_0_F0_U1/ramtmp_ramtmp_0_0/INST_RAM1K20_IP from the PolarFire device and writes it to the file output.txt.

```tcl
read_lsram -name {Fabric.Logic_0/U2/F_0_F0_U1/ramtmp_ramtmp_0_0/INST_RAM1K20_IP} -fileName {output.txt}
```

#### Logical block

```tcl
read_lsram -logicalBlockName block_name -port port_name
```

**Arguments**

- `-logicalBlockName block_name`
  - Specifies the name for the user defined memory block.
- `-port port_name`
  - Specifies the port for the memory block selected. Can be either Port A or Port B.

**Example**

```tcl
read_lsram -logicalBlockName {Fabric.Logic_0/U2/F_0_F0_U1} -port {Port A}
```

### read_usram

Tcl command; reads a uSRAM block from the device.
Physical block

```
read_usram [-name block_name] -fileName file_name
```

**Arguments**

- `-name block_name`
  Specifies the name for the target block.
- `-fileName file_name`
  Optional; specifies the output file name for the data read from the device.

**Exceptions**

- Array must be programmed and active
- Security locks may disable this function

**Example**

Reads the uSRAM Block Fabric.Logic_0/U3/F_0_F0_U1/ramtmp_ramtmp_0_0/INST_RAM64x12_IP from the PolarFire device and writes it to the file sram_block_output.txt.

```
read_usram -name {Fabric.Logic_0/U3/F_0_F0_U1/ramtmp_ramtmp_0_0/INST_RAM64x12_IP} -fileName (output.txt)
```

Logical block

```
read_usram -logicalBlockName block_name -port port_name
```

**Arguments**

- `-logicalBlockName block_name`
  Specifies the name of the user defined memory block.
- `-port port_name`
  Specifies the port of the memory block selected. Can be either Port A or Port B.

**Example**

```
read_usram -logicalBlockName {Fabric.Logic_0/U3/F_0_F0_U1} -port {Port A}
```

`remove_from_probe_group`

Tcl command; removes the specified probe points from the group. That is, the removed probe points won’t be associated with any probe group.

**Note:** Probes cannot be removed from the bus.

```
remove_from_probe_group -name probe_name
```

**Arguments**

- `-name probe_name`
  Specifies one or more probe points to remove from the probe group.

**Example**

The following command removes two probes from my_grp2.

```
Move_out_of_probe_group -name my_grp2.out[3]:out[3]:Q \n  -name my_grp2.out[3]:out[3]:Q
```
remove_probe_insertion_point

This Tcl command deletes an added probe from the probe insertion UI.

\[ \text{remove_probe_insertion_point -net net\_name -driver driver} \]

**Arguments**

- **-net net\_name**
  Name of the existing net which is added using the `add_probe_insertion_point` command.

- **-driver driver**
  Driver of the net.

**Example**

\[ \text{remove_probe_insertion_point -net \{count\_out\_c[0]\} -driver \{Counter\_8bit\_0\_count\_out[0]:Q\}} \]

run_selected_actions

This Tcl command is used to run the selected action for a device.

\[ \text{run_selected_actions} \]

This command takes no arguments.

**Example**

\[ \text{set\_programming\_action -name \{MPF300(T\_ES|TS\_ES)\} -action \{DEVICE\_INFO\}} \]
\[ \text{set\_programming\_action -name \{M2S/M2GL090(T|TS|TV)\} -action \{ERASE\}} \]

**See Also**

- `construct\_chain\_automatically`
- `scan\_chain\_prg`
- `enable\_device`
- `set\_debug\_programmer`
- `set\_device\_name`
- `set\_programming\_file`
- `set\_programming\_action`

save_active_probe_list

Tcl command; saves the list of active probes to a file.

\[ \text{save_active_probe_list -file file\_path} \]

**Arguments**

- **-file file\_path**
  The output file location.

**Example**

\[ \text{save_active_probe_list -file ".\/my\_probes.txt"} \]
scan_chain_prg

In single mode, this Tcl command runs scan chain on a programmer. In chain mode, this Tcl command runs scan and check chain on a programmer if devices have been added in the grid.

```
scan_chain_prg -name {programmer_name}
```

**Arguments**

- `-name`
  Specify the device (programmer) name. This argument is mandatory.

**Example**

```
scan_chain_prg -name {21428}
```

**See Also**

- `construct_chain_automatically`
- `enable_device`
- `set_debug_programmer`
- `set_device_name.htm`
- `set_programming_file`
- `set_programming_action`
- `run_selected_actions`

select_active_probe

Tcl command; manages the current selection of active probe points to be used by active probe READ operations. This command extends or replaces your current selection with the probe points found using the search pattern.

```
select_active_probe [-deviceName device_name] [-name probe_name_pattern] [-reset true|false]
```

**Arguments**

- `-deviceName`
  `device_name`
  Parameter is optional if only one device is available in the current configuration..

- `-name`
  `probe_name_pattern`
  Specifies the name of the probe. Optionally, search pattern string can specify one or multiple probe points. The pattern search characters “*” and “?” also can be specified to filter out the probe names.

- `-reset`
  `true | false`
  Optional parameter; resets all previously selected probe points. If name is not specified, empties out current selection.

**Example**

The following command selects three probes. In the below example, “grp1” is a group and “out” is a bus..

```
Select_active_probe -name out[5]:out[5]:Q
Select_active_probe -name out.out[1]:out[1]:Q \
  -name out.out[3]:out[3]:Q \
  -name out.out[5]:out[5]:Q
```
set_live_probe

Tcl command; set_live_probe channels A and/or B to the specified probe point(s). At least one probe point must be specified. Only exact probe name is allowed (i.e. no search pattern that may return multiple points).

```
set_live_probe [-deviceName device_name] [-probeA probe_name] [-probeB probe_name]
```

Arguments

- `device_name`
  Parameter is optional if only one device is available in the current configuration or set for debug (see SmartDebug user guide for details).
- `probeA probe_name`
  Specifies target probe point for the probe channel A.
- `probeB probe_name`
  Specifies target probe point for the probe channel B.

Exceptions

- The array must be programmed and active
- Active probe read or write operation will affect current settings of Live probe since they use same probe circuitry inside the device
- Setting only one Live probe channel affects the other one, so if both channels need to be set, they must be set from the same call to set_live_probe
- Security locks may disable this function
- In order to be available for Live probe, ProbeA and ProbeB I/O's must be reserved for Live probe respectively

Example

Sets the Live probe channel A to the probe point A12 on device MPF300TS_ES.

```
set_live_probe [-deviceName MPF300TS_ES] [-probeA A12]
```

set_debug_programmer

This Tcl command is used to set the debug programmer.

```
set_debug_programmer -name {programmer_name}
```

Arguments

- `programmer_name`
  Specify the programmer. This argument is mandatory.

Example

```
set_debug_programmer -name {S201YQST1V}
```

See Also

- construct_chain_automatically
- scan_chain_prg
- enable_device
- set_device_name
- set_programming_file
- set_programming_action
run_selected_actions

**set_programming_action**

This Tcl command is used to select the action for a device.

```
set_programming_action [-name {device_name}] -action {procedure_action}
```

**Arguments**

- **-name**
  Specify the device name. This argument is mandatory.
- **-action**
  Specify the programming action. This argument is mandatory.

**Example**

```
set_programming_action -name {MPF300(T_ES|TS_ES)} -action {DEVICE_INFO}
set_programming_action -name {M2S/M2GL090(T|TS|TV)} -action {ERASE}
```

**See Also**

construct_chain_automatically
scan_chain_prg
enable_device
set_debug_programmer
set_device_name
set_programming_file
run_selected_actions

**set_programming_file**

This Tcl command is used to set the programming file for a device. Either the file or the no_file flag must be specified. A programming file must be loaded. The device must be a Microsemi device.

```
set_programming_file -name {device_name} -file {stapl_file_name_with_path}
```

**Arguments**

- **-name**
  Specify the device name. This argument is mandatory.
- **-file**
  Specify the file path. This argument is mandatory.

**Example**

```
set_programming_file -name {MPF300(T_ES|TS_ES)} -file {D:/export/CM1_PCIE_TOP_default_uic_I2_200_0_I2.stp}
```

**See Also**

construct_chain_automatically
scan_chain_prg
enable_device
set_debug_programmer
smartbert_test

This Tcl command is used for the following:

- Start a Smart BERT test
- Stop a Smart BERT test
- Reset error count

smartbert_test -start

This Tcl command starts a Smart BERT test with a specified pattern on a specified lane.

smartbert_test -start -pattern {pattern_type} -lane {Physical_Location}

**Arguments**

**-start**
Start the Smart BERT test.

**pattern {pattern_type}**
Specify the pattern type of the Smart BERT test.

**-lane {Physical_Location}**
Specify the physical location of the lane.

**-EQ -NearEndLoopback**
Enable EQ-Near End Loopback on specified lane.

**Examples**

smartbert_test -start -pattern {prbs9} -lane {Q0_LANE3}
smartbert_test -start -pattern {prbs23} -lane {Q3_LANE2}
smartbert_test -start -pattern {prbs7} -lane {Q3_LANE1}
smartbert_test -start -pattern {prbs31} -lane {Q1_LANE2} -EQ -NearEndLoopback
smartbert_test -start -pattern {prbs9} -lane {Q2_LANE2} -EQ -NearEndLoopback
smartbert_test -start -pattern {prbs15} -lane {Q3_LANE3} -EQ -NearEndLoopback

smartbert_test -stop

This Tcl command stops a Smart BERT test on a specified lane.

smartbert_test -stop -lane {Physical_Location}

**Arguments**

**-stop**
Stop the smart BERT test.

**-lane {Physical_Location}**
Specify the physical location of the lane.

**Examples**

smartbert_test -stop -lane {Q0_LANE0}
smartbert_test -stop -lane {Q0_LANE3}
smartbert_test -stop -lane {Q3_LANE2}
smartbert_test -stop -lane {Q3_LANE1}
smartbert_test -stop -lane {Q1_LANE2}
smartbert_test -stop -lane {Q2_LANE2}
smartbert_test -stop -lane {Q2_LANE3}

smartbert_test -reset_counter
This Tcl command resets a lane error counter.

```tcl
smartbert_test -reset_counter -lane {Physical_Location}
```

**Arguments**

- `reset_counter`
  Reset lane error counter on hardware and cumulative error count on the UI.
- `lane {Physical_Location}`
  Specify the physical location of the lane.

**Examples**

```
smartbert_test -reset_counter -lane {Q0_LANE0}
smartbert_test -reset_counter -lane {Q3_LANE2}
smartbert_test -reset_counter -lane {Q2_LANE3}
smartbert_test -reset_counter -lane {Q2_LANE2}
smartbert_test -reset_counter -lane {Q1_LANE2}
smartbert_test -reset_counter -lane {Q3_LANE1}
```

static_pattern_transmit
This Tcl command starts and stops a Static Pattern Transmit.

**static_pattern_transmit -start**

```tcl
static_pattern_transmit -start -lane {Physical_Location} -pattern {pattern_type} -value {user_pattern_value}
```

**Parameters**

- `start`
  Start the Static Pattern Transmit.
- `lane {Physical_Location}`
  Specify physical location of lane.
- `pattern {pattern_type}`
  Specify pattern_type of Static Pattern Transmit.
- `value {user_pattern_value}`
  Specify user_pattern_value in hex if pattern_type selected is custom.

**Examples**

```
static_pattern_transmit -start -lane {Q0_LANE0} -pattern {fixed}
static_pattern_transmit -start -lane {Q0_LANE2} -pattern {maxrunlength} -value {}
static_pattern_transmit -start -lane {Q3_LANE2} -pattern {custom} -value {df}
static_pattern_transmit -start -lane {Q3_LANE0} -pattern {fixed} -value {}
static_pattern_transmit -start -lane {Q1_LANE1} -pattern {custom} -value {4578}
static_pattern_transmit -start -lane {Q1_LANE2} -pattern {fixed} -value {}
static_pattern_transmit -start -lane {Q2_LANE2} -pattern {maxrunlength} -value {}
static_pattern_transmit -start -lane {Q2_LANE1} -pattern {custom} -value {abcdef56}
```
### static_pattern_transmit -stop

static_pattern_transmit -stop -lane *(Physical_Location)*

#### Parameters

- **-stop**
  - Stop the Static Pattern Transmit.

- **-lane *(Physical_Location)***
  - Specify physical location of lane.

#### Examples

- `static_pattern_transmit -stop -lane Q0_LANE0`
- `static_pattern_transmit -stop -lane Q0_LANE2`
- `static_pattern_transmit -stop -lane Q3_LANE2`
- `static_pattern_transmit -stop -lane Q3_LANE0`
- `static_pattern_transmit -stop -lane Q1_LANE1`
- `static_pattern_transmit -stop -lane Q1_LANE2`
- `static_pattern_transmit -stop -lane Q2_LANE2`
- `static_pattern_transmit -stop -lane Q2_LANE1`

### ungroup

Tcl command; disassociates the probes as a group.

ungroup -name *group_name*

#### Arguments

- **-name *group_name***
  - Name of the group.

#### Example

- `ungroup -name my_grp4`

### unset_live_probe

Tcl command; discontinues the debug function and clears live probe A, live probe B, or both probes (Channel A/Channel B). An all zeros value is shown in the oscilloscope.

unset_live_probe -probeA 1 -probeB 1 [-deviceName *device_name*]

#### Arguments

- **-probeA**
  - Live probe Channel A.

- **-probeB**
  - Live probe Channel B.

- **-deviceName *device_name***
  - Parameter is optional if only one device is available in the current configuration or set for debug (see the SmartDebug User’s Guide for details).

#### Exceptions

- The array must be programmed and active.
- Active probe read or write operation affects current of Live Probe settings, because they use the same probe circuitry inside the device.
- Security locks may disable this function.

**Example**

The following example unsets live probe Channel A from the device MPF300TS_ES.

```tcl
unset_live_probe -probeA 1[-deviceName MPF300TS_ES]
```

**uprom_read_memory**

This Tcl command reads a uPROM memory block from the device.

```tcl
read_uprom_memory -startAddress {hex_value} -words {integer_value}
```

**Arguments**

- **-startAddress** *hex_value*
  Specifies the start address of the uPROM memory block.
- **-words** *integer_value*
  Specifies the number of 9-bit words.

**Example**

```tcl
read_uprom_memory -startAddress {0xA} -words {100}
```

**write_active_probe**

Tcl command; sets the target probe point on the device to the specified value. The target probe point name must be specified.

```tcl
write_active_probe [-deviceName device_name] -name probe_name -value true|false
- group_name group_bus_name -group_value "hex-value" | "binary-value"
```

**Arguments**

- **-deviceName** *device_name*
  Parameter is optional if only one device is available in the current configuration.
- **-name** *probe_name*
  Specifies the name for the target probe point. Cannot be a search pattern.
- **-value** true | false hex-value | binary-value
  Specifies values to be written.
  True = High
  False = Low
- **-group_name** *group_bus_name*
  Specify the group or bus name to write to complete group or bus.
- **-group_value** "hex-value" | "binary-value"
  Specify the value for the complete group or bus.
  Hex-value format: "<size>h<value>"
  Binary-value format: "<size>b<value>"

**Example**

```tcl
write_active_probe -name out[5]:out[5]:Q -value true <-- write to a single probe
```
write_active_probe -name grp1.out[3]:out[3]:Q -value low <- write to a probe in the group
write_active_probe -group_name grp1 -group_value “8’hF0” <- write the value to complete group
write_active_probe -group_name out -group_value “8‘b11110000” 
   -name out[2]:out[2]:Q -value true <- write multiple probes at the same time.

write_lsram
Tcl command; writes a word into the specified large SRAM location.

Physical block
write_lsram -name block_name] -offset offset_value -value integer_value

Arguments

-name block_name
   Specifies the name for the target block.
-offset offset_value
   Offset (address) of the target word within the memory block.
-value integer_value
   Word to be written to the target location. Depending on the configuration of memory blocks, the width can be 1, 2, 5, 10, or 20 bits.

Exceptions

- Array must be programmed and active
- The maximum value that can be written depends on the configuration of memory blocks
- Security locks may disable this function

Example
write_lsram -name {Fabric_Logic_0/U2/F_0_F0_U1/ramtmp_ramtmp_0_0/INST_RAM1K20_IP} -offset 0 -value 291

Logical block
write_lsram -logicalBlockName block_name -port port_name -offset 1 offset_value -logicalValue hexadecimal_value

Arguments

-logicalBlockName block_name
   Specifies the name of the user defined memory block.
-port port_name
   Specifies the port of the memory block selected. Can be either Port A or Port B.
-offset offset_value
   Offset (address) of the target word within the memory block.
-logicalValue hexadecimal_value
   Specifies the hexadecimal value to be written to the memory block. Size of the value is equal to the width of the output port selected.

Example
write_lsram -logicalBlockName {Fabric_Logic_0/U2/F_0_F0_U1} -port {Port A} -offset 1 -logicalValue {00FFF}
write_usram
Tcl command; writes a 12-bit word into the specified uSRAM location.

Physical block

```
write_usram -name block_name] -offset offset_value -value integer_value
```

**Arguments**
- `-name block_name`
  Specifies the name for the target block.
- `-offset offset_value`
  Offset (address) of the target word within the memory block.
- `-value integer_value`
  12-bit value to be written.

**Exceptions**
- Array must be programmed and active
- The maximum value that can be written is 0x1FF
- Security locks may disable this function

**Example**
Writes a value of 0x291 to the device PolarFire in the
Fabric.Logic_0/U3/F_0_F0_U1/ramtmp_ramtmp_0_0/INST_RAM64x12_IP with an offset of 0.
```
write_usram -name {Fabric.Logic_0/U3/F_0_F0_U1/ramtmp_ramtmp_0_0/INST_RAM64x12_IP} -offset 0 -value 291
```

Logical block

```
write_usram -logicalBlockName block_name -port port_name -offset offset_value -logicalValue hexadecimal_value
```

**Arguments**
- `-logicalBlockName block_name`
  Specifies the name of the user defined memory block.
- `-port port_name`
  Specifies the port of the memory block selected. Can be either Port A or Port B.
- `-offset offset_value`
  Offset (address) of the target word within the memory block.
- `-logicalValue hexadecimal_value`
  Specifies the hexadecimal value to be written to the memory block. Size of the value is equal to the width of the output port selected.

**Example**
```
write_usram -logicalBlockName {Fabric.Logic_0/U3/F_0_F0_U1} -port {Port A} -offset 1 -logicalValue {00FFF}
```

xcvr_read_register
This Tcl command reads SCB registers and their field values. Read value is in hex format. This command is used in SmartDebug Signal Integrity.

```
xcvr_read_register -inst_name <inst_name> -reg_name [<reg_name> | <reg_name:field_name>]
```
Arguments

- **-inst_name <inst_name>**
  Specify the lane instance name used in the design.

- **-reg_name <reg_name>**
  Specify the <reg_name> for register name or <reg_name>:<field_name> for the register’s field.

Examples

Reading pceslane’s 32-bit register LNTV_R0:

```
xvcvr_read_register -inst_name {CM1_PCIE_SS_0/PF_PCIE_0/LANE1} -reg_name {LNTV_R0}
```

Output:
```
Register Name: LNTV_R0 value: 0x12
The 'xcvr_write_register' command succeeded.
```

Reading Register LNTV_R0 field LNTV_RX_GEAR (i.e. 0th bit of 32-bit register):

```
xvcvr_read_register -inst_name {CM1_PCIE_SS_0/PF_PCIE_0/LANE1} -reg_name {LNTV_R0:LNTV_RX_GEAR}
```

Output:
```
Register Name: LNTV_R0:LNTV_RX_GEAR, Value: 0x0
The 'xcvr_read_register' command succeeded.
```

Exception: **SOFT_RESET Register**

The SOFT_RESET register is an SCB read/write register containing information such as block ID and Map IDs. It is also used to provide a pulsed reset to the SCB registers. It is a group-specific register.

The SOFT_RESET register is available with the four groups (pma_lane, pma_cmn, pceslanelane, and pcscmn). To read or write this register or its field value, "group name" must be added before "SOFT_RESET".

- **-reg_name <group name>_SOFT_RESET** for register name

or

- **[{<group name>_SOFT_RESET>:field_name}]** for register field name

where <group name> can be PCS, PCSCMN, PMA, or PMA_CMN.

Examples

Reading all four groups' SOFT_RESET register and its field BLOCKID

**Reading the PCS SOFT_RESET register and its field BLOCKID (i.e. 16th to 31st bit):**

```
xvcvr_read_register -inst_name SmartBERT_L4_0/PF_XCVR_0/LANE0 -reg_name {PCS_SOFTWARE_RESET}
```

Output:
```
Register Name: PCS_SOFTWARE_RESET, Value: 0x300100
The 'xcvr_read_register' command succeeded.
```

**Reading field BLOCKID:**

```
xvcvr_read_register -inst_name SmartBERT_L4_0/PF_XCVR_0/LANE0 -reg_name {PCS_SOFTWARE_RESET:BLOCKID}
```

Output:
```
Register Name: PCS_SOFTWARE_RESET:BLOCKID, Value: 0x30
The 'xcvr_read_register' command succeeded.
```
**Reading PCSCMN’s SOFT_RESET register and its field BLOCKID (i.e. 16th to 31st bit):**

```bash
cvr_read_register -inst_name SmartBERT_L4_0/PF_XCVR_0/LANE0 -reg_name {PCSCMN_SOFT_RESET}
```

Register Name: PCSCMN_SOFT_RESET, Value: 0x340100

The 'xcvr_read_register' command succeeded.

**Reading field BLOCKID:**

```bash
cvr_read_register -inst_name SmartBERT_L4_0/PF_XCVR_0/LANE0 -reg_name {PCSCMN_SOFT_RESET:BLOCKID}
```

Output:

Register Name: PCSCMN_SOFT_RESET:BLOCKID, Value: 0x34

The 'xcvr_read_register' command succeeded.

**Reading PMA’s SOFT_RESET register and its field BLOCKID (i.e. 16th to 31st bit):**

```bash
cvr_read_register -inst_name SmartBERT_L4_0/PF_XCVR_0/LANE0 -reg_name {PMA_SOFT_RESET}
```

Output:

Register Name: PMA_SOFT_RESET, Value: 0x1300100

The 'xcvr_read_register' command succeeded.

**Reading field BLOCKID:**

```bash
cvr_read_register -inst_name SmartBERT_L4_0/PF_XCVR_0/LANE0 -reg_name {PMA_SOFT_RESET:BLOCKID}
```

Output:

Register Name: PMA_SOFT_RESET:BLOCKID, Value: 0x130

The 'xcvr_read_register' command succeeded.

**Reading PMA_CMN’s SOFT_RESET register and it’s field BLOCKID (i.e. 16th to 31st bit):**

```bash
cvr_read_register -inst_name SmartBERT_L4_0/PF_XCVR_0/LANE0 -reg_name {PMA_CMN_SOFT_RESET}
```

Output:

Register Name: PMA_CMN_SOFT_RESET, Value: 0x1340100

The 'xcvr_read_register' command succeeded.

**Reading field BLOCKID:**

```bash
cvr_read_register -inst_name SmartBERT_L4_0/PF_XCVR_0/LANE0 -reg_name {PMA_CMN_SOFT_RESET:BLOCKID}
```

Output:

Register Name: PMA_CMN_SOFT_RESET:BLOCKID, Value: 0x134

The 'xcvr_read_register' command succeeded.

**See Also**

`xcvr_write_register`

**xcvr_write_register**

This Tcl command writes SCB registers and their field values. Write value is in hex format. This command is used in SmartDebug Signal Integrity.

```bash
cvr_write_register -inst_name <inst_name> -reg_name [<reg_name> | <reg_name:field_name>] -value {write_value}
```
Arguments

-\textit{inst\_name <inst\_name>}
Specify the lane instance name used in the design.

-\textit{reg\_name <reg\_name> \textasciitilde <reg\_name:field\_name>}
Specify the \textit{<reg\_name>} for register name or \textit{<reg\_name>:<field\_name>} for the register's field.

-\textit{value <write\_value>}
Specify the value in hex format.

Examples

Writing \textit{pcscmn}'s 32-bit register \textit{GSSCLK\_CTRL}

\begin{verbatim}
xcvr_write_register -inst_name {CM1_PCIE_SS_0/PP_PCIE_0/LANE1} -reg_name {GSSCLK\_CTRL} -value 0xffffffff
\end{verbatim}

Output:

Register Name: GSSCLK\_CTRL value: 0xffffffff
The 'xcvr_write_register' command succeeded.

Writing Register \textit{GSSCLK\_CTRL} field \textit{MCLK\_GSSCLK\_2\_SEL} i.e. 16th to 20th bits (5 bits) of 32-bit register

\begin{verbatim}
xcvr_write_register -inst_name {CM1_PCIE_SS_0/PP_PCIE_0/LANE1} -reg_name {GSSCLK\_CTRL\_MCLK\_GSSCLK\_2\_SEL} -value 0x6
\end{verbatim}

Output:

Register Name: GSSCLK\_CTRL\_MCLK\_GSSCLK\_2\_SEL value: 0x6
The 'xcvr_write_register' command succeeded.

Exception: \textit{SOFT\_RESET} Register

The \textit{SOFT\_RESET} register is an SCB read/write register containing information such as block ID and Map IDs. It is also used to provide a pulsed reset to the SCB registers. It is a group-specific register.

The \textit{SOFT\_RESET} register is available with the four groups (\textit{pma\_lane}, \textit{pma\_cmn}, \textit{pca\_lane}, and \textit{pcsc\_cmn}). To read or write this register or its field value, "group name" must be added before "SOFT\_RESET".

-\textit{reg\_name <group\_name>_<SOFT\_RESET>} for register name

or

-\textit{[<group\_name>_<SOFT\_RESET>:field\_name]} for register field name

where \textit{<group\_name>} can be \textit{PCS}, \textit{PCSCMN}, \textit{PMA}, or \textit{PMA\_CMN}

Examples

Writing all four groups' \textit{SOFT\_RESET} register and its field \textit{PERIPH}

\begin{verbatim}
Writing to the PCS SOFT\_RESET register (32-bits) and its field PERIPH (i.e. 8th bit):
xcvr_write_register -inst_name SmartBERT\_L4_0/PP_XCVR\_0/LANE0 -reg_name {PCS\_SOFT\_RESET} -value 0xffffffff
\end{verbatim}

Output:

Register Name: PCS\_SOFT\_RESET value: 0xffffffff
The 'xcvr_write_register' command succeeded.
Writing to field PERIPH:

xcvr_write_register -inst_name SmartBERT_L4_0/PF_XCVR_0/LANE0 -reg_name {PCS_SOFT_RESET:PERIPH} -value 0x1

Output:
Register Name: PCS_SOFT_RESET:PERIPH value: 0x1
The 'xcvr_write_register' command succeeded.

Writing to PCSCMN's SOFT_RESET register (32-bits) its field PERIPH (i.e. 8th bit):

xcvr_write_register -inst_name SmartBERT_L4_0/PF_XCVR_0/LANE0 -reg_name {PCSCMN_SOFT_RESET} -value 0xffffffff

Output:
Register Name: PCSCMN_SOFT_RESET value: 0xffffffff
The 'xcvr_write_register' command succeeded.

Writing to field PERIPH:

xcvr_write_register -inst_name SmartBERT_L4_0/PF_XCVR_0/LANE0 -reg_name {PCSCMN_SOFT_RESET:PERIPH} -value 0x1

Output:
Register Name: PCSCMN_SOFT_RESET:PERIPH value: 0x1
The 'xcvr_write_register' command succeeded.

Writing to PMA's SOFT_RESET register its field PERIPH (i.e. 8th bit):

xcvr_write_register -inst_name SmartBERT_L4_0/PF_XCVR_0/LANE0 -reg_name {PMA_SOFT_RESET} -value 0xffffffff

Output:
Register Name: PMA_SOFT_RESET value: 0xffffffff
The 'xcvr_write_register' command succeeded.

Writing to field PERIPH:

xcvr_write_register -inst_name SmartBERT_L4_0/PF_XCVR_0/LANE0 -reg_name {PMA_SOFT_RESET:PERIPH} -value 0x1

Output:
Register Name: PMA_SOFT_RESET:PERIPH value: 0x1
The 'xcvr_write_register' command succeeded.

Writing to PMA_CMN's SOFT_RESET register its field PERIPH (i.e. 8th bit):

xcvr_write_register -inst_name SmartBERT_L4_0/PF_XCVR_0/LANE0 -reg_name {PMA_CMN_SOFT_RESET} -value 0xffffffff

Output:
Register Name: PMA_CMN_SOFT_RESET value: 0xffffffff
The 'xcvr_write_register' command succeeded.

Writing to field PERIPH:

xcvr_write_register -inst_name SmartBERT_L4_0/PF_XCVR_0/LANE0 -reg_name {PMA_CMN_SOFT_RESET:PERIPH} -value 0x1

Output:
Register Name: PMA_CMN_SOFT_RESET:PERIPH value: 0x1
The 'xcvr_write_register' command succeeded.

See Also
xcvr_read_register
JTAG Configuration Tcl Commands

These commands take a script that contains JTAG chain configuration-specific Tcl commands and passes them to FlashPro Express for execution.

Note that these commands cannot be executed directly from Libero.

add_actel_device

Add an Actel device to the chain. Either the file or device parameter must be specified. Chain programming mode must have been set.

```
add_actel_device [-file {filename}] [-device {device}] -name {name}
```

**Arguments**

Where:

- `-file {filename}`
  Specifies a programming filename.
- `-device {device}`
  Specifies the device family (such as MPF300).
- `-name {name}`
  Specifies the device user name.

**Exceptions**

None

**Example**

```
add_actel_device -file {e:/design/stp/TOP.stp} -name {MyDevice1}
add_actel_device -device {MPF300} -name {MyDevice2}
```

add_non_actel_device

Add a non-Actel device in the chain. Either the file, or (-tck And -ir) parameters must be specified. The Chain programming mode must have been set.

```
add_non_actel_device [-file {filename}] [-ir {ir}] [-tck {tck}] [-name {name}]
```

**Arguments**

- `-file {filename}`
  Specifies a BSDL file.
- `-ir {ir}`
  Specifies the IR length.
- `-tck {tck}`
  Specifies the maximum TCK frequency (in MHz).
add_non_actel_device

Exceptions
None

Examples
add_non_actel_device -file {e:/design/bsdl/DeviceX.bsdl} -name {MyDevice3}
add_non_actel_device -ir 8 - tck 5 -name {MyDevice4}

add_non_actel_device_to_database
Imports settings via a BSDL file that adds non-Actel or non-Microsemi devices to the device database so that they are recognized during scan chain and auto-construction operations.

Arguments
- file {bsdl_filename}
  Specifies the path to the BSDL file and the BSDL filename add to the database.

Supported Families
All non-Microsemi and non-Actel families

Exceptions
N/A

Examples
The following example uses a BSDL file to add a non-Microsemi (1502AS J44) device to the device database:
add_non_actel_device_to_database -file {c:/bsdl/atmel/1502AS_J44.bsd}
The following example uses a BSDL file to add a non-Microsemi (80200) device to the device database:
add_non_actel_device_to_database -file {c:/bsdl/intel/80200_v1.0.bsd}

construct_chain_automatically
Automatically starts chain construction for the specified programmer.

Arguments
- name {name}
  Specifies the programmer(s) name(s).

Exceptions
N/A
Example

Example for one programmer:

```
construct_chain_automatically -name {21428}
```

Example for two programmers:

```
construct_chain_automatically -name {21428} -name {00579}
```

copy_device

Copies a device in the chain to the clipboard. Chain programming mode must be set. See the `paste_device` command for more information.

```
copy_device (-name {name})*
```

Arguments

- `-name {name}`
  
  Specifies the device name. Repeat this argument to copy multiple devices.

Exceptions

None

Example

The example copies the device 'mydevice1' to the same location with a new name 'mydevice2'.

```
copy_device -name {MyDevice1} -name {MyDevice2}
```

cut_device

Removes one or more devices from the chain. It places the removed device in the clipboard. Chain programming mode must be set to use this command. See the `paste_device` command for more information.

```
cut_device (-name {name})*
```

Arguments

- `-name {name}`
  
  Specifies the device name. You can repeat this argument for multiple devices.

Exceptions

None

Example

The following example removes the devices 'mydevice1' and 'mydevice2' from the chain.

```
cut_device -name {MyDevice1} -name {MyDevice2}
```

enable_device

Enables or disables a device in the chain (if the device is disabled, it is bypassed). Chain programming mode must be set. The device must be a Microsemi device.

```
enable_device -name {name} -enable {TRUE|FALSE}
```
Arguments

- **name** 
  Specifies your device name
- **enable** {TRUE|FALSE}
  Specifies whether the device is to be enabled or disabled. If you specify multiple devices, this argument applies to all specified devices. (TRUE = enable. FALSE = disable)

Exceptions

None

Example

The following example disables the device 'mydevice1' in the chain.
```
enable_device –name {MyDevice1} –enable {FALSE}
```

**paste_device**

Pastes the devices that are on the clipboard in the chain, immediately above the `position_name` device, if this parameter is specified. Otherwise it places the devices at the end of the chain. The chain programming mode must be enabled.

```
paste_device [-position_name {position_name}]
```

Arguments

- **position_name** {position_name}
  Optional argument that specifies the name of a device in the chain.

Exceptions

None

Examples

The following example pastes the devices on the clipboard immediately above the device 'mydevice3' in the chain.
```
paste_device -position_name {MyDevice3}
```

**remove_device**

Removes the device from the chain. Chain programming mode must be set.
```
remove_device (-name {name})*
```

Arguments

- **name** {name}
  Specifies the device name. You can repeat this argument for multiple devices.

Exceptions

None
Example

Remove a device 'M2S050T' from the chain:

```tcl
remove_device (-name (M2S050T))
```

**remove_non_actel_device_from_database**

Removes settings for non-Microsemi or non-Actel device from the device database.

```tcl
remove_non_actel_device_from_database [-name {device_name}]
```

**Arguments**

- `-name {device_name}`
  
  Specifies the non-Actel or non-Microsemi device name to be removed from the database. You can repeat this argument for multiple devices.

**Supported Families**

Non-Microsemi and non-Actel devices

**Exceptions**

None

**Example**

The following example removes the F1502AS_J44 device from the database:

```tcl
remove_non_actel_device_from_database -name {F1502AS_J44}
```

The following example removes the SA2_PROCESSOR device from the database:

```tcl
remove_non_actel_device_from_database -name {SA2_PROCESSOR}
```

**select_libero_design_device**

This command selects the Libero design device for the Programming Connectivity and Interface tool within Libero. This command is needed when the tool cannot automatically resolve the Libero design device when there are two or more identical devices that match the Libero design device in the configured JTAG chain.

```tcl
select_libero_design_device -name {device_name}
```

**Arguments**

- `-name {device_name}`
  
  Specifies a user-assigned unique device name in the JTAG chain.

**Exceptions**

None

**Example**

```tcl
select_libero_design_device -name {M2S050TS (2)}
select_libero_design_device -name {my_design_device}
```
Note

This Tcl command is typically used in a Tcl command script file that is passed to the Libero run_tool command.

```
run_tool -name {CONFIGURE_CHAIN} -script {<flashPro_cmd>.tcl}
```

set_bsdl_file

Sets a BSDL file to a non-Microsemi device in the chain. Chain programming mode must have been set. The device must be a non-Microsemi device.

```
set_bsdl_file -name {name} -file {file}
```

Arguments

- name {name}
  Specifies the device name.
- file {file}
  Specifies the BSDL file.

Supported Families

Any non-Microsemi device supported by FlashPro Express.

Exceptions

None

Example

The following example sets the BSDL file /design/bsdl/NewBSDL2.bsdl to the device 'MyDevice3':

```
set_bsdl_file -name {MyDevice3} -file {e:/design/bsdl/NewBSDL2.bsdl}
```

set_device_ir

Sets the IR length of a non-Microsemi device in the chain. Chain programming mode must be set. The device must be a non-Microsemi device.

```
set_device_ir -name {name} -ir {ir}
```

Arguments

- name {name}
  Specifies the device name.
- ir {ir}
  Specifies the IR length.

Supported Families

Any non-Microsemi device supported by FlashPro Express.

Exceptions

None

Example

The following example sets the IR length to '2' for the non-Microsemi device 'MyDevice4':

```
set_device_ir -name {MyDevice4} -ir 2
```
set_device_ir -name {MyDevice4} -ir {2}

set_device_name

Changes the user name of a device in the chain. Chain programming mode must be set.

set_device_name -name {name} -new_name {new_name}

Arguments

- name {name}
  Identifies the old device name.
- new_name {new_name}
  Specifies the new device name.

Exceptions

None

Example

The following example changes the user name of the device from 'MyDevice4' to 'MyDevice5':

set_device_name -name {MyDevice4} -new_name {MyDevice5}

set_device_order

Sets the order of the devices in the chain to the order specified. Chain programming mode must have been set. Unspecified devices will be at the end of the chain.

set_device_order (-name {name})*

Arguments

- name {name}
  Specifies the device name. To specify a new order you must repeat this argument and specify each device name in the order desired.

Exceptions

None

Example

The following example sets the device order for 'MyDevice1', 'MyDevice2', 'MyDevice3', and 'MyDevice4'. 'MyDevice2' is unspecified so it moves to the end of the chain.

set_device_order -name {MyDevice3} -name {MyDevice1} -name {MyDevice4}
  the new order is:
  MyDevice3 MyDevice1 MyDevice4 MyDevice2

set_device_tck

Sets the maximum TCK frequency of a non-Microsemi device in the chain. Chain programming mode must be set. The device must be a non-Microsemi device.

set_device_tck -name {name} -tck {tck}
Arguments

- **name** `{name}`
  Specifies the device name.

- **tck** `{tck}`
  Specifies the maximum TCK frequency (in MHz).

Supported Families

Any non-Microsemi device supported by FlashPro Express.

Exceptions

None

Example

The following example sets the maximum TCK frequency of the non-Microsemi device 'MyDevice4':

```
set_device_tck -name {MyDevice4} -tck {2.25}
```

**set_device_type**

Changes the family of a Microsemi device in the chain. The device must be a Microsemi device. The device parameter below is now optional.

```
set_device_type -name {name} -type {type}
```

Arguments

- **name** `{name}`
  Identifies the name of the device you want to change.

- **type** `{type}`
  Specifies the device family.

Exceptions

None

Example

The following example sets the device 'MyDevice2' to the type MPF300.

```
set_device_type -name {MyDevice2} -type {MPF300}
```

**set_programming_action**

This Tcl command is used to select the action for a device.

```
set_programming_action [-name {device_name}] -action {procedure_action}
```

Arguments

- **name**
  Specify the device name. This argument is mandatory.

- **action**
  Specify the programming action. This argument is mandatory.
Example

```
set_programming_action -name {MPF300(T_ES|TS_ES)} -action {DEVICE_INFO}
set_programming_action -name {M2S/M2GL090(T|TS|TV)} -action {ERASE}
```

See Also

- construct_chain_automatically
- scan_chain_prg
- enable_device
- set_debug_programmer
- set_device_name
- set_programming_file
- run_selected_actions

**set_programming_file**

This Tcl command is used to set the programming file for a device. Either the file or the no_file flag must be specified. A programming file must be loaded. The device must be a Microsemi device.

```
set_programming_file -name {device_name} -file {stapl_file_name_with_path}
```

Arguments

- `-name`
  Specify the device name. This argument is mandatory.
- `-file`
  Specify the file path. This argument is mandatory.

Example

```
set_programming_file -name {MPF300(T_ES|TS_ES)} -file {D:/export/CM1_PCIE_TOP_default_uic_12_200_0_12.stp}
```

See Also

- construct_chain_automatically
- scan_chain_prg
- enable_device
- set_debug_programmer
- set_device_name
- set_programming_action
- run_selected_actions
Example Tcl Script to Create a NativePMA_prbs Design

To run the below Tcl script to create the design, download the designs files from https://coredocs.s3.amazonaws.com/Libero/12_0_0/support_files/tcl_ref_gde_examples_pf/web_upload.7z and execute the Tcl script DG0759_pma.

```tcl
set PF_XCVRver {2.0.100}
set PF_XCVR_ERMver {2.0.100}
set PF_XCVR_REF_CLKver {1.0.103}
set PF_TX_PLLver {2.0.002}
set PF_CCCver {1.0.115}
set PF_OSCver {1.0.102}
set PF_CORECORTEXM1ver {3.0.100}
set PF_CoreAHBLitever {5.3.101}
set PF_COREAHBTOAPB3ver {3.1.100}
set PF_CoreAPB3ver {4.1.100}
set COREUARTver {5.6.102}
set CoreJESD204BTXver {3.0.114}
set CoreJESD204BRXver {3.0.126}
set PF_URAMver {1.1.107}
set PF_INIT_MONITORver {2.0.103}
set COREFIFOver {2.6.108}
set CORERESET_PFver {2.1.100}
set PF_CORESMARTBERTver {2.2.101}
set LiteFastver {1.0.2}
set XCVRparamver 2.0.100
set use_enhanced_constraint_flow 1
set PrJname "DG0759_pma"
set Proj "/$PrJname"
set tb {testbench}
#file delete -force "$Proj"
set rootcomp {NativePMA_Prbs}
set rootcomp1 NativePMA_Prbs
set TOP NativePMA_Prbs
set error 0
set error1 0
set warning "SmartDesign '$rootcomp1' was generated, but"
set Msg1 "THE error_out SIGNAL IS LOW AS EXPECTED"
set Msg2 "THE error_count SIGNAL IS LOW AS EXPECTED"
```
set Msg3 "THE lock SIGNAL IS HIGH AS EXPECTED"
set Msg4 "NON-DATA SIMULATIONS PASSED"
set SimTime 100us
set NUM_TX_PLL 1
set quad 1
set txpll_refclk_mode "ded"
set xcvrrefclk_refclk_mode "diff"
#Device Selection
set family {PolarFire}
set die {MPF300T}
set package {FCG1152}
set speed {-1}
set die_voltage {1.0}
set part_range {EXT}
#Device Settings
set IOTech {LVCMOS 1.8V}
set ResProbe {1}
set ResSPI {0}
#Analysis operating conditions
set TEMPR {EXT}
set VOLTR {EXT}
set IOVOLTR_12 {EXT}
set IOVOLTR_15 {EXT}
set IOVOLTR_18 {EXT}
set IOVOLTR_25 {EXT}
set IOVOLTR_33 {EXT}
#Design Flow
set HDL {VERILOG}
set Block 0
set SAPI 0
set vmflow 1
set synth 1
set fanout {10}
#XCVR_Parameters
set UI_IS_CONFIGURED true
set UI_XCVR_RX_ENHANCED_MANAGEMENT false
set UI_XCVR_RX_CALIBRATION None
set XT_ES_DEVICE false
set UI_PROTOCOL_PRESET_USED EPCS
set UI_NUMBER_OF_LANES 1
set UI_TX_RX_MODE Duplex
set UI_TX_DATA_RATE 5000
set UI_TX_CLK_DIV_FACTOR 1
set UI_ENABLE_SWITCH_BETWEEN_TXPLLs false
set UI_ENABLE_SWITCH_BETWEEN_CDR_REFCLKs false
set UI_CDR_REFERENCE_CLK_SOURCE Dedicated
set UI_CDR_REFERENCE_CLK_FREQ 156.25
set UI_CDR_REFERENCE_CLK_TOLERANCE 1
set UI_CDR_LOCK_MODE "(Lock to data)"
set UI_TX_PCS_FAB_IF_WIDTH 40
set UI_INTERFACE_TXCLOCK "(Regional)"
set UI_INTERFACE_RXCLOCK "(Regional)"
set UI_USE_INTERFACE_CLK_AS_PLL_REFCLK false
set UI_ENABLE_PMA_MODE true
set UI_ENABLE_8B10B_MODE false
set UI_ENABLE_64B6XB_MODE false
set UI_ENABLEPIPE_MODE false
set UI_ENABLE_64B66B true
set UI_ENABLE_64B67B false
set UI_ENABLE_DISPARITY false
set UI_ENABLE_SCRAMBLING false
set UI_ENABLE_BER false
set UI_ENABLE_32BIT_DATA_WIDTH false
set UI_PIPE_PROTOCOL_USED {"PCIe Gen1 (2.5 Gbps)"
set UI_EXPOSE_CDR_BITSLIP_PORT false
set UI_EXPOSE_JA_CLOCK_PORT false
set UI_EXPOSE_DYNAMIC_RECONFIGURATION_PORTS false
set EXPOSE_FWF_EN_PORTS false
set UI_EXPOSE_TX_BYPASS_DATA false
set UI_EXPOSE_TX_ELEC_IDLE false
set UI_ENABLE_FIBRE_CHANNEL_DISPARITY false
set UI_ENABLE_PHASE_COMP_MODE false
set UI_FABIF_BUS_IS_USED false
set SD_EXPORT_HIDDEN_PORTS false
set EXPOSE_ALL_DEBUG_PORTS false
# create a new project
new_project -ondemand_build_dh 1 -location "$Proj" -name "$Prjname" -project_description {} -block_mode $Block -standalone_peripheral_initialization $SAPI -use_enhanced_constraint_flow $use_enhanced_constraint_flow -hdl $HDL -family $family -die $die -package $package -speed $speed -die_voltage $die_voltage -part_range $part_range -adv_options IO_DEFT_STD:$IOTech -adv_options RESTRICTPROBEPINS:$ResProbe -adv_options RESTRICTSPIPINS:$ResSPI -adv_options TEMPR:$TEMPR -adv_options VCCI_1.2_VOLTR:$IOVOLT_12 -adv_options VCCI_1.5_VOLTR:$IOVOLT_15 -adv_options VCCI_1.8_VOLTR:$IOVOLT_18 -adv_options VCCI_2.5_VOLTR:$IOVOLT_25 -adv_options VCCI_3.3_VOLTR:$IOVOLT_33 -adv_options VOLTR:$VOLT
# import_files
import_files \
-convert_EDN_to_HDL 0 \
-hdl_source "/src/hdl/FabUART.v" \
-hdl_source "/src/hdl/prbs_asic_chk.v" \
-hdl_source "/src/hdl/prbs_asic_gen.v" \
-hdl_source "/src/hdl/PRBS_chk.v" \
-hdl_source "/src/hdl/PRBS_gen.v"
build_design_hierarchy

set SD {UART_INTERFACE}
create_smartdesign -sd_name $SD
build_design_hierarchy

sd_instantiate_hdl_module -sd_name $SD -hdl_module_name {FabUART} -hdl_file \\n{hdl\FabUART.v} -instance_name {FabUART_0}
create_and_configure_core -core_vlnv "Actel:DirectCore:COREUART:$COREUARTver" -component_name {COREUART_comp} \
-params {"TX_FIFO:0" "RX_FIFO:0" "RX_LEGACY_MODE:0" "BAUD_VAL_FRCTN_EN:true" \
"testbench:User" "USE_SOFT_FIFO:0" "HDL_license:U"}

sd_instantiate_component -sd_name $SD -component_name {COREUART_comp} -instance_name {COREUART_comp_0}

sd_connect_pins -sd_name $SD -pin_names {COREUART_comp_0:OEN \
FabUART_0:uart_oen}
sd_connect_pins -sd_name $SD -pin_names {COREUART_comp_0:WEN \
FabUART_0:uart_wen}
sd_connect_pins -sd_name $SD -pin_names {COREUART_comp_0:DATA_IN \
FabUART_0:uart_data_out}
sd_connect_pins -sd_name $SD -pin_names {COREUART_comp_0:RXRDY \
FabUART_0:uart_rxrdy}
sd_connect_pins -sd_name $SD -pin_names {COREUART_comp_0:TXRDY \
FabUART_0:uart_txrdy}
sd_connect_pins -sd_name $SD -pin_names {COREUART_comp_0:DATA_OUT \
FabUART_0:uart_data_in}
sd_connect_pins -sd_name $SD -pin_names {COREUART_comp_0:RESET_N \
FabUART_0:reset}
sd_connect_pins -sd_name $SD -pin_names {COREUART_comp_0:CLK \
FabUART_0:clk}
sd_connect_pin_to_port -sd_name $SD -pin_name {COREUART_comp_0:CLK}
sd_connect_pin_to_port -sd_name $SD -pin_name {COREUART_comp_0:RESET_N}
sd_connect_pin_to_port -sd_name $SD -pin_name {COREUART_comp_0:RX}
sd_connect_pins_to_constant -sd_name $SD -pin_names {COREUART_comp_0:BIT8} -value {VCC}
sd_connect_pins_to_constant -sd_name $SD -pin_names {COREUART_comp_0:CSN} -value {GND}
sd_connect_pins_to_constant -sd_name $SD -pin_names \
{COREUART_comp_0:ODD_N_EVEN} -value (GND)
sd_connect_pins_to_constant -sd_name $SD -pin_names {COREUART_comp_0:PARIITY_EN} -value {GND}
sd_connect_pins_to_constant -sd_name $SD -pin_names {COREUART_comp_0:BAUD_VAL} -value {0x32C}
sd_connect_pins_to_constant -sd_name $SD -pin_names {COREUART_comp_0:BAUD_VAL_FRACTION} -value {0x6}
sd_mark_pins_unused -sd_name $SD -pin_names {COREUART_comp_0:OVERFLOW}
sd_mark_pins_unused -sd_name $SD -pin_names {COREUART_comp_0:PARITY_ERR}
sd_mark_pins_unused -sd_name $SD -pin_names {COREUART_comp_0:FRAMING_ERR}
sd_connect_pin_to_port -sd_name $SD -pin_name {FabUART_0:rx_val}
sd_rename_port -sd_name $SD -library {} -current_port_name {rx_val} -new_port_name {EPCS_RX_VAL}
sd_connect_pin_to_port -sd_name $SD -pin_name {FabUART_0:rx_lock}
sd_connect_pin_to_port -sd_name $SD -pin_name {FabUART_0:error_error}
sd_connect_pin_to_port -sd_name $SD -pin_name {FabUART_0:start}
sd_connect_pin_to_port -sd_name $SD -pin_name {FabUART_0:clear}
sd_connect_pin_to_port -sd_name $SD -pin_name {FabUART_0:generate_err}
sd_connect_pin_to_port -sd_name $SD -pin_name {FabUART_0:connect_o}
sd_mark_pins_unused -sd_name $SD -pin_names {FabUART_0:switch}
sd_mark_pins_unused -sd_name $SD -pin_names {FabUART_0:timer_switch}
generate_component -component_name $SD -recursive 0

# Create SmartDesign Reset_Block
set SD {Reset_Block}
create_smartdesign -sd_name $SD
create_and_configure_core -core_vlnv "Actel:DirectCore:CORERESET_PF:$CORERESET_PFver" -component_name {reset_syn} \
-params {"testbench:User"}
sd_instantiate_component -sd_name $SD -component_name {reset_syn} -instance_name {Reset_sync_tx_0}
sd_instantiate_component -sd_name $SD -component_name {reset_syn} -instance_name {Reset_sync_rx_0}
sd_instantiate_component -sd_name $SD -component_name {reset_syn} -instance_name {Reset_sync_uart_0}
sd_connect_pin_to_port -sd_name $SD -pin_name {Reset_sync_tx_0:CLK}
sd_rename_port -sd_name $SD -current_port_name {CLK} -new_port_name {TX_clk}
sd_connect_pin_to_port -sd_name $SD -pin_name {Reset_sync.tx_0:EXT_RST_N} -current_port_name {Start}

#sd_connect_pin_to_port -sd_name $SD -pin_name {Reset_sync.tx_0:PLL_LOCK} -current_port_name {PLL_LOCK} -new_port_name {TX_clk_stable}
sd_connect_pin_to_port -sd_name $SD -pin_name {Reset_sync.tx_0:INIT_DONE}
sd_connect_pin_to_port -sd_name $SD -pin_name {Reset_sync.tx_0:FABRIC_RESET_N}
sd_rename_port -sd_name $SD -current_port_name {FABRIC_RESET_N} -new_port_name {Pattern_gen_rst_n}
sd_connect_pins_to_constant -sd_name $SD -pin_names {Reset_sync.tx_0:SS_BUSY} -value {GND}
```tcl
sd_connect_pins_to_constant -sd_name $SD -pin_names
{Reset_sync_rx_0:FF_US_RESTORE} -value {GND}

sd_connect_pin_to_port -sd_name $SD -pin_name (Reset_sync_rx_0:CLK)

sd_rename_port -sd_name $SD -current_port_name {CLK} -new_port_name {RX_clk}

sd_connect_pins -sd_name $SD -pin_names "$SD:Start Reset_sync_rx_0:EXT_RST_N"

sd_connect_pin_to_port -sd_name $SD -pin_name (Reset_sync_rx_0:PLL_LOCK)

sd_rename_port -sd_name $SD -current_port_name {PLL_LOCK} -new_port_name {RX_ready}

sd_connect_pins -sd_name $SD -pin_names "$SD:INITDONE
Reset_sync_rx_0:INIT_DONE"

sd_connect_pin_to_port -sd_name $SD -pin_name (Reset_sync_rx_0:FABRIC_RESET_N)

sd_rename_port -sd_name $SD -current_port_name {FABRIC_RESET_N} -new_port_name {Pattern_chk_rst_n}

sd_connect_pins_to_constant -sd_name $SD -pin_names {Reset_sync_rx_0:SS_BUSY} -value {GND}

sd_connect_pins_to_constant -sd_name $SD -pin_names {Reset_sync_rx_0:FF_US_RESTORE} -value {GND}

sd_rename_port -sd_name $SD -current_port_name {CLK} -new_port_name {uart_clk}

sd_connect_pins -sd_name $SD -pin_names "{SD}:INITDONE
Reset_sync_UART_0:INIT_DONE"

sd_connect_pin_to_port -sd_name $SD -pin_name (Reset_sync_UART_0:PLL_LOCK)

sd_rename_port -sd_name $SD -current_port_name {FABRIC_RESET_N} -new_port_name {uart_rst_n}

sd_connect_pins_to_constant -sd_name $SD -pin_names {Reset_sync_UART_0:SS_BUSY} -value {GND}

sd_connect_pins_to_constant -sd_name $SD -pin_names {Reset_sync_UART_0:FF_US_RESTORE} -value {GND}

generate_component -component_name $SD -recursive 0

# create smartdesign top
create_smartdesign -sd_name $TOP

create_and_configure_core -core_vlnv
"Actel:SystemBuilder:PF_XCVR_ERM:${PF_XCVR_ERMver}" -component_name
{PF_XCVR_ERM_comp} \ 
-params "UI_PROTOCOL_PRESET_USED:${UI_PROTOCOL_PRESET_USED} \ 
UI_NUMBER_OF_LANES:${UI_NUMBER_OF_LANES} \ 
UI_XCVR_RX_CALIBRATION:${UI_XCVR_RX_CALIBRATION} \ 
UI_XCVR_RX_ENHANCED_MANAGEMENT:${UI_XCVR_RX_ENHANCED_MANAGEMENT} \ 
UI_TX_RX_MODE:${UI_TX_RX_MODE} \ 
UI_TX_DATA_RATE:${UI_TX_DATA_RATE} \ 
UI_TX_CLK_DIV_FACTOR:${UI_TX_CLK_DIV_FACTOR} \ 
UI_CDR_REFERENCE_CLK_SOURCE:${UI_CDR_REFERENCE_CLK_SOURCE} \ 
UI_CDR_REFERENCE_CLK_FREQ:${UI_CDR_REFERENCE_CLK_FREQ} \ 
```
UI_CDR_REFERENCE_CLK_TOLERANCE:${UI_CDR_REFERENCE_CLK_TOLERANCE} \nUI_CDR_LOCK_MODE:${UI_CDR_LOCK_MODE} \nUI_TX_PCS_FAB_IF_WIDTH:${UI_TX_PCS_FAB_IF_WIDTH} \nUI_INTERFACE_TXCLOCK:${UI_INTERFACE_TXCLOCK} \nUI_INTERFACE_RXCLOCK:${UI_INTERFACE_RXCLOCK} \nUI_USE_INTERFACE_CLK_AS_PLL REFCLK:${UI_USE_INTERFACE_CLK_AS_PLL_REFCLK} \nUI_ENABLE_PMA_MODE:${UI_ENABLE_PMA_MODE} \nUI_ENABLE_8B10B_MODE:${UI_ENABLE_8B10B_MODE} \nUI_ENABLE_64B6XB_MODE:${UI_ENABLE_64B6XB_MODE} \nUI_ENABLE_PIPE_MODE:${UI_ENABLE_PIPE_MODE} \nUI_ENABLE_64B66B:${UI_ENABLE_64B66B} \nUI_ENABLE_64B67B:${UI_ENABLE_64B67B} \nUI_ENABLE_DISPARITY:${UI_ENABLE_DISPARITY} \nUI_ENABLE_SCRAMBLING:${UI_ENABLE_SCRAMBLING} \nUI_ENABLE_BER:${UI_ENABLE_BER} \nUI_ENABLE_32BIT_DATA_WIDTH:${UI_ENABLE_32BIT_DATA_WIDTH} \nUI_PIPE_PROTOCOL_USED:${UI_PIPE_PROTOCOL_USED} \nUI_EXPOSE_CDR_BITSLIP_PORT:${UI_EXPOSE_CDR_BITSLIP_PORT} \nUI_EXPOSE_JA_CLOCK_PORT:${UI_EXPOSE_JA_CLOCK_PORT} \nEXPOSE_FWF_EN_PORTS:${EXPOSE_FWF_EN_PORTS} \nUI_EXPOSE_DYNAMIC_RECONFIGURATION_PORTS:${UI_EXPOSE_DYNAMIC_RECONFIGURATION_PORTS} \nUI_ENABLE_SWITCH_BETWEEN_TXPLLS:${UI_ENABLE_SWITCH_BETWEEN_TXPLLS} \nUI_ENABLE_SWITCH_BETWEEN_CDR_REFCLKS:${UI_ENABLE_SWITCH_BETWEEN_CDR_REFCLKS} \nUI_ENABLE_FIBRE_CHANNEL_DISPARITY:${UI_ENABLE_FIBRE_CHANNEL_DISPARITY} \nSD_EXPORT_HIDDEN_PORTS:${SD_EXPORT_HIDDEN_PORTS} \nEXPOSE_ALL_DEBUG_PORTS:${EXPOSE_ALL_DEBUG_PORTS} \nXT_ES_DEVICE:${XT_ES_DEVICE} \nUI_EXPOSE_TX_BYPASS_DATA:${UI_EXPOSE_TX_BYPASS_DATA} \nUI_EXPOSE_TX_ELEC_IDLE:${UI_EXPOSE_TX_ELEC_IDLE}"

create_and_configure_core -core_vlnv "Actel:SgCore:PF TX_PLL:${PF_TX_PLLver}" -component_name {PF_TX_PLL_comp} \
-params "TxPLL_MODE:NORMAL \nTxPLL_REF:156.25 \nTxPLL_FAB_REF:200 \nTxPLL_OUT:2500.000 \nTxPLL_SSM_DEPTH:0 \nTxPLL_SSM_DOWN_SPREAD:false \nTxPLL_DYNAMIC_RECONFIG_INTERFACE_EN:false \nTxPLL_SSM_DIVVAL:1 \nTxPLL_EXT_WAVE_SEL:0 \nTxPLL_SSM_RAND_PATTERN:0 \n
TxPLL_SSM_FREQ:64 \
TxPLL_SOURCE:DEDICATED \
TxPLL_AUX_OUT:125 \
TxPLL_AUX_LOW_SEL:true \
TxPLL_FAB_LOCK_EN:false \
TxPLL_CLK_125_EN:true \
INIT:0x0 \
VCOFREQUENCY:1600"

create_and_configure_core -core_vlnv
"Actel:SgCore:PF_XCVR_REF_CLK:$(PF_XCVR_REF_CLKver)" -component_name
{PF_XCVR_REF_CLK_comp} \
-params "ENABLE_FAB_CLK_0:true \nENABLE_FAB_CLK_1:false \nENABLE_REF_CLK_0:true \nENABLE_REF_CLK_1:false \nREF_CLK_MODE_0:DIFFERENTIAL \nREF_CLK_MODE_1:LVCMOS" 

sd_instantiate_component -sd_name $TOP -component_name {PF_XCVR_ERM_comp} -instance_name {PF_XCVR_ERM_comp_0}

sd_instantiate_component -sd_name $TOP -component_name {PF_XCVR_REF_CLK_comp} -instance_name {PF_XCVR_REF_CLK_comp_0}

sd_instantiate_component -sd_name $TOP -component_name {PF_TX_PLL_comp} -instance_name {PF_TX_PLL_comp_0}

sd_create_scalar_port -sd_name $TOP -port_name {LANE0_PCS_ARST_N} -port_direction {IN}

sd_create_scalar_port -sd_name $TOP -port_name {LANE0_PMA_ARST_N} -port_direction {IN}

sd_create_bus_port -sd_name $TOP -port_name {LANE0_TX_DATA} -port_direction {IN} -port_range {{39:0}}

sd_create_scalar_port -sd_name $TOP -port_name {LANE0_RX_BYPASS_DATA} -port_direction {OUT}

sd_create_scalar_port -sd_name $TOP -port_name {LANE0_RX_CLK_R} -port_direction {OUT}

sd_create_scalar_port -sd_name $TOP -port_name {LANE0_TX_CLK_R} -port_direction {OUT}

sd_create_scalar_port -sd_name $TOP -port_name {LANE0_RX_IDLE} -port_direction {OUT}

sd_create_scalar_port -sd_name $TOP -port_name {LANE0_RX_READY} -port_direction {OUT}

sd_create_scalar_port -sd_name $TOP -port_name {LANE0_RX_VAL} -port_direction {OUT}

sd_create_scalar_port -sd_name $TOP -port_name {LANE0_TX_CLK_STABLE} -port_direction {OUT}

sd_create_bus_port -sd_name $TOP -port_name {LANE0_RX_DATA} -port_direction {OUT} -port_range {{39:0}}

sd_connect_pins -sd_name $TOP -pin_names "${TOP}:LANE0_PCS_ARST_N PF_XCVR_ERM_comp_0:LANE0_PCS_ARST_N"
sd_connect_pins -sd_name $TOP -pin_names "${TOP}:LANE0_PMA_ARST_N PF_XCVR_ERM_comp_0:LANE0_PMA_ARST_N"

sd_connect_pins -sd_name $TOP -pin_names "${TOP}:LANE0_TX_DATA PF_XCVR_ERM_comp_0:LANE0_TX_DATA"

sd_connect_pins -sd_name $TOP -pin_names "${TOP}:LANE0_RX_BYPASS_DATA PF_XCVR_ERM_comp_0:LANE0_RX_BYPASS_DATA"

sd_connect_pins -sd_name $TOP -pin_names "${TOP}:LANE0_RX_CLK_R PF_XCVR_ERM_comp_0:LANE0_RX_CLK_R"

sd_connect_pins -sd_name $TOP -pin_names "${TOP}:LANE0_TX_CLK_R PF_XCVR_ERM_comp_0:LANE0_TX_CLK_R"

sd_connect_pins -sd_name $TOP -pin_names "${TOP}:LANE0_RX_IDLE PF_XCVR_ERM_comp_0:LANE0_RX_IDLE"

sd_connect_pins -sd_name $TOP -pin_names "${TOP}:LANE0_RX_READY PF_XCVR_ERM_comp_0:LANE0_RX_READY"

sd_connect_pins -sd_name $TOP -pin_names "${TOP}:LANE0_RX_VAL PF_XCVR_ERM_comp_0:LANE0_RX_VAL"

sd_connect_pins -sd_name $TOP -pin_names "${TOP}:LANE0_TX_CLK_STABLE PF_XCVR_ERM_comp_0:LANE0_TX_CLK_STABLE"

sd_connect_pins -sd_name $TOP -pin_names "${TOP}:LANE0_RX_DATA PF_XCVR_ERM_comp_0:LANE0_RX_DATA"

sd_connect_pins -sd_name $TOP -pin_names {"PF_XCVR_REF_CLK_comp_0:REF_CLK" "PF_XCVR_ERM_comp_0:LANE0_CDR_REF_CLK_0"}

sd_connect_pins -sd_name $TOP -pin_names {"PF_XCVR_REF_CLK_comp_0:REF_CLK" "PF_TX_PLL_comp_0:CLK_125"

sd_connect_pins -sd_name $TOP -port_name {CLK_125} -port_direction {OUT}

sd_connect_pins -sd_name $TOP -port_name {PLL_LOCK} -port_direction {OUT}

sd_connect_pins -sd_name $TOP -pin_names "${TOP}:CLK_125 PF_TX_PLL_comp_0:CLK_125"

sd_connect_pins -sd_name $TOP -pin_names "${TOP}:PLL_LOCK PF_TX_PLL_comp_0:PLL_LOCK"

sd_connect_pins -sd_name $TOP -pin_names {"PF_TX_PLL_comp_0:CLKS_TO_XCVR" "PF_XCVR_ERM_comp_0:CLKS_FROM_TXPLL_0"}

sd_mark_pins_unused -sd_name $TOP -pin_names {PF_XCVR_REF_CLK_comp_0:FAB_REF_CLK}

create_and_configure_core -core_vlnv "Actel:SgCore:PF_OSC:${PF_OSCver}" -component_name {PF_OSC_comp} \
-params {"RCOSC_160MHZ_GL_EN:true" "RCOSC_160MHZ_CLK_DIV_EN:false" "RCOSC_160MHZ_NGMUX_EN:false" "RCOSC_2MHZ_GL_EN:false" "RCOSC_2MHZ_CLK_DIV_EN:false" "RCOSC_2MHZ_NGMUX_EN:false" "SD_EXPORT_HIDDEN_PORTS:false" "TGIGEN_DISPLAY_LOG_WINDOW:false" "TGIGEN_DISPLAY_SYMBOL:true"}

create_and_configure_core -core_vlnv "Actel:SgCore:PF_CCC:${PF_CCCver}" -component_name {PF_CCC_comp} \
-params {"GL0_0_IS_USED:true" "GL0_0_OUT_FREQ:125" "PLL_BANDWIDTH_0:2" "PLL_BANDWIDTH_1:1" "PLL_IN_FREQ_0:160"}

create_and_configure_core -core_vlnv "Actel:SgCore:PF_INIT_MONITOR:${PF_INIT_MONITORver}" -component_name {Init_macro} \
-params {}
-params "CTRL_TYPE:2 \\ 
SYNC:0 \\ 
PIPE:1 \\ 
ECC:0 \\ 
PREFETCH:false \\ 
FWFT:false \\ 
RCLK_EDGE:1 \\ 
WCLK_EDGE:1 \\ 
RE_POLARITY:0 \\ 
WE_POLARITY:0 \\ 
RESET_POLARITY:0 \\ 
RWIDTH:35 \\ 
RDEPTH:1024 \\ 
WWIDTH:35 \\ 
WDEPTH:1024 \\ 
READ_DVALID:false \\ 
WRITE_ACK:false \\ 
ESTOP:false \\ 
UNDERFLOW_EN:false \\ 
FSTOP:false \\ 
OVERFLOW_EN:false \\ 
AE_STATIC_EN:false \\ 
AF_STATIC_EN:false \\ 
AFVAL:4 \\ 
AFSTATIC_EN:false \\ 
AFVAL:1020 \\ 
WRCNT_EN:false \\ 
RDCNT_EN:false \\ 
testbench:User"
set SD {UART_INTERFACE}
sd_instantiate_component -sd_name $TOP -component_name $SD -instance_name ${SD}_0
set SD {Reset_Block}
sd_instantiate_component -sd_name $TOP -component_name $SD -instance_name ${SD}_0
build_design_hierarchy
set_root -module ${TOP}::work
sd_instantiate_hdl_module -sd_name $TOP -hdl_module_name {PRBS_gen} -hdl_file {hdl\PRBS_gen.v} -instance_name {PRBS_gen_0}
sd_instantiate_hdl_module -sd_name $TOP -hdl_module_name {PRBS_chk} -hdl_file {hdl\PRBS_chk.v} -instance_name {PRBS_chk_0}
sd_instantiate_component -sd_name $TOP -component_name {PF_OSC_comp} -instance_name {PF_OSC_comp_0}
sd_instantiate_component -sd_name $TOP -component_name {PF_CCC_comp} -instance_name {PF_CCC_comp_0}
sd_instantiate_component -sd_name $TOP -component_name {Init_macro} -instance_name {Init_macro_0}

sd_instantiate_component -sd_name $TOP -component_name {FIFO_CDC} -instance_name {FIFO_CDC_0}

sd_delete_ports -sd_name $TOP -port_names {LANE0_TX_DATA}

sd_delete_ports -sd_name $TOP -port_names {LANE0_RX_READY}

sd_delete_ports -sd_name $TOP -port_names {LANE0_PCS_ARST_N}

sd_delete_ports -sd_name $TOP -port_names {LANE0_RX_VAL}

sd_delete_ports -sd_name $TOP -port_names {LANE0_RX_IDLE}

sd_delete_ports -sd_name $TOP -port_names {LANE0_PMA_ARST_N}

sd_delete_ports -sd_name $TOP -port_names {LANE0_TX_CLK_STABLE}

sd_delete_ports -sd_name $TOP -port_names {LANE0_RX_DATA}

sd_delete_ports -sd_name $TOP -port_names {LANE0_RX_BYPASS_DATA}

sd_connect_pins -sd_name $TOP -pin_names {PF_XCVR_ERM_comp_0:LANE0_TX_DATA PRBS_gen_0:data_out}

sd_connect_pins -sd_name $TOP -pin_names {PF_XCVR_ERM_comp_0:LANE0_RX_DATA PRBS_chk_0:data_in}

sd_connect_pins -sd_name $TOP -pin_names {PF_XCVR_ERM_comp_0:LANE0_TX_CLK_R PRBS_gen_0:clk}

sd_connect_pins -sd_name $TOP -pin_names {PF_XCVR_ERM_comp_0:LANE0_TX_CLK_R Reset_Block_0:TX_clk}

sd_connect_pins -sd_name $TOP -pin_names {PF_XCVR_ERM_comp_0:LANE0_RX_CLK_R PRBS_chk_0:clk}

sd_connect_pins -sd_name $TOP -pin_names {PF_XCVR_ERM_comp_0:LANE0_RX_CLK_R FIFO_CDC_0:WCLOCK}

sd_connect_pins -sd_name $TOP -pin_names {PF_XCVR_ERM_comp_0:LANE0_RX_CLK_R Reset_Block_0:RX_clk}

sd_connect_pins -sd_name $TOP -pin_names {PF_XCVR_ERM_comp_0:LANE0_RX READY Reset_Block_0:RX_ready}

sd_connect_pins -sd_name $TOP -pin_names {PF_XCVR_ERM_comp_0:LANE0_RX_VAL PRBS_chk_0:rx_val}

sd_connect_pins -sd_name $TOP -pin_names {PF_XCVR_ERM_comp_0:LANE0_TX_CLK_STABLE Reset_Block_0:TX_clk_stable}

sd_connect_pins_to_constant -sd_name $TOP -pin_names {PF_XCVR_ERM_comp_0:LANE0_PCS_ARST_N} -value {VCC}

sd_connect_pins_to_constant -sd_name $TOP -pin_names {PF_XCVR_ERM_comp_0:LANE0_PMA_ARST_N} -value {VCC}

sd_mark_pins_unused -sd_name $TOP -pin_names {PF_XCVR_ERM_comp_0:LANE0_RX_IDLE}

sd_mark_pins_unused -sd_name $TOP -pin_names {PF_XCVR_ERM_comp_0:LANE0_RX_BYPASS_DATA}

sd_create_pin_slices -sd_name $TOP -pin_name {FIFO_CDC_0:DATA} -pin_slices [{31:0} [32:32] [33:33] [34:34]]

sd_create_pin_slices -sd_name $TOP -pin_name {FIFO_CDC_0:Q} -pin_slices [{31:0} [32:32] [33:33] [34:34]]

sd_connect_pins_to_constant -sd_name $TOP -pin_names {FIFO_CDC_0:WE} -value {VCC}

sd_connect_pins_to_constant -sd_name $TOP -pin_names {FIFO_CDC_0:RE} -value {VCC}

sd_mark_pins_unused -sd_name $TOP -pin_names {FIFO_CDC_0:FULL}
sd_mark_pins_unused -sd_name $TOP -pin_names {FIFO_CDC_0:EMPTY}

sd_connect_pins -sd_name $TOP -pin_names {UART_INTERFACE_0:CLK
PF_CCC_comp_0:OUT0_FABCLK_0}

sd_connect_pins -sd_name $TOP -pin_names {UART_INTERFACE_0:RESET_N
Reset_Block_0:uart_rst_n]

sd_connect_pins -sd_name $TOP -pin_names {UART_INTERFACE_0:clear
PF_CCC_comp_0:clr_err_counter}

sd_connect_pins -sd_name $TOP -pin_names {UART_INTERFACE_0:start
FIFO_CDC_0:RESET}

sd_connect_pins -sd_name $TOP -pin_names {UART_INTERFACE_0:start
PRBS_chk_0:start]

sd_connect_pins -sd_name $TOP -pin_names {UART_INTERFACE_0:start
PRBS_chk_0:start]

sd_connect_pins -sd_name $TOP -pin_names {UART_INTERFACE_0:start
Reset_Block_0:Start}

sd_connect_pins -sd_name $TOP -pin_names {UART_INTERFACE_0:generate_err
PRBS_gen_0:generate_error_i}

sd_connect_pins -sd_name $TOP -pin_names {UART_INTERFACE_0:EPCS_RX_VAL
FIFO_CDC_0:Q[32]}

sd_connect_pins -sd_name $TOP -pin_names {UART_INTERFACE_0:rx_lock
FIFO_CDC_0:Q[33]}

sd_connect_pins -sd_name $TOP -pin_names {UART_INTERFACE_0:rx_error
FIFO_CDC_0:Q[34]}

sd_connect_pins -sd_name $TOP -pin_names {UART_INTERFACE_0:error_count
FIFO_CDC_0:Q[31:0]}

sd_connect_pin_to_port -sd_name $TOP -pin_name {UART_INTERFACE_0:RX}

sd_connect_pin_to_port -sd_name $TOP -pin_name {UART_INTERFACE_0:TX}

sd_mark_pins_unused -sd_name $TOP -pin_names {UART_INTERFACE_0:connect_o}

sd_connect_pins -sd_name $TOP -pin_names {PRBS_chk_0:reset
Reset_Block_0:Pattern_chk_rst_n]}

sd_connect_pins -sd_name $TOP -pin_names {PRBS_chk_0:error_out
FIFO_CDC_0:DATA[34]}

sd_connect_pins -sd_name $TOP -pin_names {PRBS_chk_0:lock FIFO_CDC_0:DATA[33]}

sd_connect_pins -sd_name $TOP -pin_names {PRBS_chk_0:rx_val_o
FIFO_CDC_0:DATA[32]}

sd_connect_pins -sd_name $TOP -pin_names {PRBS_chk_0:rx_val_o
FIFO_CDC_0:DATA[31:0]}

sd_connect_pins -sd_name $TOP -pin_names {PRBS_gen_0:reset
Reset_Block_0:Pattern_gen_rst_n]}

sd_connect_pins -sd_name $TOP -pin_names {PF_CCC_comp_0:REF_CLK_0
PF_Osc_comp_0:ROSC_160MHZ_GL}

sd_connect_pins -sd_name $TOP -pin_names {PF_CCC_comp_0:OUT0_FABCLK_0
FIFO_CDC_0:RCLOCK}

sd_connect_pins -sd_name $TOP -pin_names {PF_CCC_comp_0:OUT0_FABCLK_0
Reset_Block_0:uart_clk]}

sd_connect_pins -sd_name $TOP -pin_names {PF_CCC_comp_0:PLL_LOCK_0
Reset_Block_0:PLL_LOCK}

sd_connect_pins -sd_name $TOP -pin_names {Init_macro_0:DEVICE_INIT_DONE
Reset_Block_0:INIT_DONE}

sd_mark_pins_unused -sd_name $TOP -pin_names {Init_macro_0:FABRIC_POR_N}

sd_mark_pins_unused -sd_name $TOP -pin_names {Init_macro_0:PCIE_INIT_DONE}
sd_mark_pins_unused -sd_name $TOP -pin_names {Init_macro_0:USRAM_INIT_DONE}
sd_mark_pins_unused -sd_name $TOP -pin_names {Init_macro_0:SRAM_INIT_DONE}
build_design_hierarchy
generate_component -component_name $TOP -recursive 1
save_log -file {./test_log_file.txt}
save_project

# import constraint files
import_files 
  -io_pdc ./src/user_io.pdc
import_files 
  -fp_pdc ./src/user_fp.pdc
import_files 
  -sdc ./src/user.sdc
organize_tool_files -tool {PLACEROUTE} -file $Proj/constraint/io/user_io.pdc -file $Proj/constraint/fp/user_fp.pdc -file $Proj/constraint/user.sdc -module ${TOP}::work -input_type {constraint}
organize_tool_files -tool {VERIFYTIMING} -file $Proj/constraint/user.sdc -module ${TOP}::work -input_type {constraint}
run_tool -name {CONSTRAINT_MANAGEMENT}

# Simulations settings
import_files -stimulus "./src/stimulus/Test_PRBS.v"
build_design_hierarchy
organize_tool_files -tool {SIM_PRESYNTH} -file ./${Prjname}/stimulus/Test_PRBS.v -module ${TOP}::work -input_type {stimulus}
set_modelsim_options -use_automatic_do_file 1 -sim_runtime $SimTime 
  -tb_module_name {Test_PRBS} 
  -log_all_signals 1 
  -disable_pulse_filtering 1 
  -resolution {1ps} 
  -timeunit 1 
  -timeunit_base {ns} 
  -precision 1 
  -precision_base {ps}
run_tool -name {SIM_PRESYNTH}
catch [run_tool -name {SIM_PRESYNTH}]
save_project
save_log -file {./log_file.txt}

# run synthesis
run_tool -name {SYNTHESIZE}
puts "\nSynthesis completed successfully\n"
save_project
save_log -file {./log_file.txt}

# run Place and route
configure_tool -name {PLACEROUTE} -params {DELAY_ANALYSIS:MAX} -params {EFFORT_LEVEL:true} -params {INCRPLACEANDROUTE:false} -params {IOREG_COMBINING:true} -params {MULTI_PASS_CRITERIA:VIOLATIONS} -params {MULTI_PASS_LAYOUT:false} -params {NUM_MULTI_PASSES:5} -params {PDPR:false} -params {RANDOM_SEED:0} -params {REPAIR_MIN_DELAY:true} -params {START_SEED_INDEX:1} -params {STOP_ON_FIRST_PASS:false} -params {SLACK_CRITERIA:WORST_SLACK} -params {SPECIFIC_CLOCK:} -params {TDPR:true}

run_tool -name {PLACEROUTE}
puts "\nPnR completed successfully\n"

# Verify Timing
configure_tool -name {VERIFYTIMING} -params {CONSTRAINTS_COVERAGE:1} -params {FORMAT:XML} -params {MAX_TIMING_FAST_HV_LT:1} -params {MAX_TIMING_SLOW_LV_HT:1} -params {MAX_TIMING_SLOW_LV_LT:1} -params {MAX_TIMING_VIOLATIONS_FAST_HV_LT:1} -params {MAX_TIMING_VIOLATIONS_SLOW_LV_HT:1} -params {MAX_TIMING_VIOLATIONS_SLOW_LV_LT:1} -params {MIN_TIMING_FAST_HV_LT:1} -params {MIN_TIMING_SLOW_LV_HT:1} -params {MIN_TIMING_SLOW_LV_LT:1} -params {MIN_TIMING_VIOLATIONS_FAST_HV_LT:1} -params {MIN_TIMING_VIOLATIONS_SLOW_LV_HT:1} -params {MIN_TIMING_VIOLATIONS_SLOW_LV_LT:1}

run_tool -name {VERIFYTIMING}
run_tool -name {GENERATEPROGRAMMINGDATA}
configure_tool \n-params {back_level_protection:false} \n-params {debug_passkey:} \n-params {disable_authenticate_action:false} \n-params {disable_autoprog_iap_services:false} \n-params {disable_debug_jtag_boundary_scan:false} \n-params {disable_debug_read_temp_volt:false} \n-params {disable_debug_ujtag:false} \n-params {disable_ext_zeroization:false} \n-params {disable_external_digest_check:false} \n-params {disable_jtag:false} \n-params {disable_program_action:false} \n-params {disable_puf_emulation:false} \n-params {disable_smartdebug_debug:false} \n-params {disable_smartdebug_live_probe:false} \n-params {disable_smartdebug_snvm:false} \n-params {disable_spi_slave:false} \n-params {disable_user_encryption_key_1:false} \n-params {disable_user_encryption_key_2:false} \n-params {disable_verify_action:false} \n-params {fabric_update_protection:open} \n-params {security_factory_access:open} \n-params {security_key_mode:custom} \n-params {snvm_update_protection:open} \n
-params
{user_encryption_key_1:6F70FA7580F3C25AAFF87D42C759EB20CF419C8187E7A14A6B99F40681ABEC0F} \ 
-params
{user_encryption_key_2:87A1C07AC6E4EBC33BD9B3F56EBAAD62DCDD55FA602F2654EBA55E33F62F5D} \ 
-params
{user_passkey_1:BFC4AA7B2A46CBB03AF52A8001FD170DF8B0680E7DB98CA8583A4C613ACC777} \ 
-params
{user_passkey_2:8F2F1A3A582FBA6AFA35C98C853D0AF341D25433D55D2950ADF31983CE21D3477} 
configure_tool \ 
-name {SPM_OTP} \ 
-params {permanently_disable_debugging:false} \ 
-params {permanently_disable_dpk:false} \ 
-params {permanently_disable_factory_access:false} \ 
-params {permanently_disable_prog_interfaces:false} \ 
-params {permanently_disable_upk1:true} \ 
-params {permanently_disable_upk2:false} \ 
-params {permanently_write_protect_fabric:false} 
run_tool -name {GENERATEPROGRAMMINGFILE} 
export_bitstream_file \ 
-file_name {NativePMA_Prbs} \ 
-export_dir {X:\10_docs_review\12.0_Release\sd_tcl\tcl_reference_manual_examples\g5\DG0759_pma\designer\NativePMA_Prbs\export} \ 
-format {STP DAT SPI} \ 
-master_file 1 \ 
-master_file_components {SECURITY FABRIC SNVM} \ 
-encrypted_uek1_file 1 \ 
-encrypted_uek1_file_components {FABRIC SNVM} \ 
-encrypted_uek2_file 1 \ 
-encrypted_uek2_file_components {FABRIC SNVM} \ 
-trusted_facility_file 0 \ 
-trusted_facility_file_components {} \ 
-zeroization_likenew_action 0 \ 
-zeroization_unrecoverable_action 0 \ 
-master_backlevel_bypass 0 \ 
-uek1_backlevel_bypass 0 \ 
-uek2_backlevel_bypass 0 \ 
-master_include_plaintext_passkey 0 \ 
-uek1_include_plaintext_passkey 0 \ 
-uek2_include_plaintext_passkey 0 
export_prog_job \ 
-job_file_name {NativePMA_Prbs} \

-export_dir
{X:\10_docs_review\12.0_Release\sd_tcl\tcl_reference_manual_examples\g5\DG0759_pma\designer\NativePMA_Prbs\export} \n-bitstream_file_type {UEK1} \n-bitstream_file_components {FABRIC SNVM} \n-zeroization likeness_new_action 0 \n-zeroization unrecoverable_action 0 \n-program_design 1 \n-program_spi_flash 0 \n-include Plaintext passkey 0
puts "\nDesign passed Full flow\n"