Programming and Debug Tools v12.0

Release Notes

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Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision 1.1

Revision 1.1 includes the following updates (01/24/2019):

- Added known issue in section 4.1.1.
- Updated requirements for CentOS in section 5.

Revision 1.0

Revision 1.0 was the first publication of this document.

Contents

1   Programming and Debug Tools v12.0 Release Notes

Microsemi's Programming and Debug Tools installer is intended for laboratory and production environments where Libero is not installed, and allows you to install the following tools:

- FlashPro Express
- SmartDebug Standalone
- Job Manager

1.1   Important Software and Silicon Support Changes

1.1.1   Removal of 130nm Flash-based FPGA support

Programming and Debug Tools v12.0 does not support the following 130nm Flash-based FPGA and SoC device families:

- ProASIC3 (including RT ProASIC3)
- ProASIC3E
- ProASIC3L
- IGLOO
- IGLOOe
- IGLOO +
- Fusion
- SmartFusion

Note: Programming and Debug Tools v11.9 service packs will continue to support all the above 130nm Flash-based FPGA and SoC device families, as well as IGLOO2, SmartFusion2, and RTG4 (both Classic and Enhanced Constraint Flows). However, the v11.9 software branch is in maintenance mode, and only critical bug fixes will be made going forward.

1.1.2   Removal of FlashPro Programming Software

Starting with Programming and Debug Tools v12.0, the FlashPro software will no longer be included in the Libero design software nor will it be available in standalone mode. Microsemi will be supporting the FlashPro Express v12.0 programming software, which replaces the FlashPro programming software. The last versions of Libero that include FlashPro are Libero SoC v11.9 and Libero SoC PolarFire v2.3.

Users working with Programming and Debug Tools v12.0 who would like to use FlashPro standalone programming software can export a STAPL file from v12.0 and program the FPGA using standalone versions of FlashPro v11.9 or FlashPro PolarFire v2.3.

2   What's New in Programming and Debug Tools v12.0

2.1   Programming

2.1.1   SmartFusion2 and IGLOO2 SPI-Slave Programming

FlashPro Express v12.0 supports SPI-Slave Programming for SmartFusion2 and IGLOO2 families.

Note: PolarFire SPI-Slave programming will be supported in a future release. RTG4 does not support SPI-Slave programming.

2.1.2   Export Pass Keys in Plaintext

The user can explicitly select to include plaintext pass keys, if desired. By default, all exported bitstream files will not include plaintext pass keys.

Bitstream files which include plaintext pass keys should only be used in trusted environments. FlashLock/Pass keys are needed if the bitstream file is targeted to update a feature that is FlashLock/Passkey protected.

Note: Prior to the Programming and Debug Tools v12.0 release, exported _master bitstream files and exported _uek1/_uek2 bitstream files that had either sNVM/Fabric pass key protected or Program, Authenticate and Verify actions locked included plaintext pass keys.

2.1.3   Secure Production Programming Support (SPPS)

Programming and Debug Tools v12.0 adds Secure Production Programming Support for PolarFire.

2.1.4   SmartDebug

FPGA Hardware Breakpoint Enhancements

Libero SoC v12.0 adds FPGA Hardware Breakpoint Auto Instantiation (FHB) support for the RTG4 and PolarFire FPGA families.

In addition, for all supported families, the following enhancement to FHB have been added:

- The number of clock cycles supported for VCD capture has been increased to a maximum of 1,000

PolarFire Silicon Debug Enhancements

Continuing the work to provide a state-of-the-art on-chip FPGA debug tool, this release of SmartDebug includes the following enhancements targeting the PolarFire device family:

- PCIE Debug: The PCIe Debug page shows the following content of the PCIe link used in the design
  - LTSSM state of the PCIe link
  - PCIE lane status and lane link error status
  - PCIe configuration space

- Transceiver Eye Monitor enhancements
  - Three eye plot modes are now supported in Libero SoC v12.0: Normal mode (single eye plot), Infinite Persistence mode (eye plot over a period of time until halted by user), and Design initiated eye plot

3 Resolved Issues

The following table lists the customer-reported SARs resolved in Programming and Debug Tools v12.0. Resolution of previously reported "Known Issues and Limitations" is also noted in this table.

3.1 List of Resolved Issues

Case Number	Description
493642-2521157111	Program action should detect MPF300ES or XT devices
493642-2474396566	Documentation: Remove FlashLock/UPK1 protection option of eNVM bitstream programming/verify and read (from lock spreadsheet)
493642-2474396566	Remove FlashLock/UPK1 protection option of eNVM bitstream programming/verify and read
	Device Status - if user security is programmed, eNVM protection by UEK1/2 should be displayed regardless of the lock setting
	SmartFusion2/IGLOO2 Engine: Remove FlashLock/UPK1 protection option of eNVM bitstream programming/verify and read
493642-2476865426	The JTAG voltage for IGLOO2 060 device is 3.3V
493642-2520212891	SmartDebug does not show logical memory blocks
493642-2456678571	Need support for SPI Slave programming in standalone environment (outside Libero)

4 Known Issues and Limitations

4.1 Programming

4.1.1 Programming Limitations

- The following error message is displayed when an sNVM client is not selected for programming:

  "Exit -22 Bitstream or data is corrupted or noisy"

  Workaround: Enable all sNVM clients for programming.

- The following error message is displayed when an authenticated/encrypted sNVM client is programmed in Libero:

  "Exit -22: Bitstream or data is corrupted or noisy"

  Workaround: Export a bitstream file or Export FlashPro Express Job and program the device outside of Libero using FlashPro Express, DirectC, or Auto Programming

- Updating the security or sNVM with a security-only bitstream or sNVM-only bitstream on a device that has the Fabric programmed will disable the Fabric.

  If the Fabric has been disabled, you must reprogram the Fabric to enable it.

  Workaround:
    1. sNVM only bitstreams: Field update bitstream files should always program the Fabric with sNVM.

    2. Security only bitstreams: Security only bitstream should be used on a blank device only.

- When a device is programmed with a blank Silicon Signature field, it will not get erased.

  Workaround:
    1. Specify a Silicon Signature that is not blank and program the device to change value.
    2. Perform Erase program action to erase it.

- If the USERCODE which is part of the security segment is unspecified and the security is not programmed, the previous value of USERCODE will be retained. This issue will be fixed in an upcoming release.

- Programming via SPI-Slave instead of JTAG is currently not supported. Support for this use model will be added in a future release.

- Serialization is not working for SmartFusion2 and IGLOO2 in Programming and Debug Tools v12.0.

  Serialization of the eNVM client is not working for Programming and Debug Tools v12.0.

  Workaround: Use FlashPro Express v11.9.

4.1.2 SPI Flash Programming

This release includes the following limitations:

- Only the Micron SPI Flash is currently supported with the Evaluation Kit.
- This tool erases the SPI Flash prior to programming. It is recommended to program the SPI Flash with Programming and Debug Tools v12.0 prior to programming other data on the SPI Flash using non-Libero programming solutions.

- Partial update of the SPI Flash is currently not supported.
- It is not recommended to have huge gaps between clients in the SPI Flash, since gaps are currently programmed with 1's and will increase programming times.

The following table lists the ERASE, PROGRAM, and VERIFY/READ times for different client sizes. All times are in hh:mm:ss.

Note: Depending on the SPI-Flash memory silicon version, you may observe a shorter erase time.

SPI Size	ERASE	PROGRAM	VERIFY/READ	TCK	Programmer
1 MB	00:03:55	00:00:45	00:10:46	4MHz	FP5
1 MB	00:03:55	00:00:28	00:10:05	15MHz	FP5
9 MB	00:03:55	00:06:38	01:19:15	4MHz	FP5
9 MB	00:03:55	00:04:26	01:08:49	10MHz	FP5
18 MB	00:03:55	00:09:04	02:32:43	10MHz	FP5
128 MB	00:03:55	00:58:38	22:07:55	15MHz	FP5

4.1.3 sNVM write fails due to ROM client created by previous design

In the scenario where a PolarFire device is first programmed with a design with an sNVM client, and then reprogrammed with a (different) design without an sNVM client, upon completion of programming with the second design, the sNVM client will not be erased. In such a case, if there are sNVM pages that are locked, writes to those pages will fail.

There is no programming action to erase the sNVM completely.

Workaround: Create a dummy sNVM client (filled with 0's) in the second design.

4.1.4 Zeroization Security warnings for MPF300XT/TES/TSES devices

For Libero SoC v12.0 projects targeting the MPF300XT/TES/TSES devices, while running the Export Bitstream or Export FlashPro Express Job step, unexpected zeroization security warnings are shown, even though zeroization is not supported on these devices. These warnings can be ignored and will be removed in an upcoming release.

4.2 SmartDebug

4.2.1 General SmartDebug Limitations

- Initializing RAM blocks with random values in the Design Initialization Data and Memory tool will result in SmartDebug displaying incorrect values for zeroed memory blocks.

- The logical view cannot be reconstructed for:
  - LSRAM/uSRAM for port widths of x1 inferred through RTL.

- LSRAM/uSRAM configurations when a single net of an output bus is used and others are unused. i.e. A_DOUT[0]/B_DOUT[0] for DPSRAM/uSRAM and RD[0] for TPSRAM. In this scenario, the memories can be read/write using physical view.

- LSRAM/uSRAM configurations inferred using CoreAHBLtoAXI (Verilog flow), CoreFIFO (Verilog and VHDL flow).

- HDL modules inferring RAM blocks that are instantiated in SmartDesign.

  Workaround: There are no workarounds for the issues above at this time.

- Running Probe insertion from SmartDebug on an MPF500T device results in a tool crash. This issue will be fixed in an upcoming release.

4.2.2   PolarFire Transceiver Support Limitations

- Optimize receiver on a Transceiver lane is disabled in SmartDebug. Receiver calibration(DFE) through SmartDebug is not supported in this release. The following Receiver calibration use cases are affected:
    - Transceiver lanes configured in DFE mode with XCVR universal workaround solution disabled
    - SmartBERT lanes configured to use DFE
    - Receiver change from CDR to DFE by modifying signal integrity parameters in SmartDebug

  The PolarFire MPF100T/TS/TLS, MPF200T/TS/TLS, MPF300T/TS/TLS devices are affected by the above issue

- Plot Eye introduces a burst of errors in data traffic on Transceiver Interface lanes when started. This will be fixed in an upcoming Libero SoC PolarFire release.

  Workaround: Enable Eye Monitor using the Power On Eye Monitor option before starting the traffic. This will power on the DFE and EM receivers in CDR mode and no spurious errors will be seen during eye plot.

- The Custom DFE solution (using the Optimize DFE option in the Eye Monitor tab) does not work when the transceiver is configured in 8B10B PCS-PMA mode and the receiver is DFE.

  Workaround: Perform the following steps to obtain the expected eye output:

    1. Assert PCS RX RESET
    2. Optimize DFE
    3. Plot Eye
    4. De-Assert PCS RX RESET

- The SmartBERT IP does not work when lanes are configured at 250Mbps data rate.
- SmartBERT IP PRBS tests take more time to start/stop/inject error on RHEL 7.x and Cent OS 7.x platforms as compared to RHEL 6.x and Windows OS. This issue is seen only with PRBS patterns from the SmartBERT IP, and will be fixed in upcoming Libero SoC release.
- During the Static Pattern Transmit operation, the Receiver PLL (RX PLL) does not lock to the max run length pattern when looped back from TX to RX.
- SmartBERT IP PRBS tests do not work when the first Transceiver lane uses an internal pattern (PRBS from XCVR PMA) and the following lane uses a SmartBERT pattern (PRBS from SmartBERT IP).
- When multiple lanes are specified for DFE Calibration through SmartDebug, the optimize_receiver Tcl command will fail if RX_CTLE (from read back flow) is not found for any of the lanes. This will result in incomplete calibration of other lanes.
- The Power ON eye monitor Tcl command (eye_monitor_power) does not work correctly in Libero SoC v12.0. The Receive PLL does not lock to the incoming data after this Tcl command is run. This will be fixed in an upcoming Libero SoC release.

  Workaround: There are no workarounds for the issues above at this time.

4.2.3   PolarFire Signal Integrity Support Limitations

- The RX Polarity Signal Integrity parameter (Polarity P/N reversal) has no effect when a PDC file is imported using the Import option in SmartDebug. This flow works without errors in GUI mode. This will be fixed in an upcoming Libero SoC release.
- When the TX amplitude and RX CTLE parameters are changed in the SmartDebug Signal Integrity tab, BMR (Burst Mode Receiver) designs will fail to work.

4.2.4   RTG4 FPGA Hardware Breakpoint (FHB) limitations

- For designs that instantiate certain macros in HDL, Synthesis fails during FHB auto-instantiation. For example, Synthesis fails for FHB auto-instantiation flow for designs where FCCC modules are instantiated in RTL files.

- Live Probe channel assignment using a static signal (connected to GND) halts the DUT. If this occurs, initiate the Soft Reset operation using the FHB UI to restart the DUT.

- Halting a clock domain driven by a CCC will also halt all clock domains that are driven by all the CCCs in the design. This is silicon limitation.

- FHB is not supported for cascaded CCC's (CCCs that rely on other CCC outputs to source the reference/feedback clocks)

4.2.5   Standalone SmartDebug Limitations

- Microsemi devices present in chain along with non-Microsemi devices cannot be debugged using standalone SmartDebug. In addition, the ID code of Microsemi devices cannot be read in this scenario.
  Workaround: Use SmartDebug through the Libero flow to perform these operations.

- Programming fails for RTG4 devices when a standalone SmartDebug project is created using the "Construct Chain Automatically" option, and a DDC file is imported in the Programming Connectivity and Interface dialog.
  Workaround: Import the programming file(STAPL) of the device in the Programming Connectivity and Interface dialog instead of the DDC file. This will be fixed in an upcoming Libero SoC release.

4.3   Secure Production Programming Solution

4.3.1   SPPS: New JDC file need to be generated if eNVM is set to be protected by passkey, using pre-v12.0 Libero SoC

eNVM update protection with FlashLock is not supported. eNVM update is protected by User Encryption Keys (UEK1, UEK2 or UEK3).

Regenerate the JDC file without eNVM FlashLock Protection enable.

4.3.2   SPPS: Job Manager crashes when opening an existing Job Manager project from v11.9

Job Manager v12.0 does not support Job Manager project files created with releases prior to v12.0.

4.3.3   SPPS: Job Manager does not support PolarFire DAT export

PolarFire DAT file bitstream export from Job Manager is not supported in Programming and Debug Tools v12.0.

4.3.4   SmartFusion2/IGLOO2: eNVM update protection with FlashLock is no longer supported

Due to a silicon limitation, eNVM update protection with FlashLock has been defeatured. If a JDC file generated with a pre-12.0 version of Libero SoC had the eNVM set to be protected by passkey, it must be regenerated with Libero SoC v12.0 without eNVM FlashLock Protection enabled. eNVM update protection continues to be provided by User Encryption Keys (UEK1, UEK2 or UEK3).

4.3.5   ERASE Action failure for FlashPro Express Job

If a HSM FlashPro Express job has tickets for PROGRAM and ERASE actions, without a ticket for the VERIFY action, the ERASE action will fail. To successfully run the ERASE action, ensure that a ticket for the VERIFY action is included. This issue will be fixed in an upcoming release.

5 System Requirements

The Programming and Debug Tools v12.0 release has the following system requirements:

- 64-bit OS
    - Windows 7, Windows 8.1, or Windows 10 OS
    - RHEL 6.6 or later, RHEL 7, CentOS 6.6 or later, or CentOS 7.0-7.5
- A minimum of 32 GB RAM

Note: Setup instructions for using Programming and Debug Tools v12.0 on Red Hat Enterprise Linux OS or CentOS are available here. As noted in that document, installation step 2 now includes running a shell script (bin/check_linux_req.sh) to confirm the presence of all required runtime packages.

6 Programming and Debug Tools v12.0 Download

Click the following links to download Programming and Debug Tools v12.0 on Windows and Linux operating systems:

- Windows Download
- Linux Download
- Mega Vault Download

Note: Installation requires administrator privileges to the system.