Libero SoC v12.1

Release Notes

7/2019

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Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision 1.5

Revision 1.5 includes the following changes (7/8/19):

- Added RTG4 features from Libero SoC V 11.9 SP3 in sections 1.3.5, 1.3.6, 1.3.7, 1.3.8, and 1.3.9.
- Added resolved issues from Libero SoC v11.9 SP3 in section 3.1.
- Added known issues from Libero SoC v11.9 SP3 in section 3.1.

Revision 1.4

Revision 1.4 includes the following change):

- Removed resolved issue (case number 493642-1826645965) in section 3.1.
- Added known issue in section 4.2.
- Added known issue in section 4.15.6.

Revision 1.3

Revision 1.3 includes the following changes:

- Added resolved issue in section 3.1.
- Added known issue in section 4.2.
- Added known issue in section 4.4.2.
- Updated download links in section 6.

Revision 1.2

Revision 1.2 includes the following changes:

- Removed resolved issue (case number 493642-2582927771) in section 3.1.
- Added resolved issue in section 3.1.

Revision 1.1

Revision 1.1 includes minor text edits for clarity.

Revision 1.0

Revision 1.0 was the first publication of this document.

Contents

1 Libero SoC v12.1 Software Release Notes

The Libero® system on chip (SoC) v12.1 unified design suite is Microchip's flagship FPGA software, for designing with Microsemi's latest power efficient flash FPGAs, SoC FPGAs, and rad-tolerant FPGAs. The suite integrates industry standard Synopsys Synplify Pro® synthesis and Mentor Graphics ModelSim® simulation with best-in-class constraints management, debug capabilities, and secure production programming support.

Use Libero SoC v12.1 for designing with Microsemi's RTG4 Rad-Tolerant FPGAs, SmartFusion®2 and IGLOO® 2® SoC FPGAs, and PolarFire FPGAs.

To design with Microsemi's older Flash FPGA families, use Libero SoC v11.9 and subsequent service packs.

To access datasheets, silicon user guides, tutorials, and application notes, visit www.microsemi.com, navigate to the relevant product family page, and click the **Documentation** tab. Development Kits & Boards are listed in the **Design Resources** tab.

1.1 New Device Support

Libero SoC v12.1 includes the following enhancements for PolarFire devices:

- Production timing and power support for the following devices:
  - MPF100T/S/TS (1.0V)
  - MPF200T/S/TS (1.0V)
  - MPF300T/S/TS (1.0V)
- Preliminary timing and power support for all other production PolarFire devices
- The MPF300T-1FCG1152E device is now supported with a Gold license; in previous releases, this device required a Platinum license.

1.2 Design Performance and Runtime Improvements

Libero SoC v12.1 includes the following runtime enhancements:

- 15% runtime reduction in High Effort Place and Route for PolarFire
- A significant runtime reduction in Min delay Repair, for those designs that require it

1.3 New Software Features and Enhancements

1.3.1 Place and Route

For the PolarFire device family, the Place and Route tool has been enhanced to automatically use dedicated I/O to global routing resources to improve clock insertion delays.

1.3.2 Programming

Libero SoC v12.1 adds the new Production Programming Data (PPD) file format as a bitstream file type:

- You can now export PPD files from Libero, in the Handoff Design for Production subtree.
- Job files can now contain PPD files or STP files; both types are compatible with FlashPro Express v12.1. PPD files are smaller in size than STP files. For JTAG programming, you can choose to include either a PPD or STP file. However, for SPI-Slave programming, the PPD file will be selected by default.

For designs with security/permanent lock settings, the settings are automatically exported to one of the following reports under the designer/<design> folder:

- security_summary.log – for settings in Configure Security
- permanent_locks_security_summary.log – for settings in Configure Permanent Locks for Production

1.3.3 PolarFire Design Initialization Data and Memory Report

New for this release is the Design Initialization Data and Memory Report, which details all sNVM, uPROM and SPI FLASH clients in a PolarFire design. This report can be exported to a user-specified location from the Handoff Design for Production section in the Libero Design Flow window.

1.3.4 RTG4 SET Mitigation Report

For the RTG4 device family, the new Single Event Transient (SET) Mitigation Report details the state of SET Mitigation for all sequential elements in the design, including flip-flops and RAM blocks. The report is automatically generated upon completion of the Synthesis or Compile step, and can be found within the project folder location shown below. The report is available in both text format (.rpt) and a CSV format for importing into a spreadsheet.

<libero project>/designer/<root>/<root>_compile_netlist_set_mitigation.rpt(.csv)

1.3.5 RTG4: Dynamic on-die termination (ODT) Access per I/O Bank

RTG4 production devices support the Dynamic ODT I/O attribute setting. Libero SoC v12.1 provides the RTG4_ODT_DYNAMIC core that can be instantiated for each I/O bank requiring dynamic ODT control.

The RTG4_ODT_DYNAMIC core grants access to the I/O bank-level dynamic on-die termination (ODT) control signal, and provides a single, active-low input signal, An. When An is '0', it enables the Dynamic ODT setting for the selected I/O bank and specifically any user I/Os configured to use dynamic ODT. Any I/O within the bank with I/O attributes set to ODT_STATIC = OFF and ODT_DYNAMIC = ON will have the ODT resistor turned on (An = '0') or off (An = '1') dynamically during design operation. The ODT value will match the selected value in the I/O Editor, if the I/O standard supports configurable ODT values, or default to the only supported value for I/O standards supporting a single ODT value. I/Os within the bank which are configured with ODT_DYNAMIC = OFF will not be affected by the value of input An.

Dynamic ODT supports the following I/O standards:

- LVDS, RSDS, MINILVDS, LVPECL, HSTLI, HSTLII, SSTL15I, SSTL15II, SSTL18I, SSTL18II, HSTL18I, HSTL18II, LPDDRI, LPDDRII

Note: The DDRIO banks can support this feature, but not when the FDDR controller is instantiated on the same bank. FDDR controller PHY takes priority over the An fabric input to the Dynamic ODT core.

For more information, see the following documents:

- RTG4 Macro Library Guide
- PDC Commands User Guide

1.3.6 RTG4: Weak Pullup/pulldown Resistor for Differential Inputs

Libero SoC v12.1 enables optional weak pullup/pulldown resistor attributes on input I/Os for the following differential I/O standards in RTG4 designs.

- LVDS, RSDS, MINILVDS, LVPECL

Note: When the weak pullup resistor I/O attribute is applied to PADP of a differential I/O, the I/O Editor shows pullup for both PADP and PADN, but PADN will be correctly pulled down.

1.3.7 RTG4: LVDS Fail-safe Solution

Libero SoC v12.1 enables RTG4 designs to create an internal LVDS fail-safe solution. This configuration uses a combination of the above new features:

- Dynamic on-die-termination (ODT) access per I/O bank
- Weak pullup/pulldown Resistor for differential inputs

When the LVDS input temporarily floats during operation, there is a new bank-level input signal that can dynamically turn off the on-die termination resistor so that each leg of the LVDS pair will only see the weak pullup and pulldown resistor enabled, creating an LVDS fail-safe input.

The RTG4_ODT_Dynamic core should be instantiated for each bank which requires any LVDS fail-safe I/O.

The LVDS inputs which could float need to “subscribe” in the I/O Editor to join the group of inputs affected by the RTG4_ODT_Dynamic core input for the I/O bank selected. Enable the weak pullup resistor I/O attribute on PADP of the LVDS I/O. PADN will be weakly pulled down automatically. During normal operation, the internal ODT should be present for the LVDS receiver. During fail-safe, drive *An* = ‘1’ to disable ODT.

For more information, see the following document:

- UG0741: RTG4 FPGA I/O User Guide

1.3.8 RTG4: LSRAM BLK Select Deassertion Circuit for Pipelined ECC

The RTG4 Two-Port and Dual-Port LSRAM configurators in Libero SoC v12.1 have been updated to generate an additional circuit for the pipelined-ECC mode.

- This change only applies to pipelined-ECC LSRAM components generated from the IP catalog. Manually instantiated LSRAM instances will need to migrate to the respective configurator.
- The additional circuit avoids a hold time issue by delaying BLK select de-assertion to each LSRAM block.
- Note: Single-depth Dual-port LSRAM which uses the BLK select input will no longer hold the most recent Read-data after de-asserting REN. Read-data output is gated by the pipelined BLK select input, and thus Read-data will output zero after the valid read.

To insert the additional circuit, existing designs (pre-Libero SoC v11.9 SP3) must update to Libero SoC v12.1 and regenerate any LSRAM components with pipelined-ECC mode.

- An existing design opened in Libero SoC v11.9 SP3 will be invalidated if it contains any pipelined-ECC LSRAM component and you will be asked to regenerate the affected LSRAMs.
- Compile will generate an error if pipelined-ECC LSRAM catalog components still require regeneration.
- You must rerun Static Timing Analysis to check whether the updated LSRAM component with the additional circuit still meets timing requirements.

Note: This additional circuit for the pipelined-ECC mode is also available in Libero SoC v11.9 SP3.

1.3.9 SmartFusion2, IGLOO2, RTG4: Double accounting of clock latency when applied to generated clocks

When a clock latency constraint is set on a generated clock, the Static Timing Analyzer uses the late clock latency (and respectively early clock latency) value in the calculation of the data arrival time (and respectively the data required time). However, due to an error introduced in Libero SoC v11.7.SP1, an additional delay (equal to late - early) is incorrectly added to the clock net driven by the clock source in the required time calculation.

This issue is fixed in the Libero SoC v12.1 release.

1.4 New Silicon Features and Enhancements

1.4.1 PolarFire DDR Memories

Libero SoC v12.1 upgrades the DDR3, DDR4, LPDDR3 and QDR Memory Interfaces to Production status. Updated core version numbers are provided in section 2.3.

1.4.2 PolarFire Clock Conditioning Circuitry (CCC)

Libero SoC v12.1 adds two Beta features to the PolarFire CCC:

- PLL external feedback
- PLL post-divider feedback

Note that these features are not fully validated on silicon. Libero SoC v12.1 designs that use these features may need to be changed in future releases before being used in production applications. Refer to section 4, Known Issues and Limitations for the current list of issues with the PLL feedback modes.

1.4.3 PolarFire Transceiver Solution

Libero SoC v12.1 adds the following enhancements to the PolarFire Transceiver solution:

- Transceiver Transmit PLL Jitter Attenuation support for CPRI rate 8 (64-bit)
- Transceiver and Transmit PLL preset options for 10GBASE-R/KR, SGMII, QSGMII, SDI, Interlaken, CPRI and XAUI protocols

1.4.4 PolarFire IOD CDR

Libero SoC v12.1 introduces significant changes to the IOD CDR solution:

- The new asynchronous option enables support for a reference clock offset of up to 200ppm
- The IOD CDR core must be used in conjunction with the new PolarFire IOD CDR CCC

Refer to UG0686: PolarFire FPGA User I/O User Guide for details on the new IOD CDR solution.

1.4.5 PolarFire IOD Generic Interfaces

This release adds the following enhancements to PolarFire IOD Generic Interfaces:

- **IOD Generic Receive Interfaces:** A configurable delay line option has been added to the RX_DDR_G_A/C interfaces
- **IOD Generic Transmit Interfaces:**
    - Added an option to expose the Output Enable (OE) port in bypass mode or registered mode
    - Added an option to expose dynamic delay control

1.4.6 PolarFire Memory Initialization

Libero SoC v12.1 adds the following enhancements to the Design Initialization Data and Memories configuration tool:

- An option to disable the initialization of all LSRAM and uSRAM blocks to zero at powerup. When disabled, this will reduce the Power Up to Functional time of the device, and release 17 additional sNVM pages for user clients.
- The Design Initialization Data and Memories configuration tool also provides the option to initialize specific RAM instances to zero using the new “Initialization to ‘0’ client”

2 Migrating Designs to Libero SoC v12.1

2.1 Notes on Design Migration

2.1.1 Tool Invalidation

For all PolarFire projects, after opening your project in this release, the Generate Bitstream tool will be invalidated, and must be rerun. Note that the invalidation is due to an internal format change. Bitstreams generated with Libero SoC v12.0 continue to be valid.

2.1.2 Core Invalidation

If a Libero project contains a DLL with an input frequency less than 133MHz, upon opening it with Libero SoC v12.1, the CCC configuration will be invalidated. You must reconfigure the DLL with an input frequency greater than 133MHz, regenerate the CCC component, and rerun the tool flow.

2.1.3 Core Upgrade

If a Libero SoC PolarFire v12.0 project contains the following cores, and the cores have been generated, they do not need to be upgraded upon migrating the project to Libero SoC v12.1. However, if the core needs to be generated again for any reason (for example, change in parameters), the latest version from the Catalog must be downloaded and used.

- PolarFire DDR3
- PolarFire DDR4
- PolarFire LPDDR3
- PolarFire QDR
- PolarFire SRAM (AHBLite and AXI)
- PolarFire IOD CDR
- PolarFire IOD Generic Receive Interfaces
- PolarFire IOD Generic Transmit Interfaces
- PolarFire Transceiver Interfaces
- PolarFire Transmit PLL
- PolarFire PCI Express Interfaces
- PolarFire RGMII to GMII
- PolarFire CCC

For the above cores, you must do the following:

1. Download the latest version of the core into your vault.
2. Upgrade each configured core in your design to the latest version by right-clicking on the core component in the design hierarchy and selecting ‘Replace Component Version…’.
3. Regenerate the design.
4. Rerun the Derive Constraints step.
5. Rerun the tool flow.

2.2 PolarFire Devices’ Timing and Power Data State

In this release, the timing and power data states for the MPF100T/TS/TL/TLS, MPF200T/TS/TL/TLS, and MPF300T/TS/TL/TLS devices have been upgraded to “Production”, for STD as well as -1 speed grades, at 1.0V nominal.

Note: For the 1.05V nominal operating voltage for the above devices, the Power Data State is still Preliminary, although it is shown as Production in Libero SoC v12.1 software.

The table below summarizes timing and power data state for all PolarFire devices as of Libero SoC PolarFire v12.1.

Device	Nominal Voltage	Timing Data State	Power Data State
MPF100T/TS/TL/TLS	1.0V	Production	Production
MPF100T/TS/TL/TLS	1.05V	Preliminary	Preliminary
MPF200T/TS/TL/TLS	1.0V	Production	Production
MPF200T/TS/TL/TLS	1.05V	Preliminary	Preliminary
MPF300TES/TS_ES	1.0, 1.05V	Advance	Advance
MPF300XT	1.0, 1.05V	Production	Production
MPF300T/TS/TL/TLS	1.0V	Production	Production
MPF300T/TS/TL/TLS	1.05V	Preliminary	Preliminary
MPF500T/TS/TL/TLS	All	Preliminary	Preliminary

2.3 Production Cores

Display Name	Libero SoC v12.1	Changes from Libero SoC PolarFire v12.0
PolarFire Clock Conditioning Circuitry (CCC)	1.1.101	See section 1.4.2
PolarFire Clock divider	1.0.103	None
PolarFire CoreSmartBERT	2.4.101	No functional changes Uses the latest Transceiver Interface core version
PolarFire Crypto	1.0.106	None
PolarFire DDR3	2.4.104	Improved the generated constraints to achieve 100% Derived Constraint coverage Moved to Production status Removed User Power Down Option
PolarFire DDR4	2.4.104	Added new preset: Microsemi PolarFire/Evaluation Kits/PolarFire Evaluation Kit/MPF300XT/MT40A1G8WE-083E Improved the generated constraints to achieve 100% Derived Constraint coverage Moved to Production status Removed User Power Down Option Removed READ DBI Enable option
PolarFire LPDDR3	2.3.104	Improved the generated constraints to achieve 100% Derived Constraint coverage Moved to Production status

		Removed User Power Down Option
PolarFire QDR	1.5.104	Improved the generated constraints to improve QoR Added support for half access transactions with bit width 128
PF Glitchless clock mux	1.0.101	None
PF PCI Express	2.0.102	No functional changes Modified the generated netlist to achieve 100% Constraint coverage
PF Dual-Port Large SRAM	1.1.110	None
PF Micro SRAM	1.1.107	None
PF Two-Port Large SRAM	1.1.108	None
PF uPROM	1.1.108	None
PolarFire Dynamic Reconfiguration Interface	1.0.101	None
PolarFire IOD Generic Receive Interfaces	1.2.102	See Section 1.4.5
PolarFire IOD Generic Transmit Interfaces	1.2.104	See Section 1.4.5
PolarFire IOD CDR CCC	2.0.101	New core – required for the latest IOD CDR Solution
PolarFire Initialization Monitor	2.0.103	None
PolarFire RC Oscillators	1.0.102	None
PolarFire RGMII TO GMII	1.1.107	No functional changes Updated to use latest IOD Generic core versions
PolarFire SRAM (AHBLite and AXI)	1.1.135	No functional changes Core can now be configured using Tcl
PF Tamper	1.0.107	None
PF Temperature and Voltage Sensor Interface	1.0.106	None
PF Transceiver Reference Clock	1.0.103	None
PF Transmit PLL	2.0.005	Added CPRI Rate 8 Jitter cleaner support
RTG4 Two-port Large SRAM	1.1.109	None
RTG4 Dual-port Large SRAM	1.1.106	None

2.4 Pre-Production Cores

Display Name	Libero SoC v12.1	Changes from Libero SoC PolarFire v12.0
PolarFire IOD CDR	2.1.102	See section 1.4.4
PolarFire Transceiver Interface	2.0.207	See section 1.4.1
PolarFire System Services	2.2.201	None

3 Resolved Issues

The following table lists the customer-reported SARs resolved in Libero SoC v12.1. Resolution of previously reported “Known Issues and Limitations” is also noted in this table.

3.1 List of Resolved Issues

Case Number	Description
493642-1593428191, 493642-1728880212, 493642-2274343443	The eNVM data read by FlashPro/SmartDebug is not matching the data in the input file.
493642-2164708663, 493642-2220598517, 493642-2357498226	RTG4 uPROM addressing user prog space as warnings/errors/ - using ModelSim simulation
493642-2265858862	envm_init.mem file is not getting created with the proper values if Microsemi hex format is used for eNVM
493642-2386593836	TCL command to download new cores
493642-2434450086	HDLPLUS: Parameter extract error while creating a core from HDL
493642-2496543854	Log should print Reading file ./../.cfg file when running configure_ream/snvm/uprom....
493642-2514901104	PF_IOD_CDR: v1.0.210 image shown in configurator is not matching with SmartDesign components
493642-2523315704	Libero does not take the implemented design for synthesis and place and following flow if the HDLs are under new VHDL library
493642-2523315704	HDL file in new VHDL library is not setting the root automatically after building hierarchy
493642-2525018625	When running two projects in batch mode the parameter value that is set becomes same instead of different values set
493642-2527565621, 493642-2587383970	Libero Linux installer shows incorrect file system size
493642-2527865739, 493642-2572398662	-setup_only argument is not mentioned in the user guide
493642-2528399874	PF_IOD_GENERIC_TX: 1.1.106 does not have option for Dynamic Delay
493642-2540869087	Libero SoC PolarFire v2.3 MegaVault - no PolarFire Firmware driver
493642-2544111080	Add EXTEST2 instruction to STP generation to solve I/O glitch issue
493642-2545154827	ODT model missing from exported RTG4 IBIS file
493642-2550994751	Component generation in TCL flow - Repeatability issues
493642-2550994751	Importing components into Libero through TCL not working properly.
493642-2556063689	PROGRAMMING_BITSTREAM_SETTINGS is obsolete.

493642-2558949322	Provide additional information on SPI Clock divider value
493642-2566467921	Add info regarding Block Flow in Project Settings/New Project wizard
493642-2569622693	RESTRICTSPIPINS not documented under new_project
493642-2576931252	Minimum DLL Input reference frequency is 133Mhz
493642-2578493741	Warning message says error but there is no error
493642-2580431645	HDL_LANGUAGE: Segmentation fault when string size is more than 32767 in a VHDL file
493642-2584246359	Check constraints fails when there is extra space in clock name
493642-2584257149	SmartTime Slack column sort problem
493642-2593695363	Unable to open the documentation from Libero SoC v12.0 catalog for SmartFusion2 MSS (Catalog-->SF2 MSS-->Open Documentation)
493642-2594800880	When porting a design from v2.3 to v12.0, the design hierarchy results in a missing file
493642-2595165715	Missing timing path for "Clock to Output" for the registers which are combined into IOs
493642-2582923801	RTG4 Generated Clock constraint editor GUI not displaying master clock
493642-2559621344	RTG4: Two Port Memory ECC Error Flags going 'X' in x36 mode
493642-2567607057	SmartTime “Verify Timing” has a bug in fast corner
493642-2544434392	RTG4: Creation of unnecessary CDC due to derived constraints for CCC
493642-2610574861	Include all the updates made for Libero v11.9 SP3 in v12.1 Release Notes
	RTG4: LSRAM pre-synth simulation does not match correct LSRAM behavior
	RTG4: Improve placer messaging when GB0 error occurs
	RTG4: Global SET setting overrides ndc file
	Unable to open documentation for serial interfaces
	Add report with security settings (SPM and SPM OTP)
	Clarification of MSS_GPIO and other MSS peripheral timing relative to fabric
	Runtime Error during "Export SmartDebug Data"
	DPK not working when permanent settings are enabled for SmartFusion2, IGLOO2 families
	DPK not working when permanent settings are enabled for PolarFire family
	Libero reports syntax errors but syntax check on the file passes
	Synthesis error: @E: CS169 :<prjpath>\hdl\global_ctl_csr_intf.sv":36:12:36:22|Duplicate connection to named port clk
	Web installer should check available space before starting installation
	Libero for Linux crashes with executing Save As.
	Need report showing FF's with SET filtering enabled
	PCIe RTL simulation in RTG4 fails to access config space after link up
	PF_IOD_CDR: 0ppm: CDR should have eye monitor disabled
	PF_IOD_CDR: IOCDR configurator symbol does not match actual component
	PF_IOD_GENERIC_RX: Add Option for Delay Line on Clock for RX_DDR_G_A
	PF_IOD_GENERIC_RX: Clarify Fractional Aligned clock summary data
	PF_IOD_GENERIC_TX: Add option to expose OE input on generated component
	PF_QDR: CoreQDR: The BFM does not reply to half access (128-bit).
	Crash in Publish block
	Refresh issue when Generate FPGA Array Data tool is rerun with the Design And Memory Init tool kept open.
	RTG4 FDDR w/INIT - disable verbose sim
	RTG4 Programming Log: Change FCRC to Digest
	RTG4 log files do not report .mem file used for uPROM
	Synthesize step fails with SDC errors for non-work VHDL library

	Configure Permanent Security setting crashes Libero when executed from TCL script (PolarFire)
	Cannot drive a UPROM input pin from a global net
	set_clock_uncertainty behavior issue has been fixed
	RTG4 CCC: Extra ports exposed when PLL is bypassed
	VHDL RAM: Spurious message about generic ramindex

4 Known Issues and Limitations

4.1 Catalog Cores

4.1.1 Core Generation Language

In Libero SoC v12.1, the PolarFire cores listed in sections 2.3 and 2.4 generate only Verilog files, regardless of the preferred HDL language selected in the Libero project.

VHDL users desiring to simulate designs containing affected cores must use mixed-language simulation (available with ModelSim ME Pro, which is bundled with this release, and requires a Gold, Platinum, or Eval license).

4.1.2 Linux: Core generation fails in batch mode when the DISPLAY variable is not set

The following Direct Cores cannot be generated in Libero in batch mode via Tcl when the DISPLAY variable is not set on a Linux machine:

- CoreAXI4SRAM
- CoreCIC
- CoreCordic
- CoreABC
- CoreEDAC
- CoreDDS
- CoreFIFO
- CoreFFT
- CoreFIR_PF
- CoreRSDEC
- CoreRSENC

4.2 Migration

While migrating a design created with pre- Libero SoC v12.0 to Libero SoC v12.1, if PF_SRAM_AHBL_AXI core is updated to the latest version available, incorrect values are set to the AXI read Interface, AXI write Interface and AXI wrap parameters. This issue will be fixed in the upcoming Libero Soc v12.2 release.

4.3 Design Hierarchy: HDL language duplicate modules

- Opening an existing project does not show Design Hierarchy correctly when the design has duplicates between a core module and a HDL module.

  Workaround: Build the Design Hierarchy after opening the project.

- If a design has duplicates between the elaborated modules of the core and a normal HDL module, they are not shown as duplicate modules in the Design Hierarchy.
- If two different VHDL files have same signature (same inputs, outputs, and architecture), they are not detected as duplicate modules in the Design Hierarchy.

4.4 Tcl Support Limitations

Parameters for SgCore and System Builder components are not documented. To configure such cores using Tcl, do the following:

1. Use the GUI to configure the core as desired.

2. Export the core configuration Tcl description by selecting the “Export Component Description (Tcl)” action on the right-click menu of the component in the Design Hierarchy.
3. Use the exported Tcl command to create the configured core in a regular Tcl script.

Note: The below set of cores cannot be configured using Tcl; the Export Component Description (Tcl) option is thus not supported:

- SmartFusion2/IGLOO2 MSS/HPMS component
- SmartFusion2/IGLOO2 System Builder component
- RTG4 DDR memory controller with initialization (RTG4FDDRC_INIT)
- RTG4 High Speed Serial Interface 2 – EPCS and XAUI – with Initialization (NPSS_SERDES_IF_INIT)

4.5 SmartDesign

4.5.1 Modify Memory Map feature should not be used

The Modify Memory Map action used to connect peripherals to buses in the SmartDesign canvas should not be used in the Libero SoC v12.1 release. If used, Libero may crash or produce an incorrect/incomplete memory map. Connect peripherals to bus slave positions manually, as per the desired memory map.

4.5.2 Export Component Description(Tcl) issue

In some cases, when the Export Component Description(Tcl) command is executed on a SmartDesign, pin groups created by Libero are converted to Tcl and the exported Tcl script errors out when executed.

Workaround:

1. Delete the converted line(s) from the exported file.
2. Delete the created SmartDesign.
3. Re-execute the Tcl script.

4.6 Synthesis

4.6.1 MPF500T/TS/TL/TLS: encrypted blocks are limited to one top level module

To avoid Synthesis failures for Libero projects targeting the MPF500T device, ensure that each encrypted block in the design has exactly one top module. This issue also affects designs containing the Cortex-M1 IP core.

4.6.2 SynplifyPro mapping of sequential-shift to uSRAM does not support initial values

PolarFire devices do not support initial values on registers for Sequential-shift constructs mapped to uSRAMs. If an initial value is specified for a register in RTL, Synplify will ignore the value and issue a warning.

4.6.3 SynplifyPro version checking returns an error message on RHEL/CentOS 7.4

Checking the SynplifyPro version with the following command returns an error message:
synplify_pro -version -batch

```
Error creating '"Internal Error: unsupported format used in message: '
Error creating '"Internal Error: unsupported format used in message: '
N-2017.09M-SP1-1
```

Note: In Libero SoC v12.1, the dialog box where a Synthesis profile is added will display the same error message.

This error message can be safely ignored – these operating systems are supported by Libero SoC v12.1.

4.6.4 Standalone Synthesis Flow

Libero SoC v12.1 users may synthesize their design outside the Libero SoC software by using Synopsys SynplifyPro directly. When using this flow, the following additional steps are necessary to successfully synthesize and implement a design:

- Ensure that the <install location>/Designer/data/aPA5M/polarfire_syn_comps.v is passed to SynplifyPro. This file contains module declarations with timing information for PolarFire primitives not known to Synopsys.
- Many configured cores generate timing constraints. You must ensure that these constraint files are passed to synthesis for optimal results. These constraint files must also be imported into Libero along with the synthesis gate level netlist to get optimal place and route and timing analysis results. Core generate constraint files must be modified so that constraints are expressed using the proper hierarchical name of the configured cores in the top-level design. Refer to the Custom Flow User Guide for more information.

4.7 Netlist Viewer

Opening two or more views (for example, Hierarchical RTL View and Flattened Post-Compile View) in Netlist Viewer may result in a crash due to memory usage. Avoid opening multiple views for large designs.

4.8 PolarFire Block Flow

Libero SoC v12.1 supports Block Flow. The limitation is that only Fabric components (LUT, SLE, RAM, MATH) may be instantiated in a Block. All other components (CCC, DDR, etc.) must be part of the top level design, and cannot be instantiated in Blocks.

4.9 SmartTime

4.9.1 Incorrect slack for edge-shifted generated clocks

When an edge shift is specified on a generated clock, common clock period calculation for inter-clock domains with that clock may fail. In such cases, slack calculated for these inter-clock domains will be incorrect in the Max Timing Analysis Report.

4.10 IBIS Models

For PolarFire devices, the LVDS IBIS models have undesired swing in common model voltage, but the differential voltage is correct.

Refer to section 3.5 in ER0218: PolarFire FPGA Production Devices Errata for more information.

4.11 SSN Analyzer

For all PolarFire MPF300T/TS/TL/TLS -FCG1152 devices, SSN Analyzer simulated data deviates from the Silicon measured data. This deviation can be between 20%-60%.

4.12 Post-layout simulation is not supported for PolarFire

Post-layout simulation is not supported for PolarFire devices in the Libero SoC v12.1 release.

4.13 PolarFire Silicon Support Limitations

4.13.1 PLL

- Bypass option on output clocks is not available in this release.
- PLL External feedback mode limitations: As of Libero SoC v12.1, the PLL External feedback mode feature is in Beta status, and has the following limitations:
  - Timing analysis is not supported if the PLL is configured to use the delay line in the feedback path in external feedback mode. This will be fixed in a future release.
  - The PLL Lock does not assert in Post Synthesis Simulation.
  - PLL Post-divider and External feedback modes should not be used for the MPF300XT or MPF300TS_ES devices, even though the CCC configurator allows this.

4.13.2 PCIe

- During BFM simulation of the PCIe AXI interface (master or slave), the simulator may print warning messages about AHB signals, such as “HRESP”. The warning message can be ignored.
- When the PCI Express Interface is configured in single lane mode (X1), the GUI incorrectly exposes the RXD and TXD ports for two lanes. The ports for the extra lane can be ignored.

4.13.3 Transceiver

- For the MPF300XT, MPF300TES and MPF300TSES devices, the TX_ELEC_IDLE and TX_BYPASS_DATA signals are nonfunctional and must always be tied-off to “GND’.

4.13.4 Transceiver Reference Clock

- Enabling on-die-termination and external VREF on the Transceiver Interface Reference Clock I/O is not supported in the I/O editor. However, these options can be set in the I/O PDCfile.
  Refer to UG0688: PDC Commands User Guide (SmartFusion2, IGLOO2, RTG4) or UG0715: PDC Commands User Guide (PolarFire) for more information.
- The connection from the Transceiver Interface Reference Clock I/O to the South-East PLL for all the reference clocks associated with Transceiver Interface Quad 0,2 and 4 lanes is missing in the software. Place and Route will fail if this connection is attempted.

4.13.5 I/O’s: SSTL15 On-Die Termination values are incorrectly programmed

For the MPF300XT/TES/TSES devices, when the ODT value for an SSTL15 I/O is selected as 20 Ohm or 30 Ohm, an incorrect setting is programmed

Workaround: Do not use the 20 or 30 Ohm on-die termination values for the affected devices.

4.14 Programming

4.14.1 Libero Programming

- The following error message is displayed when an sNVM client is not selected for programming:
  “Exit -22 Bitstream or data is corrupted or noisy”
  Workaround: Enable all sNVM clients for programming.

- Updating the security or sNVM with a security-only bitstream or sNVM-only bitstream on a device that has the Fabric programmed will disable the Fabric.

  If the Fabric has been disabled, you must reprogram the Fabric to enable it.

  Workaround:

  1. sNVM only bitstreams: Field-update bitstream files should always program the Fabric with sNVM.
  2. Security only bitstreams: Security-only bitstream should be used on a blank deviceonly.

- When a device is programmed with a blank Silicon Signature field, it will not get erased.

  Workaround:

  1. Specify a Silicon Signature that is not blank and program the device to change the value.
  2. Perform the Erase program action to erase it.

- A SPI file that contains a Silicon Signature setting (set in Configure Programming Options) cannot be imported as a SPI bitstream file for a Recovery/Golden client (in the SPI Flash configurator).

  Workaround: Use Libero SoC v12.0 software.

- If the USERCODE that is part of the security segment is unspecified and the security is not programmed, the previous value of USERCODE will be retained.

- Device Programming using Libero SoC v12.1 via SPI-Slave instead of JTAG is currently not supported. Support for this use model will be added in a future release.

- Serialization of the eNVM client is not working for Libero SoC v12.1.

  Workaround: Use Libero SoC v11.9.

- FlashPro Express does not support SPI-Flash only programming in a JTAG chain with SmartFusion2/IGLOO2 and PolarFire devices.

4.14.2 SPI Flash Programming

This release includes the following limitations:

- Only the Micron SPI Flash is currently supported with the Evaluation Kit.
- This tool erases the SPI Flash prior to programming. It is recommended to program the SPI Flash with Libero SoC v12.1 prior to programming other data on the SPI Flash using non-Libero programming solutions.
- Partial update of the SPI Flash is currently not supported.
- It is not recommended to have huge gaps between clients in the SPI Flash, since gaps are currently programmed with 1's and will increase programming times.

  The following table lists the ERASE, PROGRAM, and VERIFY/READ times for different client sizes. All times are in hh:mm:ss.

  Note: Depending on the SPI-Flash memory silicon version, you may observe a shorter erase time.

SPI Size	ERASE	PROGRAM	VERIFY/READ	TCK	Programmer
1 MB	00:03:55	00:00:45	00:10:46	4MHz	FP5
1 MB	00:03:55	00:00:28	00:10:05	15MHz	FP5
9 MB	00:03:55	00:06:38	01:19:15	4MHz	FP5

9 MB	00:03:55	00:04:26	01:08:49	10MHz	FP5
18 MB	00:03:55	00:09:04	02:32:43	10MHz	FP5
128 MB	00:03:55	00:58:38	22:07:55	15MHz	FP5

4.14.3 sNVM write fails due to ROM client created by previous design

In the scenario where a PolarFire device is first programmed with a design with an sNVM client, and then reprogrammed with a (different) design without an sNVM client, upon completion of programming with the second design, the sNVM client will not be erased. In such a case, if there are sNVM pages that are locked, writes to those pages will fail.

There is no programming action to erase the sNVM completely.

Workaround: Create a dummy sNVM client (filled with 0's) in the second design.

4.14.4 PolarFire VERIFY_DIGEST action may fail in certain cases

The VERIFY_DIGEST step in FlashPro Express for a PolarFire device in Libero SoC v12.1 release will fail in cases where the digest check is run for segments that are not programmed.

Workaround:

Using FlashPro v2.3 (part of Libero SoC PolarFire v2.3 or Programming and Debug Tools PolarFire v2.3), load the STAPL file into FlashPro, and deselect the digest checks for segments not programmed.

4.15 SmartDebug

4.15.1 General SmartDebug Limitations

- Initializing RAM blocks with random values in the Design Initialization Data and Memory tool will result in SmartDebug displaying incorrect values for zeroed memory blocks.
- The logical view cannot be reconstructed for:
  - LSRAM/uSRAM for port widths of x1 inferred through RTL.
  - LSRAM/uSRAM configurations when a single net of an output bus is used and others are unused (i.e. A_DOUT[0]/B_DOUT[0] for DPSRAM/uSRAM and RD[0] for TPSRAM). In this scenario, the memories can be read/write using physical view.
  - LSRAM/uSRAM configurations inferred using CoreAHBLtoAXI (Verilog flow), CoreFIFO (Verilog and VHDL flow).
  - HDL modules inferring RAM blocks that are instantiated in SmartDesign.

    Workaround: There are no workarounds for the issues above at this time.

4.15.2 PolarFire Transceiver Support Limitations

- Plot Eye introduces a burst of errors in data traffic on Transceiver Interface lanes when started. This will be fixed in an upcoming Libero SoC PolarFire release.

  Workaround: Enable Eye Monitor using the Power On Eye Monitor option before starting the traffic. This will power on the DFE and EM receivers in CDR mode and no spurious errors will be seen during eye plot.

- The Custom DFE solution (using the Optimize DFE option in the Eye Monitor tab) does not work when the transceiver is configured in 8B10B PCS-PMA mode and the receiver is DFE.

  Workaround: Perform the following steps to obtain the expected eye output:

  1. Assert PCS RX RESET
  2. Optimize DFE
  3. Plot Eye
  4. De-Assert PCS RX RESET

- The SmartBERT IP does not work when lanes are configured at 250Mbps data rate.
- SmartBERT IP PRBS tests take more time to start/stop/inject error on RHEL 7.x and Cent OS 7.x platforms as compared to RHEL 6.x and Windows OS. This issue is seen only with PRBS patterns from the SmartBERT IP, and will be fixed in an upcoming Libero SoC release.
- During the Static Pattern Transmit operation, the Receiver PLL (RX PLL) does not lock to the max run length pattern when looped back from TX to RX.
- SmartBERT IP PRBS tests do not work when the first Transceiver lane uses an internal pattern (PRBS from XCVR PMA) and the following lane uses a SmartBERT pattern (PRBS from SmartBERT IP).
- When multiple lanes are specified for DFE Calibration through SmartDebug, the optimize_receiver Tcl command will fail if RX_CTLE (from read back flow) is not found for any of the lanes. This will result in incomplete calibration of other lanes.
- The Power ON eye monitor Tcl command (eye_monitor_power) does not work correctly in Libero SoC v12.1. The Receive PLL does not lock to the incoming data after this Tcl command is run. This will be fixed in an upcoming Libero SoC release.

  Workaround: There are no workarounds for the issues above at this time.

4.15.3 PolarFire Signal Integrity Support Limitations

- The RX Polarity Signal Integrity parameter (Polarity P/N reversal) has no effect when a PDC file is imported using the Import option in SmartDebug. This flow works without errors in GUI mode. This will be fixed in an upcoming Libero SoC release.
- When the TX amplitude and RX CTLE parameters are changed in the SmartDebug Signal Integrity tab, BMR (Burst Mode Receiver) designs will fail to work.

4.15.4 PolarFire FPGA Hardware Breakpoint (FHB) Limitations

- FHB is not supported when a Transceiver Interface with the Enhanced Receiver Management Solution enabled is used in a design. FHB is supported when a non-ERM Transceiver Interface is used.
- Soft Reset behavior is not consistent when the DUT is clocked at frequencies less than 160MHz. In such cases, the device may not respond to a Soft Reset operation initiated from the FHB UI. A potential workaround is to do the following:

  1. Halt the DUT via Live Probe
  2. Initiate a Soft Reset operation using the FHB UI
  3. Halt the DUT again via Live Probe

4.15.5 RTG4 FPGA Hardware Breakpoint (FHB) Limitations

- Synthesis fails when FHB auto instantiation is enabled on designs containing FCCC modules using instantiation flow (i.e. FCCC modules instantiated in RTL files).
- Live Probe channel assignment using a static signal (connected to GND) halts the DUT. If this occurs, initiate the Soft Reset operation using the FHB UI to restart the DUT.

- Halting a clock domain driven by a CCC will also halt all four clock domains belonging to the CCCs in the design. This is a silicon limitation.
- FHB is not supported for cascaded CCCs (CCCs that rely on other CCC outputs to source the reference/feedback clocks). FHB is auto-instantiated, but the PLAY/HALT/STEP operations do not work.

4.15.6 RTG4 LSRAM Data corruption

- LSRAM Data corruption is seen on doing a read to LSRAM configured in 512x36 mode through SmartDebug.

4.15.7 Standalone SmartDebug Limitations

- Microsemi devices present in chain along with non-Microsemi devices cannot be debugged using standalone SmartDebug. In addition, the ID code of Microsemi devices cannot be read in this scenario.

  Workaround: Use SmartDebug through the Libero flow to perform these operations.
- Programming fails for RTG4 devices when a standalone SmartDebug project is created using the "Construct Chain Automatically" option, and a DDC file is imported in the Programming Connectivity and Interface dialog.

  Workaround:

  1. Close and reopen the Programming Connectivity and Interface UI and then click **Run Program Action**.
  2. Create a project by importing the DDC file (without Auto-construct).
- Standalone SmartDebug User Guide fails to open when no project is created

  Workaround: To open the user guide from standalone SmartDebug, a new project must be created. This will be fixed in upcoming releases.

4.16 Secure Production Programming Solution

4.16.1 Job Manager may crash during the Import Job Status operation

Running the Import Job Status operation may cause Job Manager to crash. This may happen for designs where the User ECC Key mode is enabled, targeting SmartFusion2 or IGLOO2 M2S/M2GL060, 090, or 150 devices.

4.16.2 Job Manager crashes when opening an existing Job Manager project from v11.9

Job Manager v12.1 does not support Job Manager project files created with releases prior to v12.0.

4.16.3 Job Manager does not support PolarFire DAT export

PolarFire DAT file bitstream export from Job Manager is not supported in Libero SoC v12.1.

4.16.4 SmartFusion2/IGLOO2: eNVM update protection with FlashLock is no longer supported

Due to a silicon limitation, eNVM update protection with FlashLock has been defeatured. If a JDC file generated with a pre-v12.0 version of Libero SoC had the eNVM set to be protected by passkey, it must be regenerated with Libero SoC v12.1 without eNVM FlashLock Protection enabled. eNVM update protection continues to be provided by User Encryption Keys (UEK1, UEK2 or UEK3).

4.16.5 ERASE Action failure for FlashPro Express Job

If a HSM FlashPro Express job has tickets for PROGRAM and ERASE actions, without a ticket for the VERIFY action, the ERASE action will fail. To successfully run the ERASE action, ensure that a ticket for the VERIFY action is included.

4.17 Identify Instrumentor may hang on some Windows 10 machines

When the Identify Instrumentor is opened in Integrated mode on certain machines, the tool opens, but, upon interaction, it freezes. This is an isolated issue, and happens on rare Windows 10 OS configurations.

Workaround: Use the Standalone Identify Instrumentor.

4.18 Installation and System Limitations

4.18.1 Libero does not run on 8TB File Systems

Libero is currently only supported for partitions 2TB or smaller. If either the Libero install or the Libero project is located on a partition that is larger than 2TB, file access errors or tool crashes may occur. Support for larger partitions is expected to be added in an upcoming release.

4.18.2 4K and 8K screens are not supported

4K and 8K screens are not supported in the Libero SoC v12.1 release.

4.18.3 Installation on Local Drive Only

This release is intended for installation only on a local drive. The Installer might report permission rights problems if the release is installed across a networked drive.

4.18.4 Visual C++ Redistributable Installation Error

On some machines, the installer may display a message stating:

> "The installation of Microsoft Visual C++ Redistributable Package (x86) appears to have failed. Do you want to continue the installation?"

The above error message is benign. If it is seen, click Yes and Libero SoC v12.1 will be installed successfully.

4.18.5 Installation on Windows 7

During Libero SoC v12.1 installation on Windows 7 machines, you may see pop-up warning messages about shortcuts toward the end of installation process.

These messages can be safely ignored. Click OK to close the pop-up windows and the installation will proceed and complete as expected. All Windows shortcuts will appear correctly.

4.18.6 Installation fails when there is insufficient space

In Libero SoC v12.1, the web installer quits without any user notification or error message when there is insufficient space for the installation. In addition, the estimated space for the installation is incorrect – it reads as approximately 236MB required. Ensure that there is at least 20GB free space on the target hard drive before invoking the installer.

The DVD installer will also not proceed if there is insufficient space.

4.18.7 Windows Standalone Installer: Spaces in Extraction Path

During installation of the standalone (DVD) version, the folder to which the zip file is extracted must not contain spaces. If spaces are present, invocation of the installer will fail with the error *"Windows cannot find '<truncated path to extracted folder>'. Make sure you typed the name correctly, and then try again"* Rename and/or move the extracted folder to one without spaces (in the entire path).

4.18.8 Linux Package Note

In Libero SoC v12.1, the script bin/check_linux_req/check_linux_req.sh incorrectly reports that the Linux package xz.i686 is required for RHEL/CentOS 7.x. Package xz.i686 is not required. The correct required packages are xz-libs.x86_64 and xz-libs.i686.

4.18.9 Antivirus Software Interaction

Many antivirus and HIPS (Host-based Intrusion Prevention System) tools will flag executables and prevent them from running. To eliminate this problem, users must modify their security setting by adding exceptions for specific executables. This is configured in the antivirus tool. Contact the tool provider for assistance.

Many users are running Libero SoC PolarFire successfully with no modification to their antivirus software. Microsemi is aware of issues for some antivirus tool settings that occur when using Symantec, McAfee, Avira, Sophos, and Avast tools. The combination of operating system, antivirus tool version, and security settings all contribute to the end result. Depending on the environment, the operation of Libero SoC v12.1, ModelSim ME and/or Synplify Pro ME may or may not be affected.

All public releases of Libero software are tested with several antivirus tools before they are released to ensure that they are not infected. In addition, Microsemi's software development and testing environment is also protected by antivirus tools and other security measures.

5 System Requirements

The Libero SoC v12.1 release has the following system requirements:

- 64-bit OS
    - Windows 7, Windows 8.1, or Windows 10 OS
    - RHEL 6.6 or later, RHEL 7, CentOS 6.6 or later, or CentOS 7.0-7.5
- A minimum of 16 GB RAM

Note: Setup instructions for using Libero SoC v12.1 on Red Hat Enterprise Linux OS or CentOS are available here. As noted in that document, installation now includes running a shell script (bin/check_linux_req.sh) to confirm the presence of all required runtime packages.

6 Download Libero SoC v12.1 Software

The following are available for download:

- Libero SoC v12.1 for Linux
- Libero SoC v12.1 for Windows
- Libero SoC v12.1 MegaVault for Linux
- Libero SoC v12.1 Megavault for Windows

Note: Installation requires administrative privileges.

After successful installation, clicking **Help-> About Libero** will show Version: 12.600.0.14