Programming and Debug Tools v12.1

Release Notes

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Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision 1.2

Updated download links in section 5 (5/8/19).

Revision 1.1

Revision 1.1 includes minor text edits for clarity.

Revision 1.0

Revision 1.0 was the first publication of this document.

Contents

1 Programming and Debug Tools v12.1 Release Notes

Microsemi's Programming and Debug Tools installer is intended for laboratory and production environments where Libero SoC is not installed, and allows you to install the following tools:

- FlashPro Express
- SmartDebug Standalone
- Job Manager

This document describes the Programming and Debug Tools v12.1 release. For information about the Libero SoC v12.1 release, refer to the Libero SoC v12.1 Release Notes.

1.1 New Software Features and Enhancements

1.1.1 Programming

Programming and Debug Tools v12.1 adds the new Production Programming Data (PPD) file format as a bitstream file type:

- You can now export PPD files from Libero, in the Handoff Design for Production subtree.
- Job files can now contain PPD files or STP files; both types are compatible with FlashPro Express v12.1. PPD files are smaller in size than STP files. For JTAG programming, you can choose to include either a PPD or STP file. However, for SPI-Slave programming, the PPD file will be selected by default.

For designs with security/permanent lock settings, the settings are automatically exported to one of the following reports under the designer/<design> folder:

- security_summary.log – for settings in Configure Security
- permanent_locks_security_summary.log – for settings in Configure Permanent Locks for Production

2 Resolved Issues

The following table lists the customer-reported SARs resolved in Programming and Debug Tools v12.1. Resolution of previously reported “Known Issues and Limitations” is also noted in this table.

2.1 List of Resolved Issues

Case Number	Description
493642-1593428191, 493642-1728880212, 493642-2274343443	The eNVM data read by FlashPro/SmartDebug is not matching the data in the input file.
493642-1826645965,493642-1825092298,493642-1980430671,493642-1986322124,493642-2005176595, 493642-2141382953,493642-2356766859,493642-2392075854, 493642-2461809942,493642-2513380594	SVF file support for Smartfusion2 and IGLOO2 devices
493642-2164708663, 493642-2220598517, 493642-2357498226	RTG4 uPROM addressing user prog space as warnings/errors/ - using ModelSim simulation
493642-2265858862	envm_init.mem file is not getting created with the proper values if Microsemi hex format is used for eNVM
493642-2496543854	Log should print Reading file ./../.cfg file when running configure_ream/snvm/uprom....
493642-2556063689	PROGRAMMING_BITSTREAM_SETTINGS is obsolete.
-	Add report with security settings (SPM and SPM OTP)
	Runtime Error during "Export SmartDebug Data"
	DPK not working when permanent settings are enabled for SmartFusion2, IGLOO2 families
	DPK not working when permanent settings are enabled for PolarFire family
	Configure Permanent Security setting crashes Libero when executed from TCL script (PolarFire)
	RTG4 Programming Log: Change FCRC to Digest

3 Known Issues and Limitations

3.1 Programming

3.1.1 Libero Programming

- The following error message is displayed when an sNVM client is not selected for programming:

  "Exit -22 Bitstream or data is corrupted or noisy"

  Workaround: Enable all sNVM clients for programming.

- Updating the security or sNVM with a security-only bitstream or sNVM-only bitstream on a device that has the Fabric programmed will disable the Fabric.

  If the Fabric has been disabled, you must reprogram the Fabric to enable it.

  Workaround:

  1. sNVM only bitstreams: Field update bitstream files should always program the Fabric with sNVM.
  2. Security only bitstreams: Security-only bitstream should be used on a blank device only.

- When a device is programmed with a blank Silicon Signature field, it will not get erased.

  Workaround:

  1. Specify a Silicon Signature that is not blank and program the device to change the value.
  2. Perform the Erase program action to erase it.

- A SPI file that contains a Silicon Signature setting (set in Configure Programming Options) cannot be imported as a SPI bitstream file for Recovery/Golden client (in SPI Flash configurator).

  Workaround: Use v12.0 software.

- If the USERCODE that is part of the security segment is unspecified and the security is not programmed, the previous value of USERCODE will be retained.

- Device Programming using Programming and Debug Tools v12.1 via SPI-Slave instead of JTAG is currently not supported. Support for this use model will be added in a future release.

- Serialization of the eNVM client is not working for SmartFusion2 and IGLOO2 in Programming and Debug Tools v12.1.

  Workaround: Use Programming and Debug Tools v11.9.

- FlashPro Express does not support SPI-Flash only programming in a JTAG chain with SmartFusion2/IGLOO2 and PolarFire devices.

3.1.2 SPI Flash Programming

This release includes the following SPI Flash programming limitations:

- Only the Micron SPI Flash is currently supported with the Evaluation Kit.
- This tool erases the SPI Flash prior to programming. It is recommended to program the SPI Flash with Programming and Debug Tools v12.1 prior to programming other data on the SPI Flash using non-Libero programming solutions.
- Partial update of the SPI Flash is currently not supported.
- It is not recommended to have huge gaps between clients in the SPI Flash, since gaps are currently programmed with 1's and will increase programming times.

The following table lists the ERASE, PROGRAM, and VERIFY/READ times for different client sizes. All times are in hh:mm:ss.

Note: Depending on the SPI-Flash memory silicon version, you may observe a shorter erase time.

SPI Size	ERASE	PROGRAM	VERIFY/READ	TCK	Programmer
1 MB	00:03:55	00:00:45	00:10:46	4MHz	FP5
1 MB	00:03:55	00:00:28	00:10:05	15MHz	FP5
9 MB	00:03:55	00:06:38	01:19:15	4MHz	FP5
9 MB	00:03:55	00:04:26	01:08:49	10MHz	FP5
18 MB	00:03:55	00:09:04	02:32:43	10MHz	FP5
128 MB	00:03:55	00:58:38	22:07:55	15MHz	FP5

3.1.3 sNVM write fails due to ROM client created by previous design

In the scenario where a PolarFire device is first programmed with a design with an sNVM client, and then reprogrammed with a (different) design without an sNVM client, upon completion of programming with the second design, the sNVM client will not be erased. In such a case, if there are sNVM pages that are locked, writes to those pages will fail.

There is no programming action to erase the sNVM completely.

Workaround: Create a dummy sNVM client (filled with 0's) in the second design.

3.1.4 PolarFire VERIFY_DIGEST action may fail in certain cases

The VERIFY_DIGEST step in FlashPro Express for a PolarFire device in the v12.1 release will fail in cases where the digest check is run for segments that are not programmed.

Workaround:

Using FlashPro v2.3 (part of Libero SoC PolarFire v2.3 or Programming and Debug Tools PolarFire v2.3), load the STAPL file into FlashPro, and deselect the digest checks for segments not programmed.

3.2 SmartDebug

3.2.1 General SmartDebug Limitations

- Initializing RAM blocks with random values in the Design Initialization Data and Memory tool will result in SmartDebug displaying incorrect values for zeroed memory blocks.
- The logical view cannot be reconstructed for:
  - LSRAM/uSRAM for port widths of x1 inferred through RTL.
  - LSRAM/uSRAM configurations in which a single net of an output bus is used and others are unused. i.e. A_DOUT[0]/B_DOUT[0] for DPSRAM/uSRAM and RD[0] for TPSRAM. In this scenario, the memories can be read/write using physical view.

- LSRAM/uSRAM configurations inferred using CoreAHBLtoAXI (Verilog flow), CoreFIFO (Verilog and VHDL flow).
- HDL modules inferring RAM blocks that are instantiated in SmartDesign.

  Workaround: There are no workarounds for the issues above at this time.

3.2.2 PolarFire Transceiver Support Limitations

- Plot Eye introduces a burst of errors in data traffic on Transceiver Interface lanes when started. This will be fixed in an upcoming release.

  Workaround: Enable Eye Monitor using the Power On Eye Monitor option before starting the traffic. This will power on the DFE and EM receivers in CDR mode, and no spurious errors will be seen during eye plot.
- The Custom DFE solution (using the Optimize DFE option in the Eye Monitor tab) does not work when the transceiver is configured in 8B10B PCS-PMA mode and the receiver is DFE.

  Workaround: Perform the following steps to obtain the expected eye output:

  1. Assert PCS RX RESET
  2. Optimize DFE
  3. Plot Eye
  4. De-Assert PCS RX RESET
- The SmartBERT IP does not work when lanes are configured at 250Mbps data rate.
- SmartBERT IP PRBS tests take more time to start/stop/inject error on RHEL 7.x and Cent OS 7.x platforms as compared to RHEL 6.x and Windows OS. This issue is seen only with PRBS patterns from the SmartBERT IP, and will be fixed in an upcoming release.
- During the Static Pattern Transmit operation, the Receiver PLL (RX PLL) does not lock to the max run length pattern when looped back from TX to RX.
- SmartBERT IP PRBS tests do not work when the first Transceiver lane uses an internal pattern (PRBS from XCVR PMA) and the following lane uses a SmartBERT pattern (PRBS from SmartBERT IP).
- When multiple lanes are specified for DFE Calibration through SmartDebug, the optimize_receiver Tcl command will fail if RX_CTLE (from read back flow) is not found for any of the lanes. This will result in incomplete calibration of other lanes.
- The Power ON eye monitor Tcl command (eye_monitor_power) does not work correctly in Programming and Debug Tools v12.1. The Receive PLL does not lock to the incoming data after this Tcl command is run. This will be fixed in an upcoming release.

  Workaround: There are no workarounds for the issues above at this time.

3.2.3 PolarFire Signal Integrity Support Limitations

- The RX Polarity Signal Integrity parameter (Polarity P/N reversal) has no effect when a PDC file is imported using the Import option in SmartDebug. This flow works without errors in GUI mode. This will be fixed in an upcoming release.
- When the TX amplitude and RX CTLE parameters are changed in the SmartDebug Signal Integrity tab, BMR (Burst Mode Receiver) designs will fail to work.

3.2.4 PolarFire FPGA Hardware Breakpoint (FHB) Limitations

- FHB is not supported when a Transceiver Interface with the Enhanced Receiver Management Solution enabled is used in a design. FHB is supported when a non-ERM Transceiver Interface is used.
- Soft Reset behavior is not consistent when the DUT is clocked at frequencies less than 160MHz. In such cases, the device may not respond to a Soft Reset operation initiated from the FHB UI. A potential workaround is to do the following:

1. Halt the DUT via Live Probe.
2. Initiate a Soft Reset operation using the FHB UI.
3. Halt the DUT again via Live Probe.

3.2.5 RTG4 FPGA Hardware Breakpoint (FHB) Limitations

- Synthesis fails when FHB auto instantiation is enabled on designs containing FCCC modules using instantiation flow (i.e. FCCC modules instantiated in RTL files).
- Live Probe channel assignment using a static signal (connected to GND) halts the DUT. If this occurs, initiate the Soft Reset operation using the FHB UI to restart the DUT.
- Halting a clock domain driven by a CCC will also halt all four clock domains belonging to the CCCs in the design. This is a silicon limitation.
- FHB is not supported for cascaded CCCs (CCCs that rely on other CCC outputs to source the reference/feedback clocks). FHB is auto-instantiated, but the PLAY/HALT/STEP operations do not work.

3.2.6 Standalone SmartDebug Limitations

- Microsemi devices present in chain along with non-Microsemi devices cannot be debugged using standalone SmartDebug. In addition, the ID code of Microsemi devices cannot be read in this scenario.

  Workaround: Use SmartDebug through the Libero flow to perform these operations.
- Programming fails for RTG4 devices when a standalone SmartDebug project is created using the “Construct Chain Automatically” option, and a DDC file is imported in the Programming Connectivity and Interface dialog.

  Workaround:

  1. Close and reopen the Programming Connectivity and Interface UI and then click **Run Program Action**.
  2. Create a project by importing the DDC file (without Auto-construct).
- Standalone SmartDebug User Guide fails to open when no project is created

  Workaround: To open the user guide from standalone SmartDebug, a new project must be created. This will be fixed in an upcoming release.

3.3 Secure Production Programming Solution

3.3.1 Job Manager may crash during the Import Job Status operation

Running the Import Job Status operation may cause Job Manager to crash. This may happen for designs where the User ECC Key mode is enabled, targeting SmartFusion2 or IGLOO2 M2S/M2GL060, 090, or 150 devices.

3.3.2 Job Manager crashes when opening an existing Job Manager project from v11.9

Job Manager v12.1 does not support Job Manager project files created with releases prior to v12.0.

3.3.3 Job Manager does not support PolarFire DAT export

PolarFire DAT file bitstream export from Job Manager is not supported in Programming and Debug Tools v12.1.

3.3.4 SmartFusion2/IGLOO2: eNVM update protection with FlashLock is no longer supported

Due to a silicon limitation, eNVM update protection with FlashLock has been defeatured. If a JDC file generated with a pre-v12.0 version of Libero SoC had the eNVM set to be protected by passkey, it must be regenerated with Libero SoC v12.1 without eNVM FlashLock Protection enabled. eNVM update protection continues to be provided by User Encryption Keys (UEK1, UEK2 or UEK3).

3.3.5 ERASE Action failure for FlashPro Express Job

If a HSM FlashPro Express job has tickets for PROGRAM and ERASE actions, without a ticket for the VERIFY action, the ERASE action will fail. To successfully run the ERASE action, ensure that a ticket for the VERIFY action is included.

4 System Requirements

The Programming and Debug Tools v12.1 release has the following system requirements:

- 64-bit OS
    - Windows 7, Windows 8.1, or Windows 10 OS
    - RHEL 6.6 or later, RHEL 7, CentOS 6.6 or later, or CentOS 7.0-7.5
- A minimum of 16 GB RAM

Note: Setup instructions for using Programming and Debug Tools v12.1 on Red Hat Enterprise Linux OS or CentOS are available here. As noted in that document, installation now includes running a shell script (bin/check_linux_req.sh) to confirm the presence of all required runtime packages.

5 Programming and Debug Tools v12.1 Download

Click the following links to download Programming and Debug Tools v12.1 on Windows and Linux operating systems:

- Windows Download
- Linux Download
- Libero SoC v12.1 MegaVault for Linux
- Libero SoC v12.1 Megavault for Windows

Note: Installation requires administrative privileges.