Libero SoC v12.5 Release Notes

Introduction

The Libero® system on chip (SoC) v12.5 unified design suite is Microchip's flagship FPGA software for designing with Microsemi's latest power efficient flash FPGAs, SoC FPGAs, and rad-tolerant FPGAs. The suite integrates industry-standard Synopsys Synplify Pro® synthesis and Mentor Graphics ModelSim® simulation with best-in-class constraints management, debug capabilities, and secure production programming support.

Use Libero SoC v12.5 for designing with Microsemi's RTG4™ Rad-Tolerant FPGAs, SmartFusion®2 and IGLOO® 2 SoC FPGAs, PolarFire® FPGAs, and PolarFire SoC FPGAs.

To design with Microsemi's older Flash FPGA families, use Libero SoC v11.9 and subsequent service packs.

To access datasheets, silicon user guides, tutorials, and application notes, visit www.microsemi.com, navigate to the relevant product family page, and click the **Documentation** tab. Development Kits & Boards are listed in the **Design Resources** tab.

Note: Libero SoC v12.5 does not support Classic Constraint Flow. IGLOO2, SmartFusion2, and RTG4 projects using the "Classic" flow cannot be opened in this release. For details about how to migrate Classic Constraint Flow projects to the Enhanced Constraint Flow, refer to Migrating an Existing Project Created with Classic Constraint Flow to Enhanced Constraint Flow.

Table of Contents

1. Libero SoC v12.5 Software Release Notes

These release notes contain important information about the Libero® system on chip (SoC) v12.5 unified design suite.

1.1 Customer Notification (CN) and Customer Advisory Notification (CAN) Support

Libero SoC v12.5 includes changes that address certain important issues. For more information about these issues, refer to www.microsemi.com/company/quality/product-notifications/cn/asic-soc-fpga.

1.1.1 RT PolarFire Pin Assignment Change

DDR3 and DDR4 pin assignments of the RTPF500T-CG1509 package have been altered in Libero SoC v12.5. Place and route performed on a design with Libero SoC v12.4 will be invalidated when opened using Libero SoC v12.5.

For more information, refer to CAN20016.

1.1.2 PolarFire PF_SPI and UJTAG Timing Change

UJTAG

The timing model of most output signals from the UJTAG to the fabric were updated to be triggered on the falling edge of the clock rather than the rising edge.

From	To	Previous Triggering Edge	New Triggering Edge
TCK	UDRCAP	Rising	Falling
TCK	UDRSH	Rising	Falling
TCK	UDRUPD	Rising	Falling
TCK	UIREG [7:0]	Rising	Falling
TCK	TDI	Rising	Falling

Note: The reset signal, fab_uj_trstb, going into the fabric is now considered asynchronous. External timing checks are not included in the model.

PF_SPI

The timing model has been updated to allow proper timing checks through PF_SPI for CLK, SS, DI, DO signals.

For more information, refer to CN20018.

1.1.3 PolarFire LSRAM Configurator Asymmetric Widths

A change to PolarFire Two-port Large SRAM configurator, Dual-port Large SRAM configurator and CoreFIFO has been implemented. The LSRAM configurator engine correctly generates asymmetric width configurations and optimizes the area for High-speed and Low-power selections.

For more information, refer to CN20019.

1.1.4 PolarFire LSRAM Configurator Write Byte Enable Fragments

A change to PolarFire Two-port Large SRAM configurator and Dual-port Large SRAM configurator has been implemented. The LSRAM configurator engine for Write Byte Enable selection divides the entire width of the memory into equal fragments controlled by each Write Byte Enable bit.

For more information, refer to CN20020.

1.1.5 PolarFire LSRAM Timing Change

The following changes were made to the PolarFire LSRAM timing model:

- Adjust the minimum period requirement in SmartTime to be aligned with the datasheet by accounting for ECC/NoECC and Pipeline/Bypass.
- Update the enable signal setup/hold timing model when the LSRAM is used in the following modes: 2-port x33, ECC-Register non-pipelined, and output port pipelined.
- Update the reset signal removal/recovery timing model when the LSRAM is used in the following modes: 2-port x33, ECC-Register non-pipelined, and output port pipelined.

For more information, refer to CAN20021.

1.1.6 Timing Paths May be Missing from Static Timing Analysis (STA) for the SmartFusion2, IGLOO2, RTG4, and PolarFire Product Families

Ongoing software quality testing on Libero SoC has found minor Static Timing Analysis (STA) coverage issues, preventing complete analysis of the path through combinational cells for specific scenarios for the SmartFusion2, IGLOO2, RTG4, and PolarFire Product Families. With the Libero SoC releases listed below, these issues have been corrected, allowing SmartTime to produce a complete static timing analysis.

- Libero SoC v12.5 and later for RTG4 and PolarFire
- Libero SoC v12.5 SP1 and later for SmartFusion2 and IGLOO2

For more information, refer to CN20022.

1.2 New Device Support

1.2.1 PolarFire SoC

Libero SoC v12.5 introduces support for PolarFire SoC, the industry's first System on Chip (SoC) Field-Programmable Gate Array (FPGA), with a deterministic, coherent RISC-V CPU cluster and a deterministic L2 memory subsystem that enables Linux and real-time applications.

This Libero SoC version supports the FPGA design portion of the new PolarFire SoC devices. SoftConsole is a software development environment facilitating the rapid development of bare-metal and RTOS based C/C++ software for Microchip CPU and SoC based FPGAs. It provides development and debug support for PolarFire SoC devices, and will be available as a separate installation.

1.2.1.1 Preliminary Timing and Power Support

Libero SoC v12.5 introduces “Preliminary” timing and power support for the following devices/package combinations.

Table 1-1. Preliminary Timing and Power Support

Device and Package	Part Number	Libero Licensing			
		Eval	Silver	Gold	Platinum
Device MPFS250T, Package FCVG484					
	MPFS250T-FCVG484E	Yes	Yes	Yes	Yes
	MPFS250TL-FCVG484E	Yes	No	Yes	Yes
	MPFS250T-1FCVG484E	Yes	Yes	Yes	Yes
	MPFS250T-FCVG484I	Yes	No	Yes	Yes
	MPFS250TL-FCVG484I	Yes	No	Yes	Yes
	MPFS250T-1FCVG484I	Yes	No	Yes	Yes
Device MPFS250, Package FCSG536					

.....continued					
Device and Package	Part Number	Libero Licensing			
		Eval	Silver	Gold	Platinum
	MPFS250T-FCSG536_EvalE	Yes	No	Yes	Yes
	MPFS250TL-FCSG536_EvalE	Yes	No	Yes	Yes
	MPFS250T-1FCSG536_EvalE	Yes	No	Yes	Yes
	MPFS250T-FCSG536_EvalI	Yes	No	Yes	Yes
	MPFS250TL-FCSG536_EvalI	Yes	No	Yes	Yes
	MPFS250T-1FCSG536_EvalI	Yes	No	Yes	Yes
Device MPFS250, Package FCVG784					
	MPFS250T-FCVG784_EvalE	Yes	No	Yes	Yes
	MPFS250TL-FCVG784_EvalE	Yes	No	Yes	Yes
	MPFS250T-1FCVG784_EvalE	Yes	No	Yes	Yes
	MPFS250T-FCVG784_EvalI	Yes	No	Yes	Yes
	MPFS250TL-FCVG784_EvalI	Yes	No	Yes	Yes
	MPFS250T-1FCVG784_EvalI	Yes	No	Yes	Yes
Device MPFS250, Package FCG1152					
	MPFS250T-FCG1152_EvalE	Yes	Yes	Yes	Yes
	MPFS250TL-FCG1152E	Yes	No	Yes	Yes
	MPFS250T-1FCG1152E	Yes	Yes	Yes	Yes
	MPFS250T-FCG1152I	Yes	No	Yes	Yes
	MPFS250TL-FCG1152I	Yes	No	Yes	Yes
	MPFS250T-1FCG1152I	Yes	No	Yes	Yes

1.2.1.2 Preliminary Timing, Power, and Programming Support

Libero SoC v12.5 introduces “Preliminary” timing, power, and programming support for the following devices/package combinations.

Table 1-2. Preliminary Timing, Power, and Programming Support

Device and Package	Part Number	Libero Licensing			
		Eval	Silver	Gold	Platinum
Device MPFS250T, Package FCVG784					
	MPFS250T_ES-FCVG784_EvalE	Yes	No	Yes	Yes
	MPFS250T_ES-1FCVG784_EvalE	Yes	No	Yes	Yes
Device MPFS250T, Package FCSG536					
	MPFS250T_ES-FCSG536_EvalE	Yes	No	Yes	Yes
	MPFS250T_ES-1FCSG536_EvalE	Yes	No	Yes	Yes

1.2.1.3 Advance Timing and Power Support

Libero SoC v12.5 introduces “Advance” timing and power support for the following devices/package combinations.

Table 1-3. Advance Timing and Power Support

Device and Package	Part Number	Libero Licensing			
		Eval	Silver	Gold	Platinum
Device MPFS460, Package FCG1152					
	MPFS460T-FCG1152_EvalE	Yes	No	No	Yes
	MPFS460TL-FCG1152_EvalE	Yes	No	No	Yes
	MPFS460T-1FCG1152_EvalE	Yes	No	No	Yes
	MPFS460T-FCG1152_EvalI	Yes	No	No	Yes
	MPFS460TL-FCG1152_EvalI	Yes	No	No	Yes
	MPFS460T-1FCG1152_EvalI	Yes	No	No	Yes

1.2.2 PolarFire

1.2.2.1 Military Operating Condition

Production timing support has been added for the following devices:

- MPF200TS MIL temp, 1.05V, STD speed grade
- MPF300TS MIL temp, 1.05V, STD speed grade
- MPF500TS MIL temp, 1.05V, STD speed grade

1.2.2.2 New Lidless Package for MPF300T/S

Libero SoC v12.5 introduces support for a new lidless package for the following PolarFire devices. The package is similar to the regular FCG784, with the same pinouts and support. Refer to the PolarFire FPGA Packaging and Pin Descriptions User Guide for the package drawing of the FCG784N lidless package.

- MPF300T FCG784N, IND temp, STD and -1 speed grade
- MPF300TS FCG784N, IND temp, STD and -1 speed grade

1.3 Licensing Update for PolarFire FPGAs

Starting with the Libero SoC v12.5 release, the Silver license supports the following PolarFire FPGA part numbers:

- MPF300TS-1FCG1152I
- MPF300TS-1FGG484I
- MPF300TS-FGG484I
- MPF300T-1FCG1152E
- MPF300T-1FCG484E

1.4 Software Features and Enhancements

1.4.1 Include Path and Global File Settings for Verilog and SystemVerilog Sources

Libero SoC v12.5 enables support to globally specify one or more search paths for Verilog and SystemVerilog include files. This allows users to include files without having to specify a hard-coded absolute or relative path.

Libero SoC v12.5 also enables support to specify a Verilog or SystemVerilog file as a global file. Global files are added at the beginning of the file compile order passed to Synthesis and Simulation.

1.4.2 New Report for VHDL Generic and Verilog Parameter Values for Each Specific Instance of the Whole Hierarchy

Libero SoC v12.5 allows users to export a report that shows, for each instantiated Verilog module or VHDL entity, the list of parameters/generics and their actual final instantiated values. The report is generated for the current root.

1.4.3 New Report Listing All IP Cores and Their Configuration

Libero SoC v12.5 provides a Tcl command that allows users to generate a report, in plain text and JSON format, that lists all the cores used in the design. The report includes the core version and its configuration parameters.

Note: The following cores do not list configuration parameters in the report:

- SmartFusion2/IGLOO2 System Builder components
- SmartFusion2/IGLOO2 MSS/HPMS components
- RTG4FDDRC_INIT
- RTG4 NPSS_SERDES_IF_INIT
- RTG4 PCIE_SERDES_IF_INIT

1.4.4 User Control to Force Design State to be Up-to-Date Manually

Libero SoC v12.5 introduces a “Force Design up-to-date” feature. With this feature, if changes are made to HDL and/or constraint files, Libero puts the design flow out-of-date if it was in a pass state. In this way, users can use the new feature to force the design flow back to a pass state.

Example: If a source file (HDL file or constraint) is modified after running the Libero design flow through to the Implement design steps (including Place and Route), Libero invalidates the synthesis and layout states automatically. Users can restore the states of the implementation tools to "pass" using the **Force Design up-to-date** action.

For more information about this feature, refer to the appropriate guide according to the SoC family:

- Libero SoC v12.5 Design Flow User Guide for PolarFire
- Libero SoC v12.5 Design Flow User Guide for RTG4, SmartFusion2, and IGLOO2

1.4.5 Block Flow Enhancements for VHDL and Timing Constraints

Libero SoC v12.5 introduces block flow support for VHDL designs for SmartFusion2, IGLOO2, and RTG4 designs. Blocks created for VHDL designs can now be imported into SystemVerilog, Verilog, and VHDL top-level modules. Internal block constraints, such as false paths or multi-cycle, are now fully supported for a published block.

1.4.6 Verify Timing Configurations

Libero SoC v12.5 extends the configurations of Verify Timing for customizing the generated Timing reports in SmartFusion2, IGLOO2, and RTG4 designs. The new Report settings:

- Are available in XML, Text, CSV (Tcl only), and HTML (Tcl only) formats.
- Limit the number of reported paths per section.
- Limit the number of expanded paths per section.
- Limit the number of parallel paths per expanded path.
- Configure the maximum slack threshold for Timing Violations report.

Note: In Libero v12.4, this feature was available for PolarFire only. In Libero v12.5, this feature is also available for SmartFusion2, IGLOO2, and RTG4.

1.4.7 Synthesis Enhancements

SynplifyPro Q2020.03M included in Libero SoC v12.5 contains the following enhancements:

- Support for PolarFire SoC technology
- Uniform naming of Soft TMR registers for PolarFire and RT PolarFire
- Soft TMR support for register arrays for SmartFusion2, IGLOO2, and PolarFire
- Improved timing correlation for PolarFire technology

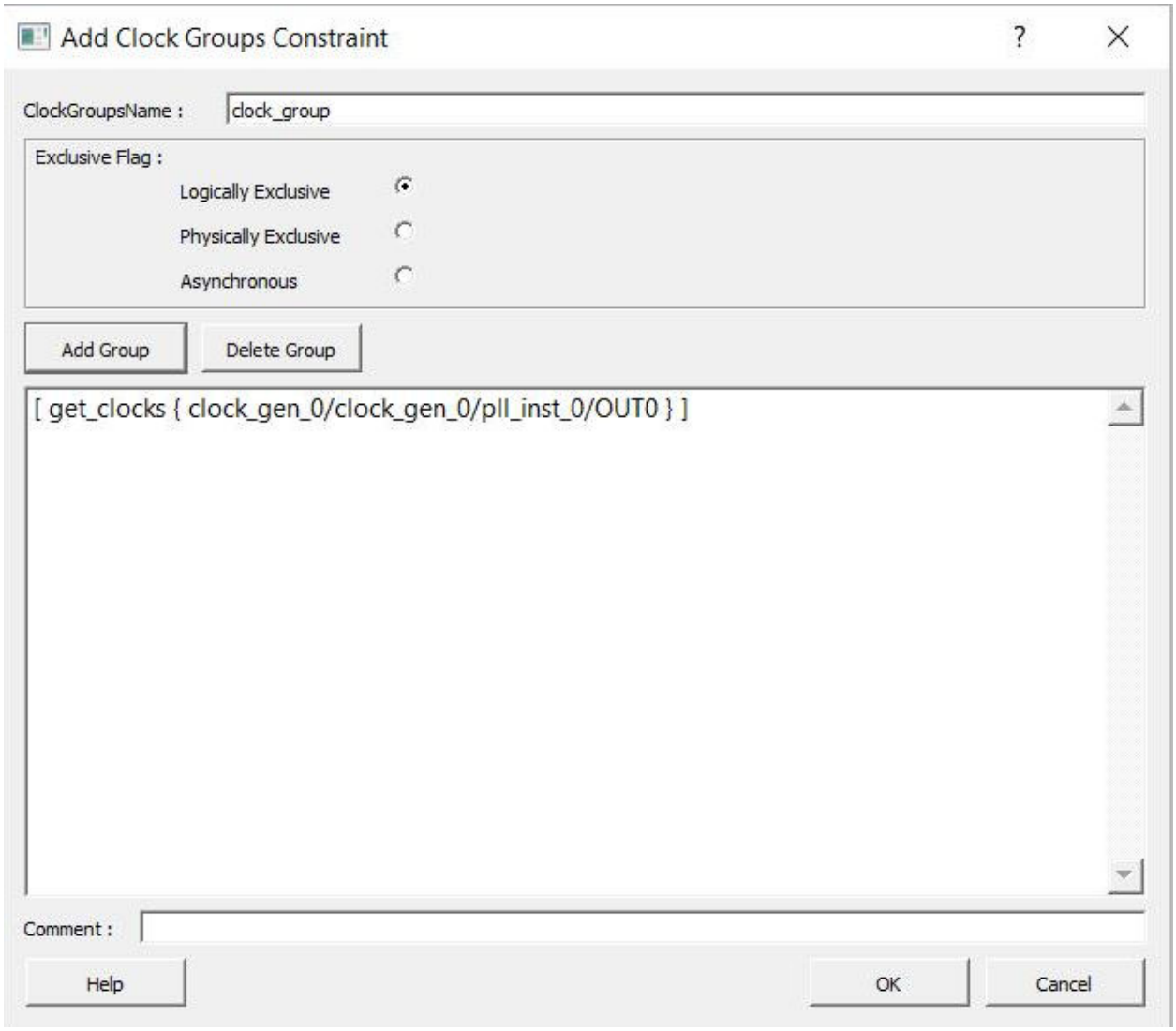
Libero SoC v12.5 users can synthesize designs outside the Libero SoC software using Synopsys SynplifyPro directly. When using this flow, the following additional steps are necessary to synthesize and implement a design:

- Make sure the <Libero SoC v12.5 installation>/data/aPA5M/polarfire_syn_comps.v is added as a source file to the SynplifyPro project. This file contains module declarations with timing information for PolarFire primitives not known to SynplifyPro. For projects created with a previous version, update the location of this file in the SynplifyPro project.
- Many configured cores generate timing constraints. For optimal results, make sure these constraint files are passed to synthesis. These constraint files must also be imported into Libero along with the synthesis gate level netlist for optimal place, route, and timing analysis results. Core-generated constraint files must be modified so that constraints are expressed using the proper hierarchical name of the configured cores in the top-level design.

For more information, see <Libero SoC v12.5 installation>/SynplifyPro/doc.

1.4.8 CDC Report Enhancements

Right-clicking the boxes in the CDC table opens a menu with options for copying the source clock and destination clock to the Clipboard, and for adding a clock group constraint between the source and destination clock using the Add Clock Groups Constraint dialog box (shown below).



Note: This dialog box belongs to the constraint editor. Therefore, the constraint editor must be in an open/running state before performing this action. Cross-probing will not work if the invoked tool is not already in the open/running state. These added constraints will change the behavior of timing and invalidate the Verify Timing design flow step and SmartTime analysis results. As a result, Verify Timing will need to be re-run.

1.4.9 SuSE Support

Libero SoC v12.5 introduces support for OpenSUSE Leap 42.3 (SLES 12.3 equivalent). For details, refer to 5. System Requirements.

For installation details, refer to the UG0710 Libero SoC Linux Environment Setup User Guide.

1.5 New Silicon Features and Enhancements

1.5.1 PolarFire SoC

1.5.1.1 Stand-alone MSS Configurator

Besides supporting FPGA design flow for PolarFire SoC devices, Libero SoC v12.5 includes a stand-alone MSS configurator (pre-production) located at <Libero SoC v12.5 installation>/bin64/pfsoc_mss.

The stand-alone MSS configurator outputs a generated MSS component that must be imported into the Libero SoC project to complete the design. Additionally the MSS configurator outputs an xml file that SoftConsole will use as source to initialize the processor subsystem based off of selections made in the MSS configurator.

1.5.1.2 PolarFire SoC MSS Simulation

For simulation, the PolarFire SoC MSS is modeled with a Bus Functional Model (BFM). The BFM helps users:

- Verify the connectivity and addressing of peripherals in the Fabric that connect to the MSS using the Fabric Interface Controllers (FICs).
- Emulate interrupts behavior between the MSS and the FPGA fabric.

1.5.1.3 SmartDebug for PolarFire SoC MPFS250T_ES Extended Device

The Libero SoC v12.5 release supports SmartDebug for PolarFire SoC MPFS250T_ES extended device.

1.5.2 PolarFire and PolarFire SoC

1.5.2.1 Transceiver - New Static DFE Calibration Option for Signal Integrity

Libero SoC v12.5 enhances the PolarFire Transceiver Enhanced Receiver Management (ERM) solution to support static calibration for the DFE mode. The PolarFire Transceiver ERM core has been updated to add a new static DFE calibration option. The set_io PDC constraint has been extended to set the RX_DFE_COEFFICIENT_H* (1-5) coefficients. When using the static DFE calibration option, users must also set the RX_CTLE setting. For more details, refer to the Microsemi PolarFire FPGA Transceiver User Guide.

1.5.2.2 Transceiver CTLE Settings

Starting with Libero SoC v12.5, all RX_CTLE settings have been fully validated and can be considered as production.

1.5.2.3 I/O Gearing Interfaces

The new Octal IOD PHY configurator supports generation of PF_IOD_OCTAL_DDR core based on an 8-bit Serial Interface operating Double Data Rate (DDR) mode. The PF_IOD_OCTAL_DDR IOD PHY supports interfaces tor xSPI (JESD251), HyperBUS, and ONFI for interfacing to associated third-party memory controller IP.

1.5.2.4 Additional DDR3 and DDR4 Presets

Libero SoC v12.5 introduces additional DDR3 and DDR4 preset configurations that can be selected to improve ease of use.

For DDR3, the new preset configurations support:

- DDR3-1600, DDR3-1866, DDR3-2133
- tCK greater than 1.5 ns (frequencies 666.67 MHz and lower)
- All CL/CWL combinations

For DDR4, the new preset configurations support:

- DDR4-1866, DDR4-2133, DDR4-2400, DDR4-2666, DDR4-2933, and DDR4-3200
- tCK greater than 1.25 ns (frequencies 800 MHz and lower)
- All CL/CWL combinations

1.5.2.5 SmartDebug - I/O Margining Analysis for DDR Memory Controllers

With Libero SoC 12.5, SmartDebug introduces the new Debug DDR Memory tool for DDR3/DDR4/LPDDR3. This tool is supported by PolarFire only and allows users to visualize the margin on the DDR I/Os after the DDR I/O interface has been trained.

1.5.2.6 PolarFire System Services

The CoreSysServices_PF soft IP has been deprecated. New designs should instantiate the PolarFire System Services core, which provides an easy user interface to run the system services along with sNVM. For more information, see the UG0848 PolarFire System Services User Guide.

1.5.2.7 PolarFire XCVR Sourced Fabric Clocks and Jitter Compensation

The PolarFire XCVR can source three different clocks into the fabric:

- TX_CLK
- RX_CLK
- REFCLK (FAB_REF_CLK)

These clocks contain high frequency jitter that is not automatically taken into account by Libero in the timing report and SmartTime. It is recommended that users add clock-uncertainty constraints to these clocks in their design.

The following table shows recommended values for clock uncertainty per clock, resource, and speed-grade.

Table 1-4. Recommended Values for Clock Uncertainty

Clock Type	STD	-1
FAB_REF_CLK on Global	275ps	200ps
FAB_REF_CLK on Regional	N/A	N/A
TX_CLK_G on Global	300ps	225ps
TX_CLK_R on Regional	225ps	150ps
RX_CLK_G on Global	325ps	250ps
RX_CLK_R on Regional	250ps	175ps

The following example shows a clock-uncertainty constraint that can be added to the user's timing SDC file.

```
set_clock_uncertainty -setup 0.150 [ get_pins { PF_XCVR_ERM_LANE2/I_XCVR/LANE0/TX_CLK_R } ]
set_clock_uncertainty -setup 0.175 [ get_pins { PF_XCVR_ERM_LANE2/I_XCVR/LANE0/RX_CLK_R } ]

# TX_CLK and RX_CLK on Globals
set_clock_uncertainty -setup 0.300 [ get_pins { PF_XCVR_ERM_LANE2/I_XCVR/LANE0/TX_CLK_G } ]
set_clock_uncertainty -setup 0.325 [ get_pins { PF_XCVR_ERM_LANE2/I_XCVR/LANE0/RX_CLK_G } ]

# FAB_REF_CLK on Global
set_clock_uncertainty -setup 0.275 [get_clocks PF_DDR4_C0_0/CCC_0/pll_inst_0/OUT1]
```

The automatic management of these constraints will be added in a future release of Libero SoC.

1.5.3 RT PolarFire

1.5.3.1 RTPF500T-CG1509M Package Pinout Update

To optimize PCB layout and signal integrity of DDR signals, DDR3 and DDR4 pin assignments of the RTPF500T-CG1509M package have been altered in Libero SoC v12.5. These changes affect DDR3 and DDR4 I/Os only, and do not affect any other I/O assignment. Place and route performed with Libero SoC v12.4 will be invalidated when the Libero SoC v12.4 design is opened with Libero v12.5. Any DDR assignments in an existing pdc constraints file must be discarded and re-entered through the I/O Editor.

1.5.3.2 Project Setting to Abort Flow if 3.3V I/O is Found in the Design

Libero SoC v12.5 prevents RT PolarFire designs containing 3.3V I/Os from proceeding, unless you uncheck the new **Abort flow if 3.3V I/O found in the design** option in the Project settings menu. If this option is unchecked, a warning is issued inside the <design>_pinrpt_boardlayout report and when you Generate FPGA Array Data.

⚠WARNING I/Os at 3.3V are vulnerable to Single Event Latch-up at low LET levels. Review RT PolarFire radiation data at Microchip.com.

1.5.3.3 Enable System Controller Suspended Mode by Default

The System controller suspended mode is enabled by default for all new RT PolarFire projects created starting with Libero SoC v12.5. Disabling the System controller suspended mode increases vulnerability to radiation single event effects in the System controller.

If the System controller suspended mode is enabled in any PolarFire design, the following operations will not be available during normal operation:

- All System controller services requested after power-up is complete and the System controller is suspended
- System controller-generated Tamper flags
- Device reset and zeroization Tamper responses
- SPI-Master In-Application Programming (IAP)
- SPI-Slave programming mode

For more information, refer to the System Services section in the PolarFire FPGA Security User Guide.

1.5.3.4 Clock Buffer Usage Statistics to Help Compute Risk of Clock Upsets

The Global Net report in Libero SoC v12.5 includes a Clock Signals summary section that prints statistics showing utilization of clock networks after completion of place and route for PolarFire designs. Designers should consult the latest radiation effects data regarding RT PolarFire clock networks from Microchip to determine the risk of clock upsets specific to their design in their target radiation environment.

1.5.4 RTG4

1.5.4.1 SSN Analyzer for CQ352 Package

Libero SoC v12.5 adds SSN Analyzer support for RT4G150-CQ352.

1.5.4.2 Configure Register Lock Bits

RTG4 devices allow you to restrict access to SERDES and FDDR configuration registers. Libero SoC v12.5 includes the Register Lock Bits Configuration tool to lock these configuration registers and prevent them from being overwritten by masters that have access to these registers.

An initial Configuration Lock Bit file is created when you Generate FPGA Array Data. The file is named <project>/designer/<design>/<design>_init_config_lock_bits.txt. This is the initial and the default Lock Bit Configuration File. Use this file as a template to make changes. Modify it to ensure that the lock bits are set to “0” for all register bits you want locked. Save the file as a *.txt file with a different name.

From the Design Flow window, click **Configure Register Lock Bits**. Click the **Browse** button to go to the text file (*.txt) that contains the Register Lock Bit settings and import the file into the project.

Note: Simulation support for this feature is unavailable.

2. Migrating Designs to Libero SoC v12.5

2.1 Design and Core Invalidation

2.1.1 RT PolarFire Designs Layout Invalidation

Place and route performed with Libero SoC v12.4 will be invalidated when Libero SoC v12.5 is invoked for designs using the RTPF500T-CG1509M device due to the package pinout update described in 1.5.3.1 RTPF500T-CG1509M Package Pinout Update.

2.2 Core Enhancements and Upgrades

If a project created in a Libero release prior to v12.5 contains the following cores that have been generated, they do not need to be upgraded after migrating the project to Libero SoC v12.5. However, if the core needs to be generated again for any reason (for example, a change in parameters), the latest version from the Catalog must be downloaded and used.

Libero SoC v12.5 includes the following **PolarFire** core updates from Libero SoC v12.4.

Core	12.5 Version	Comments
CoreSmartBERT	2.7.101	Functional Changes: Removed 12500Mbps and 12700Mbps data rates.
PolarFire DDR3	2.4.112	Enhancements: Added higher speed bin presets.
PolarFire DDR4	2.4.112	Enhancements: Added higher speed bin presets.
PolarFire IOD CDR	2.4.103	Enhancements: Updated false_path constraints generation for coverage.
PolarFire IOD CDR Clocking	2.1.105	Enhancements: Updated false_path constraints generation for coverage.
PolarFire IOD Generic Receive Interfaces	2.1.101	Functional Changes: Added a DRC to prevent using bit-slip for ratio 3.5. Enhancements: Updated false_path constraints generation to improve Quality of Result (QoR).
PolarFire RGMII to GMII	1.3.100	Enhancements: Added centered clock to data relationship support.
Transceiver Interface	3.1.100	Enhancements: Added support for Static DFE settings.
PolarFire SRAM (AHBLite and AXI)	1.2.106	Enhancements: Improved latency when ECC is configured in Pipeline mode.
RTG4 SRAM (AHBLite and AXI)	1.0.111	Enhancements: Improved latency when ECC is configured in Pipeline mode.

For information about how to update a core, refer to the 2.3 Core Update Procedure.

2.3 Core Update Procedure

Perform the following procedure to update a core version:

1. Download the latest version of the core into your vault.
2. Upgrade each configured core in your design to the latest version by right-clicking on the core component in the design hierarchy and selecting **Replace Component Version**.

3. Regenerate the core.
4. Derive the Timing Constraints again from the Constraint Manager tool to use the latest generated core timing constraints.
5. Rerun the design flow.

3. Resolved Issues

The following table lists the customer-reported defects and enhancement requests resolved in Libero SoC v12.5 that have case numbers. Resolution of previously reported “Known Issues and Limitations” are also noted in this table.

Case Number	Description
493642-2198699130	HDL_EDITOR: Font size control in Text Editor. Resolution: Libero SoC v12.5 adds font size control in the Text Editor tool bar.
493642-2707807672	Issue with run_tool -name {SYNTHESIZE} command. Resolution: Libero SoC v12.5 generates a proper error for any tool not supporting the -script option.
493642-2709650361	Enhancement: Pins that are reserved using I/O Editor or PDC are reported as UNASSIGNED. Resolution: The Libero SoC v12.5 I/O Editor has been enhanced to identify reserved pins properly.
493642-2707807672	Libero to generate an error message when "-script" is passed to Synthesis tool. Resolution: Libero SoC v12.5 generates a proper error for any tool not supporting the -script option.
493642-2724120891	Report IPs used in the design. Resolution: See 1.4.3 New Report Listing All IP Cores and Their Configuration.
493642-2725055679	Constraint Manager GUI scenarios. Resolution: The Libero SoC v12.5 Constraint Manager window now resizes automatically the columns to the default size when the design root is changed.
493642-2748882679	PF_CCC: Remove bypass option from configurator. Resolution: The bypass option has been removed from the PolarFire CCC configurator in Libero SoC v12.5.
493642-2719322398	Enhancement: PF_RGMII_TO_GMII v1.2.109 to support center-aligned, and to provide required timing constraints on IO and fabric side. Resolution: The centered clock-to-data relationship support has been added to the PF_RGMII_TO_GMII core version 1.3.100 available with Libero SoC v12.5.
493642-2670706372	PF_IOD_GENERIC_TX: Issue with IOD configurator. Resolution: The **No forwarded clock** option when clock ratio is set to 1 is now fully working in Libero SoC v12.5.
493642-2727045569	PF_IOD_RX: Issue in Bitslip port functionality. Resolution: The bit-slip option is no longer supported for ratio 3.5. The PolarFire IOD Generic Receive Interfaces core version 2.1.101 available with Libero SoC v12.5 prevents the use of the bit-slip option for ratio 3.5.
493642-2714858502	PF_IOD_GENERIC_RX v2.0.123: Synthesis warning for inferred clock. Resolution: Libero SoC v12.5 fixes some minor issues with some timing models passed to synthesis. The warnings are no longer present with these fixes.
493642-2739738590, 493642-2738983431	IOD_Generic_RX_IF_IP: Fix from 12.3 (1.4.105) crashes Placer on v12.4. Resolution: Libero SoC v12.5 handles unbonded I/O locations for assigning IOD.
493642-2662765497	PF_SRAM init is incorrect for RAM with native interface. Resolution: Libero SoC v12.5 considers padding for Native Interface of PF_SRAM_AHBL for memory files imported into fabric RAM.

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Case Number	Description
493642-2599859313	Crash observed at Place and Route stage. Resolution: Pre-layout timer will not run out of memory in Libero SoC v12.5.
493642-2767884077	Router fails for an RTG4 design. Resolution: Place and Route in Libero SoC v12.5 has improved the resolution of routing congestion due to multiple instances of BUFD_DELAY macros that typically are inserted to fix hold violations on APB interface.
493642-2701735993	Issue with constraint coverage report. Resolution: In Libero SoC v12.5, the constraint coverage report algorithm has been updated to add more tie-off detection and propagation rules to detect cases where all inputs of a cell are tied-off and the output is constant.
493642-2725264465	tao.exe consumes entire memory resources. Resolution: Designs where the top-level generics have no default value are illegal and fail synthesis. Prior to Libero SoC v12.5, this type of error was ignored during the processing of the timing constraints, causing an out-of-memory error. Starting with Libero v12.5, such designs will fail the synthesis step. To fix this issue, provide default values for the generic parameters.
493642-2740931364	SmartTime loads with empty/blank summary. Resolution: This issue has been resolved in Libero SoC v12.5. SmartTime opens with the correct Summary page information.
493642-2706750810	XCVR SmartBERT IP patterns and PMA patterns test issue on single/multiple lanes. Resolution: Running a PRBS test using SmartBERT after conducting a XCVR PMA PRBS test on another lane resulted in errors and inconsistent behavior on the lanes. This sequencing problem between PRBS tests has been resolved in Libero SoC v12.5.
493642-2716781171	Active Probes: Probe read on MPF500T device for a few signals shows unexpected data. Resolution: This issue has been resolved in Libero SoC v12.5. Probes are fully working for the MPF500T device.
493642-2727638971	Disable PRBS tests from XCVR PMA for PCIe lanes. Resolution: PRBS tests are not allowed for PCIe lanes. These tests are disabled in Libero SoC v12.5.
493642-2719750985, 493642-2722233076	FP5 shows 4MHz clock, even if the user sets the TCK to 1 MHz. Resolution: Scan chain always runs at 1MHz to ensure correctness. User-selected TCK is set to run user-selected action.
493642-2737556103	Error during "Generate Bitstream" in v12.4. Resolution: SmartFusion2 or Igloo2 design from Libero 12.4 and earlier, using tamper macro with power-up digest enabled, no longer has issues generating programming bitstream.
493642-2739114720	SF2: Export bitstream is failing with the "Failed to export single device PPD" message. Resolution: In Libero SoC v12.5, when the SPI clock frequency is set to an illegal 25MHz value, the proper error message is now printed in the Libero log window - "Error, SPI clock frequency of 25MHz is not supported. You must change it in Configure Programming Recovery tool."
493642-2695720170	PolarFire LSRAM with write enables not inferred. Resolution: SynplifyPro 2020.03M Prod packaged with Libero Soc v12.5 combines memory where output is defined as bus register.
493642-2702511236	Type binding error while using packages in VHDL. Resolution: SynplifyPro 2020.03M Prod packaged with Libero Soc v12.5 resolves this issue.

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Case Number	Description
493642-2708444618	Identify Instrumentor errors out when instrumenting the signal. Resolution: Identify and SynplifyPro 2020.03M Prod packaged with Libero Soc v12.5 enables probing of enum states.
493642-2701748361	Anomaly in TMR implementation. Resolution: SynplifyPro 2020.03M Prod packaged with Libero Soc v12.5 prevents optimization of the TMR voter with subsequent arithmetic logic.
493642-2716372941	Problem with Synplify Pro performing replication on register in v12.3. Resolution: SynplifyPro 2020.03M Prod packaged with Libero Soc v12.5 documents the rep_clkint_drive option.
493642-2724075924	Synplify documentation lacks some of the project settings. Resolution: SynplifyPro 2020.03M Prod packaged with Libero Soc v12.5 adds information of synthesis options to the FPGA Reference Manual.
493642-2736326666	SynplifyPro error: nets stuck at zero optimization. Resolution: SynplifyPro 2020.03M Prod packaged with Libero Soc v12.5 resolves this issue.
493642-2738118700	SynplifyPro crash: Ternary adder decomposition. Resolution: SynplifyPro 2020.03M Prod packaged with Libero Soc v12.5 resolves this issue.
493642-2734869215	SynplifyPro crash: Adder structures with the number of inputs more than the number of output pipeline registers. Resolution: SynplifyPro 2020.03M Prod packaged with Libero Soc v12.5 resolves the reported crash.
493642-2742096249	Missing orig_sources file in synthesis_1 (identify folder) in v12.4. Resolution: Identify and SynplifyPro 2020.03M Prod packaged with Libero Soc v12.5 will create the original sources directory.
493642-2743414776	m_generic.exe error in Libero SoC v 12.4. Resolution: SynplifyPro 2020.03M Prod packaged with Libero Soc v12.5 resolves the reported crash.
493642-2739833657	SmartFusion2, IGLOO2, RTG4: Synopsys synplify support for TMR register array. Resolution: SynplifyPro 2020.03M Prod packaged with Libero Soc v12.5 infers TMR for register array.
493642-2748440670	RTG4 PLL loses lock in simulation. Resolution: The RTG4 FCCC simulation model in Libero SoC v12.5 resolves the issue. Previously, due to calibration process, in some cases: • PLL was losing a LOCK after calibration. • The PLL LOCK was not coming after calibration. • Phase difference was observed due to improper initialization.
493642-2739064301 493642-2754834562	SmartFusion2, IGLOO2, RTG4: Routing conflicts report does not exist. Resolution: Libero SoC v12.5 has been enhanced to produce the routing conflicts report for SmartFusion2, IGLOO2, and RTG4.
493642-2744958875	Libero crashes when driver replication is enabled for P&R. Resolution: The netlist writer in Libero SoC v12.5 has been updated to handle user property values with embedded multiple quotes.
493642-2707340967	PolarFire SmartPower crashes when a Vectorless option is selected. Resolution: SmartPower in Libero SoC v12.5 handles arithmetic carry-chains in the Vectorless method..

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Case Number	Description
493642-2730492553	RTG4 FCCC output out of phase from Ref Clk during simulation. Resolution: The RTG4 FCCC simulation model in Libero SoC v12.5 has been updated to align the offset for the CCC outputs with the reference clock.
493642-2741966473	RTG4 TPSRAM generates unsupported Write byte-enables for Two-port x12 mode. Resolution: The RTG4 Two-port LSRAM configurator in Libero SoC v12.5 will generate the proper number of Write byte-enable signals for x12 configurations.
493642-2747132203	RTG4 CCC post-layout simulation issue. Resolution: This issue occurs when the signal pulse width is less than the element delay. To resolve this issue, Libero SoC v12.5 now adds the **+transport_path_delays** option to the vsim command automatically for post-layout simulation.
493642-2726667751	RTG4 AutoReset/Dynamic PLL Sim Failure (PLL never relocks after losing Lock). Resolution: The RTG4 FCCC simulation model in Libero SoC v12.5 resolves the issue.
493642-2756297422	Netlist with LSRAM using falling edge will retain Inverter and use unprotected net for clocks. Resolution: Libero SoC v12.5 will absorb inverted clock signals on radiation-hardened global resources.
493642-2756655021	RTG4: Global Net report states that UPROM CLK port driven by unprotected local clock. Resolution: The Global Net report in Libero SoC v12.5 will not improperly flag UPROM clock input driven by radiation hardened global resources.
493642-2333785088	HDL_LANGUAGE: DH: Generic/parameter report for Libero. Resolution: See 1.4.2 New Report for VHDL Generic and Verilog Parameter Values for Each Specific Instance of the Whole Hierarchy.
493642-2635251228	HDL_LANGUAGE: DH: Changing include files will not invalidate synthesis. Resolution: Libero SoC v12.5 invalidates the Design Hierarchy and the design flows when there is a change in the include file content, global include file (set/unset/content change), and global include path (add/delete/change include path order).
493642-2705337030	HDL_LANGUAGE: [GLOBAL_INCLUDE_FILE] : How to set an include file as a global file in Libero. Resolution: See 1.4.1 Include Path and Global File Settings for Verilog and SystemVerilog Sources.
493642-2705337030	HDL_LANGUAGE: [GLOBAL_INCLUDE_PATH] Support for Global Include Paths in Libero. Resolution: See 1.4.1 Include Path and Global File Settings for Verilog and SystemVerilog Sources.
493642-2695285103	Smartpower Export should always use Windows line endings even if generated under Linux. Resolution: SmartPower in Libero SoC v12.5 resolves the issue.
493642-2432221637, 493642-2408948028	Export IBIS with models for JTAG and SC-SPI pin. Resolution: In Libero SoC v12.5, the IBIS models for JTAG and SC-SPI have been added to the exported IBIS file.
493642-2656105250, 493642-2694971130, 493642-2658277805	The IBIS models of the DDR3/4 of MPF are modeled with fixed ODT. Resolution: In Libero SoC v12.5, the IBIS model for DDR3/4 has been updated to export the user-defined ODT settings.
493642-2735902714	SSN analyzer support for RT4G150-CQ352. Resolution: SSN analyzer support for RT4G150-CQ352 has been added in Libero SoC v12.5.

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Case Number	**Description**
493642-2737698780	Warning about 2TB system during a v12.4 installation. Resolution: The warning has been removed from the installation script. Starting with Libero SoC v12.4, Libero fully supports large drives (greater than 2 TBytes) on Linux.
493642-2636063864	Add Libero support for SuSE 12 OS support in Libero. Resolution: Libero SoC v12.5 adds support for SUSE 12.
493642-2759903125	Place & Route Failure for "get_clocks" in the "-to" Portion of Timing Constraint. Resolution: Libero SoC v12.5 resolves the reported crash.

The following table lists the customer-reported defects and enhancement requests resolved in Libero SoC v12.5 that do not have case numbers. Resolution of previously reported “Known Issues and Limitations” are also noted in this table.

Description
HDL_LANGUAGE: DH: [GLOBAL_INCLUDE_FILE] .h files imported in Libero are not read unless used in `include statement’. Resolution: See 1.4.1 Include Path and Global File Settings for Verilog and SystemVerilog Sources.
Verify Timing needs additional reporting options. Resolution: SmartPower in Libero SoC v12.5 extends the Verify Timing report options for SmartFusion2, IGLOO2 and RTG4.
Add User Control to Manually Force Design State to be Up-to-Date. Resolution: See 1.4.4 User Control to Force Design State to be Up-to-Date Manually .
Block_flow: Libero 12.x compile not able to integrate vhdl-based blockflow blocks. Resolution: See 1.4.5 Block Flow Enhancements for VHDL and Timing Constraints.
RTG4FCCCECALIB: RTG4_ECALIB configurator Display of Delay from Input to Output is not available in GUI. Resolution: Delay values are now displayed in the FCCC GUI.
Check write permission to home folder before opening libero. Resolution: Libero reports an error in the terminal when there is write permission for the home directory.
Block_Flow: PF: tao crashes when using block component. Resolution: The Constraints Manager in Libero has been updated to resolve the crash.
Support for custom STAPL file Resolution: Added custom STAPL file support for FlashPro Express.
Crash during 'Generate SmartDebug FPGA Array data'. Resolution: Libero has been updated to resolved the crash.
FDDR with FPLL Calib Sim Failure with 300MHz Div 3 and FCCC eCalib Clock Base. Resolution: The simulation model has been updated to resolve the issue.
G4 Global net report missing Local to RGB connection. Resolution: The Global Nets Report has been enhanced to report Local clock net to RGB connections.
PF_TPLSRAM Core Creates non-functional Cascade in v12.4. Resolution: The LSRAM configurator engine in Libero has been fixed to support asymmetric widths. Refer to CN20019 in Table 1-1 under 1.1 Customer Notification (CN) and Customer Advisory Notification (CAN) Support.

4. Known Issues and Limitations

The following table lists known issues and limitations associated with Libero SoC v12.5.

Family	Description
Libero	
All Families	The **Modifying Memory Map** option is not working correctly. Do not use the **Modify Memory Map** action in the Libero SoC to connect peripherals to buses in the SmartDesign canvas. Otherwise, Libero may crash or produce an incorrect or incomplete memory map. Instead, connect peripherals to bus slave positions manually, as per the desired memory map.
All Families	Opening two or more views (for example, Hierarchical RTL View and Flattened Post-Compile View) in Netlist Viewer may cause a crash due to memory usage. Avoid opening multiple views for large designs.
All Families	The DRC check in the I/O Editor does not validate all the constraints set in the tool. To validate these constraints, run Place and Route.
PolarFire SoC	Exporting BSDL and Configuring I/O States During JTAG programming is not supported for PolarFire SoC. Currently, all I/Os are tri-stated.
PolarFire SoC	Bank9 VDDI power pins connect to Bank1 VDDI power pins within package substrates for the following packages: • MPFS250 – FCVG484 • MPFS250 – FCVG536_Eval In Libero v12.5, users must make sure Bank9 has the same voltage as Bank1 when setting the banks in these devices because Libero v12.5 does not enforce this rule. This will be fixed in next Libero v12.6 release. For more information, refer to the Package Pin Assignment Table for each package.
PolarFire	In the RAM Configurator, users can enter "initialization" data using RAM content editor. This user data should be carried to the "Design and Memory Initialization" stage. However, this data is not carried to that stage correctly. Instead, the memory Content option under the Fabric RAMs tab is shown as "Content filled with 0s".
RTG4	DRC is not running during RTG4FCCCECALIB generation in TCL flow, but is working correctly in GUI mode.
Simulation	
PolarFire SoC	The PFSoC simulation supports all existing BFM commands. However, when the BFM has only 32-bit data commands, such as “write” and “read”, it causes the simulation to fail. Workaround: At the beginning of the BFM, add one mock (dummy) 64-bit command first. For example: read64 w 0x00000000 0x0 0xA0A1A2A3 0xB0B1B2B3
PolarFire	PLL may generate inaccurate frequency for certain combinations that may lead to drift of PLL outputs over a period.
PolarFire, PolarFire SoC	PLI DLL path is not automatically updated to match the current capture/build path. This issue is observed upon migration between different machines with different Libero installation locations. Workaround : Go to Project settings --> Simulation options --> Vsim commands --> modify something, so that the **Restore Defaults** button is enabled. Click the **Restore Defaults** button to set the correct PLI path. Set other options as required.
RTG4	The RTG4_SRAM_AHBL_AXI core does not support the option **Initialize RAM for Simulation** if ECC is enabled. (Pipelined or Non-pipelined)
Timing/Power	

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Family	**Description**
All Families	SmartTime stops propagating clocks when a generated clock is reached (for example, in a design where the clocks are clk1 --> gen1 --> gen2, specifying gen2 using gen1 as master causes no issue). If gen2 is specified using clk1 as master, however, the generation fails, as clk1 never reached gen2 (it was stopped by gen1). Workaround: Specify the second generated clock using the first generated clock as master.
All Families	In the SmartTime tool, the search option using **Apply filter** is not working.
PolarFire SoC	SmartPower is crashing for the MSS-based design when the **Export MPE** option is used.
SmartDebug	
All Families	In SmartDebug Stand-Alone, SmartDebug operations fail when programming-related steps such as PROGRAM/ERASE/ DEVICE_INFO, Scan Chain, and Auto-Construct Chain steps are run multiple times from the Programming Connectivity and Interface UI during a debug session. Workaround: Close and reopen the debug project to continue debugging the device.
All Families	Export TCL for program action from Standalone SmartDebug exports two additional parameters in the command “run_selected_actions". If this command is executed using execute script, the program action fails. Workaround: Remove the parameters prog_spi_flash and disable_prog_design from the command, and then execute the script.
PolarFire SoC	The **ENVM Debug** option is not available if no ENVM client is configured or if a client is configured as a placeholder in Libero. However, users can run the TCL script from SmartDebug as page view to retrieve the content from the device.
PolarFire SoC PolarFire	When Dual mode PCIe design is considered in SmartDebug, the following issues are observed in the PCIe debug feature: • For dual-PCIe designs that have PCI0 and PCIe1 controllers, only PCIe1 is shown in the UI. PCIe0 is not shown in the UI. • When PCIe0 Lane is selected, the LTSSM state is shown for the PCIe1 design, but not for PCIe0 . LTSSM state is shown for the PCIe1. • Data Rate, Link Width, and all are shown for PCIe1, but not for thePCI0.
PolarFire	Compile fails when FHB auto-instantiation is enabled on designs containing IOD/DDR macros.
Programming	
PolarFire SoC	Embedded FlashPro6 on Icicle board supports TCK between 4MHz and 20MHz. TCK is set to 4MHz when a frequency lower than 4MHz is selected.
PolarFire SoC	Icicle embedded programmer has a longer programming time in Linux than in Windows.
PolarFire SoC	Bank9 I/Os are used in the Icicle kit. This means that users who use the kit must make sure that Bank1 and Bank9 have the same voltage in their Libero design for the following SoCs: • MPFS095 – FCVG484 • MPFS095 – FCSG536 • MPFS160 – FCVG484 • MPFS160 – FCSG536 • MPFS250 – FCVG484 • MPFS250 – FCVG53 Libero v12.5 does not perform checks on Libero versions earlier than v12.6, so it is up to users to follow this guideline.
PolarFire SoC	Embedded FlashPro6 Programmer on IcicleKit does not support SPI-Flash read back on Windows.

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Family	**Description**
PolarFire SoC PolarFire	FlashPro Express developer mode is introduced in the v12.5 release. In developer mode, different SPI Flash files can only be loaded into a device that has SPI Flash file loaded previously. Otherwise, they cannot be loaded.
PolarFire	Supported Micron SPI Flash Memory Devices This release supports only the following Micron SPI Flash memory devices: • Using FlashPro5: MT25QL01G only • Using FlashPro6: all members of N25Q and MT25Q device families. **Note:** Contact Microchip Technical Support about support for Flash memory devices from other vendors and device families using FlashPro6.
PolarFire SoC PolarFir	Starting from Libero SoC v12.4, the vendor information is replaced with the expected density of the target memory to streamline SPI-Flash Programming support with FlashPro6.
PolarFire SoC PolarFire	SPI-Flash programming failure occurs for MT25Q 64-bit, 128-bit, and 2-Gbit densities using FlashPro6. The issue will be fixed in Libero v12.6. Workaround: Program the SPI-Flash using fabric design. If programming using FlashPro6 is needed prior to the release of Libero v12.6, contact Technical Support.
Installation and System Limitations	
N/A	FlashPro6 Driver Re-installation Reports Error Message Customers with FlashPro6 drivers previously installed on their system may see the following message at the end of the installation: The installation of Program Debug Tool v12.5 is finished, but some errors occurred during the install. Please see the installation log for details. Resolution: Uninstall existing FlashPro6 drivers and restart the system before installing Libero SoC v12.5. If the software is already installed, ignore the above message if installation logs do not report any errors.
N/A	Linux Package Required • In Libero SoC v12.5, the script bin/check_linux_req/check_linux_req.sh reports incorrectly that the Linux package xz.i686 is required for RHEL/CentOS 7.x. Package xz.i686 is not required. The correct required packages are xz-libs.x86_64 and xz-libs.i686. • If the installer does not boot in graphical mode, additional X window system libraries might be required. For RHEL/CentOS, the following system package is recommended: $ sudo yum install -y libXau libX11 libXi libxcb libXext libXtst libXrender.
N/A	Antivirus Software Interaction • Many antivirus and Host-based Intrusion Prevention System (HIPS) tools flag executables and prevent them from running. To avoid this problem, modify your security setting by adding exceptions for specific executables. This is configured in the antivirus tool. Contact the tool provider for assistance. • Many users run Libero SoC PolarFire successfully with no modification to their antivirus software. Microchip is aware of issues for some antivirus tool settings that occur when using Symantec, McAfee, Avira, Sophos, and Avast tools. The combination of operating system, antivirus tool version, and security settings all contribute to the end result. Depending on the environment, the operation of Libero SoC, ModelSim ME, and/or Synplify Pro ME may or may not be affected. • All public releases of Libero software are tested with several antivirus tools before they are released to ensure that they are not infected. In addition, the Microchip software development and testing environment is also protected by antivirus tools and other security measures.

5. System Requirements

The Libero SoC v12.5 release has the following system requirements.

5.1 Supported 64-bit Operating Systems

- Windows 7 or Windows 10 OS
- RHEL 6.6-6.11 and RHEL 7.2-7.6
- CentOS 6.6-6.11 and CentOS 7.2-7.6
- Ubuntu 18.04 (Synopsys and Mentor do not directly support the Ubuntu platform)
- OpenSUSE Leap 42.3 (SLES 12.3 equivalent)

Note: Setup instructions for using Libero SoC v12.5 on Red Hat Enterprise Linux OS, CentOS, or Ubuntu are available in the UG0710 Libero SoC Linux Environment Setup User Guide. As noted in that document, installation now includes running a shell script (bin/check_linux_req.sh) to confirm the presence of all required runtime packages.

5.2 Random-Access Memory (RAM) Requirements

Minimum of 16 GB RAM

6. Download Libero SoC v12.5 Software

The following are available for download:

- Libero SoC v12.5 for Linux
- Libero SoC v12.5 for Windows
- MegaVault (Linux)
- MegaVault (Windows)
- Program & Debug (Windows)
- Program & Debug (Linux)
- Standalone MSS configurator installer (Linux)
- Standalone MSS configurator installer (Windows)

Note: Windows installations require administrative privileges.
After a successful installation, clicking **Help-> About Libero** shows release number v12.5.

7. Appendix A. RTG4 SPLL and FPLL Calibration and Workaround

Previously, SPLL (SERDES PCIe and XAUI) and FPLL (FDDR) lost lock during temperature ramp as described in CN19009 and CN19009A. To resolve this issue, a new CoreABC sequence has been developed in Libero SoC v12.4 that includes an SPLL/FPLL workaround. The new sequence requires design changes to the initialization logic (CoreABC configuration and connections) in some cases described in the following sections.

For more information, refer to Appendix B in the Libero v12.4 release notes.

8. Documents Updated in this Release

The following documents have been updated for the 12.5 release.

- Libero SoC Linux Environment Setup User Guide
- Libero SoC v12.5 Design Flow User Guide for PolarFire
- Libero SoC v12.5 Design Flow User Guide for RTG4, SmartFusion2, and IGLOO2
- FCCC with Enhanced PLL Calibration Configuration User Guide for RTG4
- Libero SoC v12.5 Tcl Commands Reference Guide for SmartFusion2, IGLOO2, and RTG4
- Libero SoC v12.5 Tcl Commands Reference Guide for PolarFire
- I/O Editor User Guide for Libero SoC v12.5 for all the families
- SmartPower v12.5 User Guide for all the families
- FlashPro Express v12.5 User Guide for all the families
- SmartDebug v12.5 User Guide for SmartFusion2, IGLOO2, and RTG4 04/2020
- SmartDebug v12.5 User Guide for PolarFire

9. Revision History

Revision	Date	Description
E	11/2020	Updated 1.1.6 Timing Paths May be Missing from Static Timing Analysis (STA) for the SmartFusion2, IGLOO2, RTG4, and PolarFire Product Families
D	10/2020	Added the following information to 4. Known Issues and Limitations: • Information about Bank9 I/Os used in the Icicle kit. • Information about SPI-Flash programming failure.
C	10/2020	Revised the following sections: • 1.1.1 RT PolarFire Pin Assignment Change • 1.1.6 Timing Paths May be Missing from Static Timing Analysis (STA) for the SmartFusion2, IGLOO2, RTG4, and PolarFire Product Families • 1.4.6 Verify Timing Configurations • 1.4.7 Synthesis Enhancements
B	09/2020	Revised the following sections: • 1.4.4 User Control to Force Design State to be Up-to-Date Manually • 1.5.2.7 PolarFire XCVR Sourced Fabric Clocks and Jitter Compensation
A	06/2020	Initial Revision

10. Microchip FPGA Technical Support

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- From the rest of the world, call **650.318.4460**
- Fax, from anywhere in the world, **650.318.8044**

10.2 Customer Technical Support

Microchip FPGA Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microchip FPGA Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

You can communicate your technical questions through our Web portal and receive answers back by email, fax, or phone. Also, if you have design problems, you can upload your design files to receive assistance. We constantly monitor the cases created from the web portal throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

Technical support can be reached at soc.microsemi.com/Portal/Default.aspx.

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), log in at soc.microsemi.com/Portal/Default.aspx, go to the **My Cases** tab, and select **Yes** in the ITAR drop-down list when creating a new case. For a complete list of ITAR-regulated Microchip FPGAs, visit the ITAR web page.

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- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

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