

Programming and Debug Tools v12.5

Release Notes

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Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision 1.0

Revision 1.0 was the first publication of this document.

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1 Programming and Debug Tools v12.5 Software Release Notes

Microsemi's Programming and Debug Tools installer is intended for laboratory and production environments where Libero is not installed, and allows you to install the following tools:

- FlashPro Express
- SmartDebug Standalone
- Job Manager

1.1 Device Support

Programming and Debug Tools v12.4 supports IGLOO2, SmartFusion2, RTG4, and PolarFire families, as well as preliminary support of PolarFire SoC.

2 What's New in Programming and Debug Tools v12.5

Programming and Debugging Tools v12.5 includes the following new features and enhancements.

2.1 New Device Support PolarFire SoC

Programming and Debugging Tools v12.5 introduces programming and debugging of PolarFire SoC using FlashPro Express and SmartDebug.

Device and Package	Part Number
Device MPFS250T, Package FCVG784	
	MPFS250T_ES-FCVG784_EvalE
	MPFS250T_ES-1FCVG784_EvalE
Device MPFS250T, Package FCSG536	
	MPFS250T_ES-FCSG536_EvalE
	MPFS250T_ES-1FCSG536_EvalE

FlashPro Express

Support PolarFire SoC Programming using Job file generated by FlashPro Express.

SmartDebug

In addition to supporting all the features currently available for PolarFire, SmartDebug supports eNVM debug for PolarFire SoC. The following is the list of supported debug capabilities:

- Transceiver Debug,
- Active Probe,
- Life Probe,
- Fabric Hardware Breakpoint (FHB),
- LSRAM/uSRAM read and write,
- sNVM read, and
- eNVM read.

2.2 Support Embedded FlashPro6 Programmer on the iCicle Kit

Programming and Debugging Tools v12.5 introduces support of the PolarFire SoC device on the iCicle Kit using the embedded FlashPro6 Programmer.

The Embedded Programmer on iCicle Kit is supported on the following operating systems:

- Windows 10
- RHEL 6.6-6.11 and RHEL 7.2 -7.6
- CentOS 6.6-6.11 and CentOS 7.2-7.6
- Ubuntu 18.04
- OpenSUSE Leap 42.3 (SLE12.3 equivalent)

2.3 FlashPro Express: Developer Mode

With Programming and Debugging Tools v12.5, FlashPro Express introduces Developer Mode support. This mode enables user to load different programming files after the initial FlashPro Express project is created using the Job generated by Libero.

2.4 SmartDebug: I/O Margining Analysis for PolarFire DDR Memory Controllers

With Programming and Debug Tools v12.5, SmartDebug introduces the new Debug DDR Memory tool for DDR3/DDR4/LPDDR3. This tool retrieves the status and result from the PolarFire DDR Training IP, and allows users to visualize the margin on the DDR I/Os.

2.5 SmartDebug: Transceiver Debug Action Recording

With Programming and Debug Tools v12.5, SmartDebug introduces the capability to record the transceiver register read and write sequence when a transceiver debug operation is executed, with the exception of Eye Monitor / Persistent Eye Monitor.

3 Resolved Issues

The following table lists the customer-reported SARs resolved in Libero SoC v12.5. Resolution of previously reported “Known Issues and Limitations” is also noted in this table.

Case Number	Description
493642-2706750810	<p>XCVR SmartBERT IP patterns and PMA patterns test issue on single/multiple lanes.</p> <p>Resolution: Running a PRBS test using SmartBERT after conducting a XCVR PMA PRBS test on another lane resulted in errors and inconsistent behavior on the lanes. This sequencing problem between PRBS tests has been resolved in Libero SoC v12.5.</p>
493642-2716781171	<p>Active Probes: Probe read on MPF500T device for a few signals shows unexpected data.</p> <p>Resolution: This issue has been resolved in Libero SoC v12.5. Probes are fully working for the MPF500T device.</p>
493642-2727638971	<p>Disable PRBS tests from XCVR PMA for PCIe lanes.</p> <p>Resolution: PRBS tests are not allowed for PCIe lanes. These tests are disabled in Libero SoC v12.5.</p>
493642-2719750985, 493642-2722233076	<p>FP5 shows 4MHz clock, even if the user sets the TCK to 1 MHz.</p> <p>Resolution: Scan chain always runs at 1MHz to ensure correctness. User-selected TCK is set to run user-selected action.</p>

4 Known Issues and Limitations

4.1 SmartDebug

Family	Description
All Families	<p>In SmartDebug Stand-Alone, SmartDebug operations fail when programming-related steps such as PROGRAM/ERASE/ DEVICE_INFO, Scan Chain, and Auto-Construct Chain steps are run multiple times from the Programming Connectivity and Interface UI during a debug session.</p> <p>Workaround: Close and reopen the debug project to continue debugging the device.</p>
All Families	<p>Export TCL for program action from Standalone SmartDebug exports two additional parameters in the command "run_selected_actions". If this command is executed using execute script, the program action fails.</p> <p>Workaround: Remove the parameters from the command and then execute the script.</p>
PolarFire SoC	<p>The ENVM Debug option is not available if no ENVM client is configured or if a client is configured as a placeholder in Libero. However, users can run the TCL script from SmartDebug as page view to retrieve the content from the device.</p>
PolarFire SoC PolarFire	<p>When Dual mode PCIe design is considered in SmartDebug, the following issues are observed in the PCIe debug feature:</p> <ul style="list-style-type: none"> • For dual-PCIe designs that have PCI0 and PCIe1 controllers, only PCIe1 is shown in the UI. PCIe0 is not shown in the UI. • When PCIe0 Lane is selected, the LTSSM state is shown for the PCIe1 design, but not for PCIe0 . LTSSM state is shown for the PCIe1. • Data Rate, Link Width, and all are shown for PCIe1, but not for thePCI0.
PolarFire	<p>Compile fails when FHB auto-instantiation is enabled on designs containing IOD/DDR macros.</p>

4.2 Programming

PolarFire SoC	Embedded FlashPro6 on iCicle board supports TCK between 4MHz and 20MHz. TCK is set to 4MHz when a frequency lower than 4MHz is selected.
PolarFire SoC	iCicle embedded programmer has a longer programming time in Linux than in Windows.
PolarFire SoC	Embedded FlashPro6 Programmer on iCicleKit does not support SPI-Flash read back on Windows.
PolarFire SoC PolarFire	FlashPro Express developer mode is introduced in the v12.5 release. In developer mode, different SPI Flash files can only be loaded into a device that has SPI Flash file loaded previously. Otherwise, they cannot be loaded.
SmartFusion2 Igluo2	FP5 - Device Info log displays the wrong CheckSum and Design name during SPI Slave programming.
PolarFire	<p>Supported Micron SPI Flash Memory Devices</p> <p>This release supports only the following Micron SPI Flash memory devices:</p> <ul style="list-style-type: none"> • Using FlashPro5: MT25QL01G only • Using FlashPro6: all members of N25Q and MT25Q device families <p>Note: Contact Microchip Technical Support about support for Flash memory devices from other vendors and device families using FlashPro6.</p>

5 System Requirements

The Programming and Debug Tools v12.5 release has the following system requirements:

- 64-bit OS
 - Windows 7, or Windows 10 OS
 - RHEL 6.6-6.11, RHEL 7.2-7.6
 - CentOS 6.6-6.11 and CentOS 7.2-7.6
 - Ubuntu 18.04
 - Note:** FlashPro5 is not supported with Ubuntu.
 - OpenSUSE Leap 42.3 (SLES 12.3 equivalent)
- A minimum of 16 GB RAM

Note: Setup instructions for using Programming and Debug Tools v12.3 on Red Hat Enterprise Linux OS or CentOS are available in [UG0710 Libero SoC Linux Environment Setup User Guide](#).

6 Download Libero SoC v12.5 Programming and Debug Tools

Click the following links to download Programming and Debug Tools v12.5 on Windows and Linux operating systems:

- [Windows Download](#)
- [Linux Download](#)

Note: Installation requires administrator privileges to the system.

7 Appendix: Sample Programming and SmartDebug Times Using FlashPro5/FlashPro6

The tables in this appendix show sample programming times and SmartDebug runtimes using FlashPro5 and FlashPro6 programmers.

7.1 Microsemi FPGA Array Programming

The following table shows sample PPD programming times of the FPGA Array.

Devices ¹	PPD Programming Time ² (mm:ss)		
	FlashPro5	FlashPro6	
	TCK=4MHz USB 2.0	TCK=4MHz USB 2.0/3.0	TCK=20MHz ³ USB 2.0/3.0
M2S/A2GL 050	2min 9sec	2min 10sec	2min 2sec
M2S/A2GL 150	4min 21sec	4min 19sec	3min 54sec
RTG4	2min 10sec	1min 56sec ⁴	1min 33sec ⁴
MPF100	39sec	28sec	23sec
MPF200	1min 3sec	43sec	28sec
MPF300	1min 33sec	1min 4sec	43sec
MPF500	1min 57sec	1min 34sec	1min

¹FlashPro6 supports JTAG programming for all SmartFusion2, IGLOO2, RTG4 and PolarFire devices.

²To benefit from the improved programming time using FlashPro6, use the PPD file format for SmartFusion2, IGLOO2, and PolarFire devices.

³To ensure successful programming at 20MHz TCK, take appropriate steps to ensure signal integrity of JTAG signals.

⁴New and improved programming time for RTG4 starting with Libero SoC/FlashPro Express v12.3 and later.

7.2 SPI Flash Programming

The following table shows sample SPI Flash Programming time using the PolarFire Splash Kit.

(N25Q00AA13GSF40G / MT25QL01G BBB8ESF-0SIT TR) ¹ 10MByte Data	SPI Flash Programming Time				
	FlashPro5		FlashPro6 ²		
	TCK = 4MHZ	TCK = 15MHz ³	TCK = 4MHZ	TCK = 15MHz ³	TCK = 20MHz ³
	USB 2.0	USB 2.0	USB 2.0/3.0	USB 2.0/3.0	USB 2.0/3.0
Erase and Program SPI Flash ⁴	8min 15sec	4min 58sec	14min 53sec	5min 45sec	4min 54sec
Verify SPI Flash	1hr 57min 38sec	1hr 50min 45sec	16min 33sec	7min 53sec	7min 04sec
Read SPI Flash	2hrs 02min 43sec	1hr 55min 30sec	16min 12sec	7min 36sec	6min 47sec
Erase SPI Flash	18sec	18sec	1min 52sec	1min 50sec	1min 50sec

NOTES:

¹SPI Flash programming has been tested on N25Q00AA and MT25QL01G/MT25QU01G devices only. Contact technical support for other SPI-Flash device support needs.

²FlashPro6 has longer erase and programming times for SPI Flash devices compared to FlashPro5. However, readback and verification times are significantly shorter. As a result, the total combined Erase, Program, and Verify time is significantly lower compared to FlashPro5. Programming time for FlashPro6 will be improved in future releases.

³To program the device successfully at a high TCK frequency, take appropriate to ensure signal integrity of JTAG signals.

⁴SPI Flash programming time may vary from device to device even though the part number is the same. This is due to die to die variation.

7.3 SmartDebug Runtime Samples

The following table shows sample runtimes of some SmartDebug key functions.

SmartDebug Function Runtimes		
SmartDebug Operations	FlashPro5	FlashPro6 ¹
	TCK = 4MHZ	TCK = 4MHZ
	USB 2.0	USB 2.0/3.0
Active Probe Read (13,000 probe points)	28 sec	1 sec
Active Probe Write (13,000 probe points)	35 sec	6 sec
Logical View Read of LSRAM (340 LSRAM Blocks)	20 min	<5 min
Logical View Read to USRAM (32 USRAM Blocks)	1 sec	1 sec
FHB - Waveform dump to VCD file (160 probe points; 1,000 cycles)	7 min	25 sec

¹FlashPro6 SmartDebug runtime is applicable for SmartDebug v12.3 and later only.