PolarFire® SoC MSS Configurator User Guide

Introduction

The PolarFire SoC MSS Configurator provides a graphical user interface that allows embedded software engineers to quickly define the MSS startup state. It exports an XML file that is consumed by the embedded software flow that converts the XML into initialization constructs. Additionally, the tool outputs a CXZ file for inclusion into your Libero design flow. The CXZ file contains information about metadata and port needed by the FPGA designer to complete the connectivity between the MSS and the FPGA fabric.

MSS configurator is available as a standalone application and as part of the Libero® SoC design tool suite. The information in this user guide applies to both.

References

- Configuration of the MSS clocks.
  - For detailed information about the MSS clocking features, see *UG0913: PolarFire SoC FPGA Clocking Resources User Guide* .
- Configuration of the MSS interfaces to the FPGA fabric.
  - For detailed information about the MSS Fabric Interface Controller (FIC) features, see *UG0880: PolarFire SoC FPGA Microprocessor Subsystem (MSS) User Guide* .
- Selection and assignment of the MSS peripherals to the MSS dedicated I/Os and/or the FPGA fabric dedicated peripheral interfaces.
  - For detailed information about the MSS Peripherals features, see *UG0886: PolarFire SoC FPGA Peripherals User Guide*.
- Configuration of the MSS Bank voltages and I/O standards and attributes.
  - For detailed information about the MSS Banks and I/Os features, see *UG0916: PolarFire SoC FPGA IO User Guide*.
- Configuration of the MSS DDR memories (DDR3/L, DDR4, LPDDR3, and LPDDR4).
  - For detailed information about the MSS DDR4, DDR3, LPDDR3, and LPDDR4 features, see *UG0906: PolarFire SoC FPGA DDR Memory Controller User Guide*.
- Configuration of the MSS debug features.
  - For detailed information about the MSS debug features, see *UG0888: PolarFire SoC FPGA Trace and Debug User Guide*.

Table of Contents

1. Installing the PolarFire SoC MSS Configurator

The PolarFire SoC MSS Configurator bundled with Libero is available at the following location in the Libero installation section:

- `Windows: <$Installation_Directory>\Microsemi\Libero_SoC_vX.X\Designer \bin64\pfsoc_mss.exe`
- `Linux: <$Installation_Directory>\Microsemi\Libero_SoC_vX.X\bin64\pfsoc_mss`

The PolarFire SoC MSS Configurator can also be installed as a standalone application.

For information about how to install Libero, see www.microsemi.com/product-directory/design-resources/1750-libero-soc#documents.

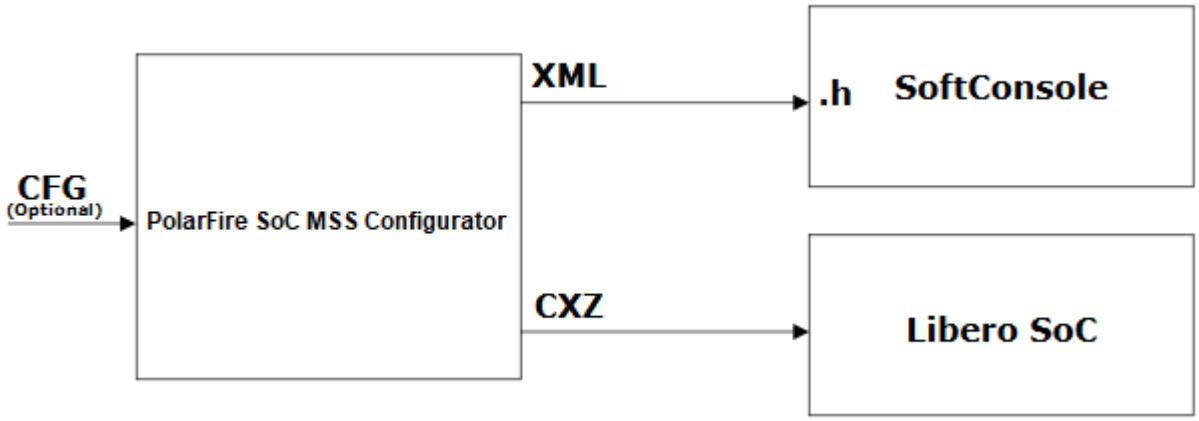
1.1 Input and Output Files

1.1.1 Output Files

The PolarFire SoC MSS Configurator generates the output file formats shown in the following figure.

- **XML Configuration File** — Contains the MSS memory map, clock, DDR memory controller, and peripheral configuration. The XML file is used to generate hardware files required for building the firmware project.
- **CXZ File** — Encapsulates the hardware design of the MSS block and can be imported into Libero SoC project.

Figure 1-1. PolarFire SoC MSS Configurator Block Diagram



1.1.2 Input files

The PolarFire SoC MSS Configurator can be invoked without any input files. A configuration file (.cfg) from an earlier MSS configurator session, can be optionally provided to the PolarFire SoC MSS Configurator.

2. Running the PolarFire SoC MSS Configurator

You can run the PolarFire SoC MSS Configurator in Batch mode or Interactive mode.

2.1 Batch Mode

The PolarFire SoC MSS Configurator application can be executed in the Batch mode for scripted execution as follows:

- Windows:

```
 <Libero SoC or Standalone MSS Configurator installation area>\bin64\pfsoc_mss.exe -
CONFIGURATION_FILE:<absolute path for configuration file name (.cfg)> -
OUTPUT_DIR:<absolute path for output directory>
```

- Linux:

```
<Libero SoC or Standalone MSS Configurator installation area>/bin64/pfsoc_mss -
CONFIGURATION_FILE:<absolute path for configuration file name (.cfg)> -
OUTPUT_DIR:<absolute path for output directory>
```

2.2 Interactive Mode

In the Interactive (GUI) mode, the PolarFire SoC MSS Configurator provides the following high-level options.

Table 2-1. Configurator-Project Menu Options

Option	Description
New	Starts configuring a new MSS subsystem.
Open	Opens a configuration (`.cfg`) file.
Save/Save As	Saves the current configuration of the MSS subsystem to a configuration (`.cfg`) file.
Generate	Generates MSS configuration (`.xml`) and component (`.cxz`) files after configuring the MSS subsystem.
Close	Closes the current configuration (`.cfg`) file.

2.3 Using the PolarFire SoC MSS Configurator GUI

The following section provides information about the MSS Configurator GUI.

2.3.1 Configuration Tabs

The PolarFire SoC MSS Configurator includes the following tabs.

- Clocks
- Fabric Interface Controllers
- I/O Configuration
- I/O REFCLK
- I/O Bank4 and Bank2
- DDR Memory
- Misc

2.3.1.1 Clocks

Use the **Clocks** tab to configure the MSS PLL clock frequency and clock sources. For more information, see UG0913: Microsemi_PolarFire_SoC_FPGA_Clocking_Resources_User_Guide.

The following options are provided.

Table 2-2. MSS Clock Selection Tab

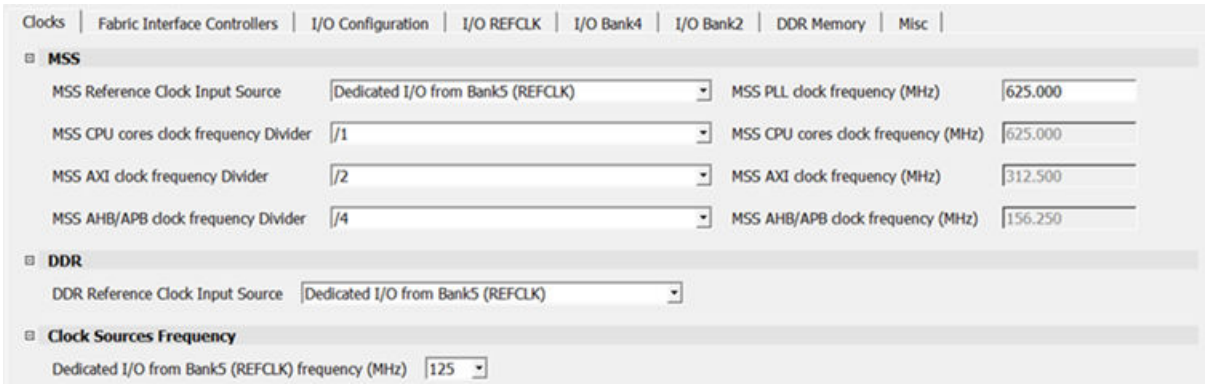
Option	Description
MSS Reference Clock Input Source	MSS can be clocked from either dedicated I/O from Bank 5 (REFCLK) or from North West PLL output. You can select the NW PLL ports or dedicated I/Os from Bank 5 (REFCLK) to source from an off-chip oscillator.
MSS PLL Clock Frequency	Maximum supported frequency for the CPU cores is 625 MHz. You can set the frequency value of up to 625 MHz. All MSS clock frequencies are derived from this setting.
MSS CPU cores clock frequency Divider	The MSS CPU clock frequency is based off the MSS PLL clock frequency and is set using the divider values of /1, /2, /4, or /8. The frequency must be greater or equal to the MSS AXI clock, and can have a maximum value of 625 MHz.
MSS AXI clock frequency Divider	The MSS AXI clock frequency is based off the MSS CPU clock frequency and is set using the divider values of /1, /2, /4, or /8. The frequency must be greater or equal to MSS AHB/APB clock, and can be a maximum value of 312.5 MHz.
MSS AHB/APB clock frequency Divider	The MSS AHB/APB clock frequency is based off the MSS CPU clock frequency and is set using the divider values of /1, /2, /4, or /8.The maximum supported frequency is 156.25 MHz.
DDR Reference Clock Input Source	You can select the NW PLL ports or I/Os from Bank 5 to source from an off-chip oscillator.

Note: The **DDR Reference Clock Input Source** option appears only when the DDR Memory type is selected from the **DDR Memory** tab.

The following figure shows the **Clocks** tab in the PolarFire SoC MSS Configurator. In this example, the following configuration is used:

- Dedicated I/Os from Bank 5 (REFCLK) are selected as the reference clock input source for the MSS. The MSS PLL clock frequency is set to 625 MHz.
- Dedicated I/Os from Bank 5 (REFCLK) are used to source the reference clock input frequency for the DDR subsystem.
- The DDR clock source and MSS clock source are set to 125 MHz.

Figure 2-1. Clocks Tab



For more information about configuring the MSS DDR subsystem, see DDR Memory.

2.3.1.2 Fabric Interface Controllers

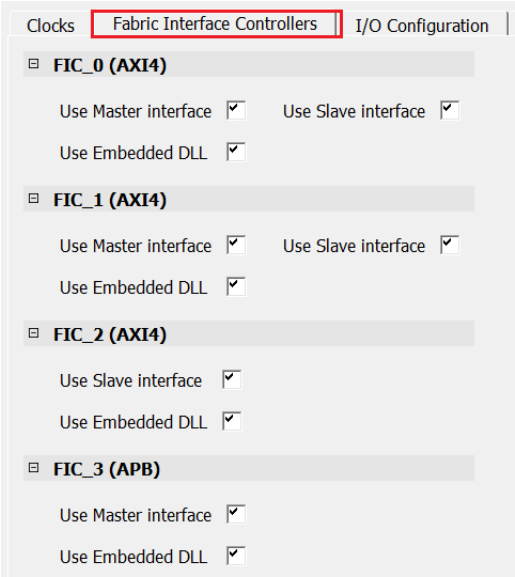
Using the **Fabric Interface Controllers** tab, any combination of **FIC_0**, **FIC_1**, **FIC_2**, **FIC_3** can be enabled and configured to support Master and Slave interfaces. For more information, see UG0880: PolarFire_SoC_FPGA_MSS User Guide

FIC_0, **FIC_1** and **FIC_2** support AXI4 interfaces, while **FIC_3** supports APB.

FIC_0 and **FIC_1** have both master and slave interfaces to and from the FPGA fabric, while **FIC_2** and **FIC_3** support slave or master interfaces, respectively.

The following figure shows all FIC options available and enabled. By default, the DLLs of all the FICs are enabled.

Figure 2-2. Fabric Interface Controllers Tab

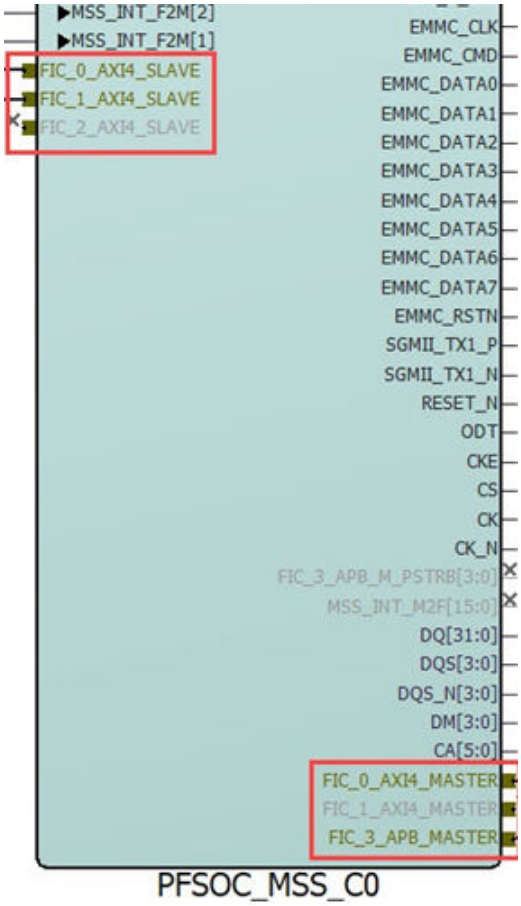


Note: The FIC interface can operate up to 250 MHz. The FIC clock is independent of the MSS clock. If the frequency of the FIC block is greater than or equal to 125 MHz, the embedded DLL must be enabled for removing clock insertion delay. If the frequency of the FIC block is less than 125 MHz, the embedded DLL must be bypassed.

When a master interface is enabled for a FIC, that master interface must be connected to a slave in the fabric. When a slave interface is enabled for a FIC, that slave interface must be connected to a master in the fabric.

There is clock domain crossing logic in the FIC block to address the asynchronous MSS and Fabric clocks.

Figure 2-3. FIC Interfaces Enabled



Note: The MSS SmartDesign component is visible only after importing the MSS CXZ file.

2.3.1.3 I/O Configuration

Using the **I/O Configuration** tab, you can select the following I/Os for the peripherals:

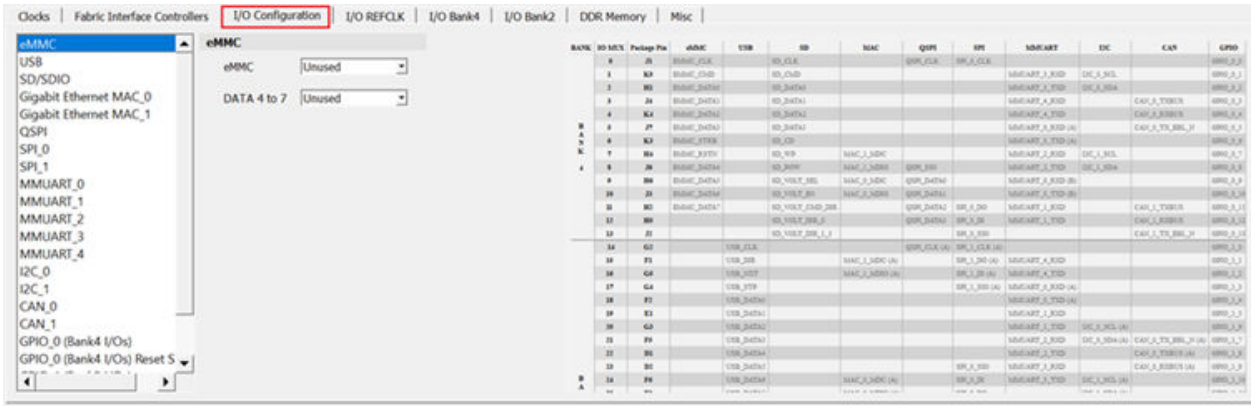
- GPIOs from Bank 2 and Bank 4, which are dedicated to the MSS.
- Fabric I/Os if the dedicated I/Os from Bank 2 and Bank 4 are not available.
- GPIOs from Bank 5 are dedicated to SGMII but can be routed to GMII or MII fabric I/Os. GPIO from Bank 5 are displayed only when Gigabit Ethernet MAC_0 or Gigabit Ethernet MAC_1 is selected.

Note: I/Os from the DDR bank are dedicated to the DDR Controller in the MSS.

For more information, see UG0880: PolarFire_SoC_FPGA_MSS User Guide

The following figure shows the **I/O Configuration** tab on the PolarFire SoC MSS Configurator.

Figure 2-4. I/O Configuration Tab



By default, all peripherals are marked as unused. To include peripherals that are required in the design, select the peripheral from the left-hand side of the window and use the corresponding drop-down to assign MSS I/Os or fabric I/Os.

The I/Os associated with the following peripherals are dedicated and cannot be assigned to fabric I/Os:

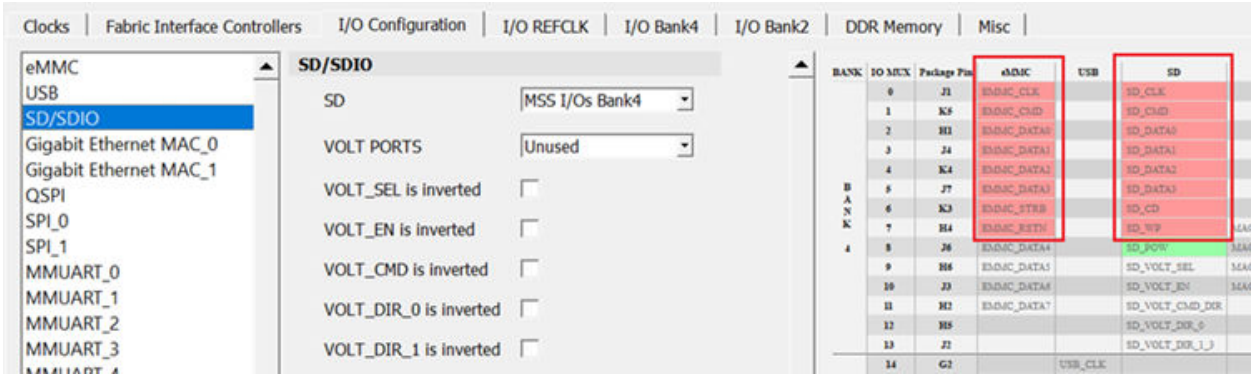
- USB peripherals are dedicated in Bank 2.
- eMMC peripherals are dedicated in Bank 4.
- SD/SDIO peripherals are dedicated in Bank 4.

Note: If the I/Os for a peripheral are selected in a bank, you cannot select the same I/Os for another peripheral from the same bank. If you try, the tool generates the following warning message in the log window:

Figure 2-5. Error Message

For example, eMMC and SD cannot be used simultaneously as shown in the following figure.

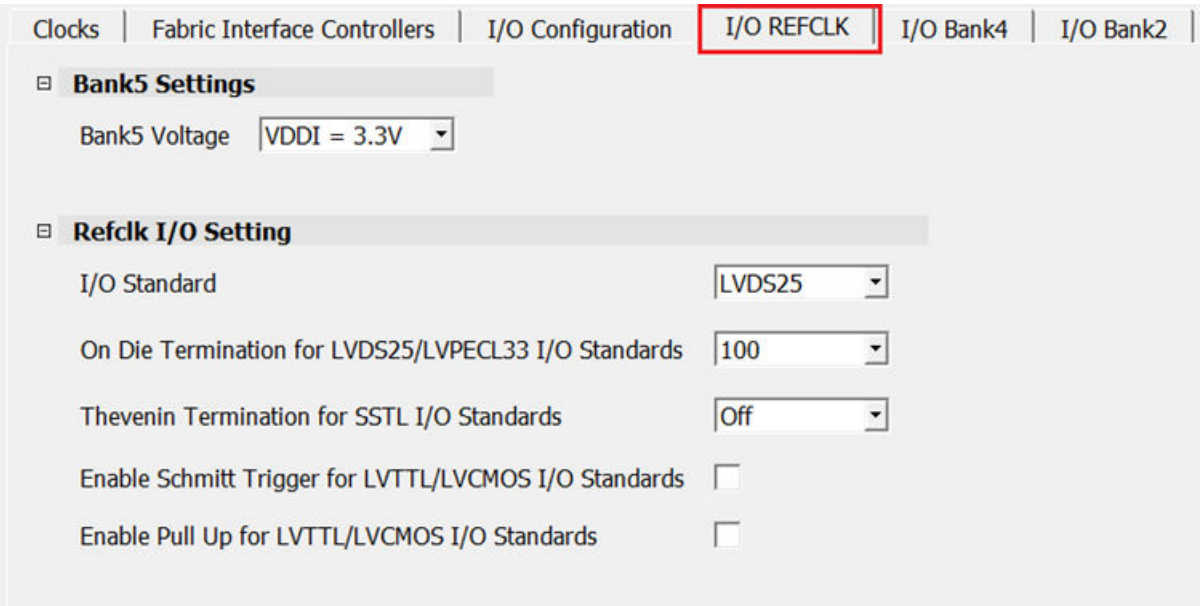
Figure 2-6. Overlapping I/O Warning



2.3.1.4 I/O REFCLK

Using the **I/O REFCLK** tab, you can select electrical characteristics of the Bank 5 I/Os, as shown in the following figure. The tool generates a warning in the log window for unsupported selections.

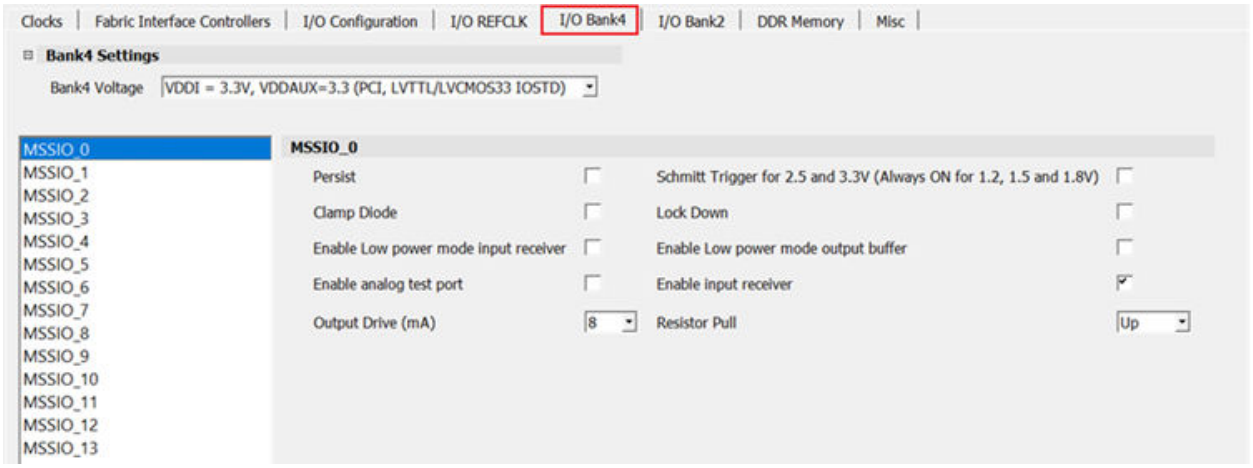
Figure 2-7. I/O REFCLK Tab



2.3.1.5 I/O Bank4 and Bank2

The MSS I/Os are available across Bank 4 and Bank 2. The **I/O Bank4** and **I/O Bank2** tabs allow you to select the electrical characteristics of the MSS I/Os.

Figure 2-8. I/O Bank4 Tab



2.3.1.6 DDR Memory

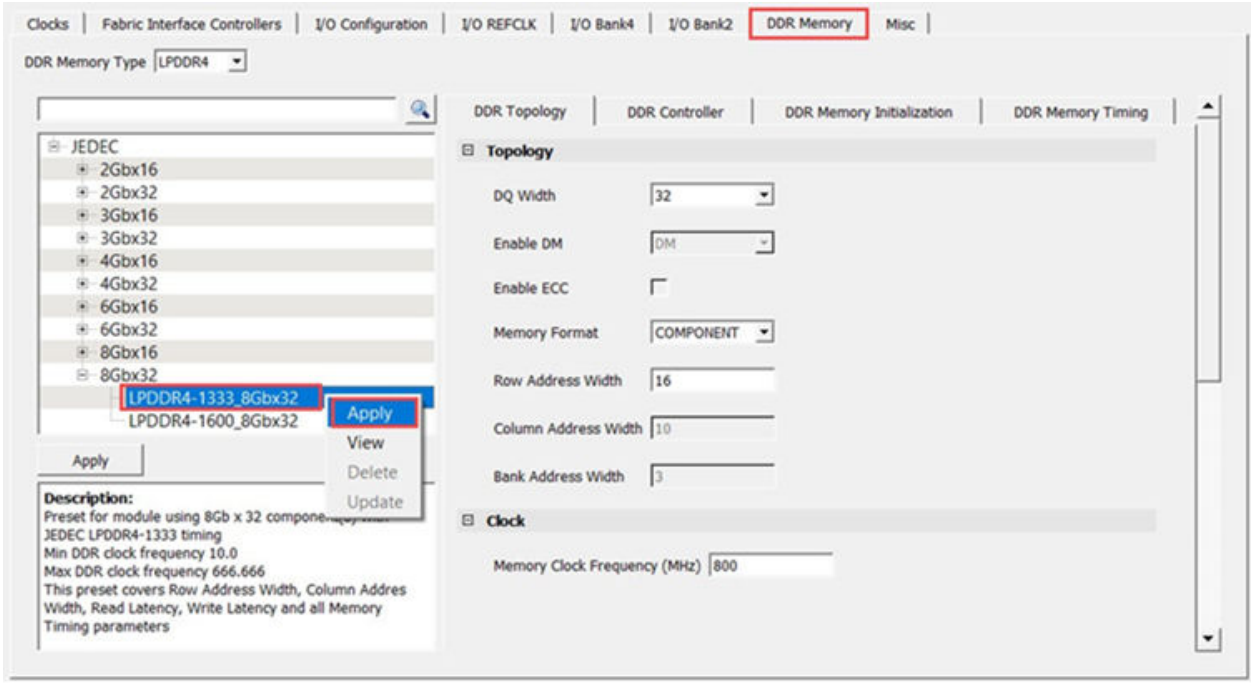
You first select the required DDR type from the **DDR Memory Type** pulldown. The DDR configuration options are available on the **DDR Topology**, **DDR Controller**, **DDR Memory Initialization**, and **DDR Memory Timing** tabs (see the following Figure 2-9).

For more information, see UG0906: PolarFire SoC FPGA DDR Memory Controller User Guide.

The **DDR Topology** tab, in the Figure 2-9 figure, controls the physical aspects of the memory, such as data and address widths, enabling of ECC and DM, and setting the clock frequency.

- For DDR3 and DDR4, the **COMPONENT**, **UDIMM**, **RDIMM**, **LRDIMM**, and **SODIMM** memory formats are supported.
- For LPDDR3/4, only the **COMPONENT** memory format is supported.

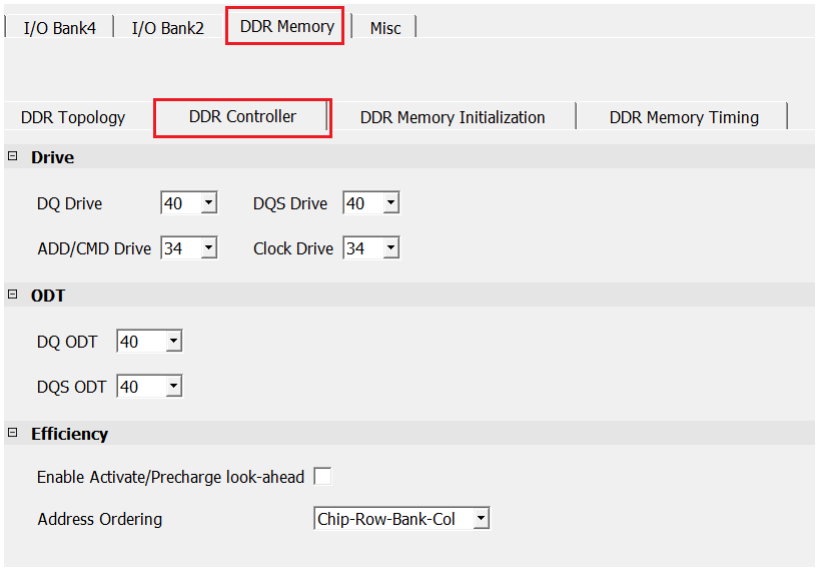
Figure 2-9. DDR Memory Tab



Note: Configure the DDR parameters according to the datasheet from the DDR vendor.

The **DDR Controller** tab controls the DQS Drive, ODT, Precharge look-ahead, and address ordering.

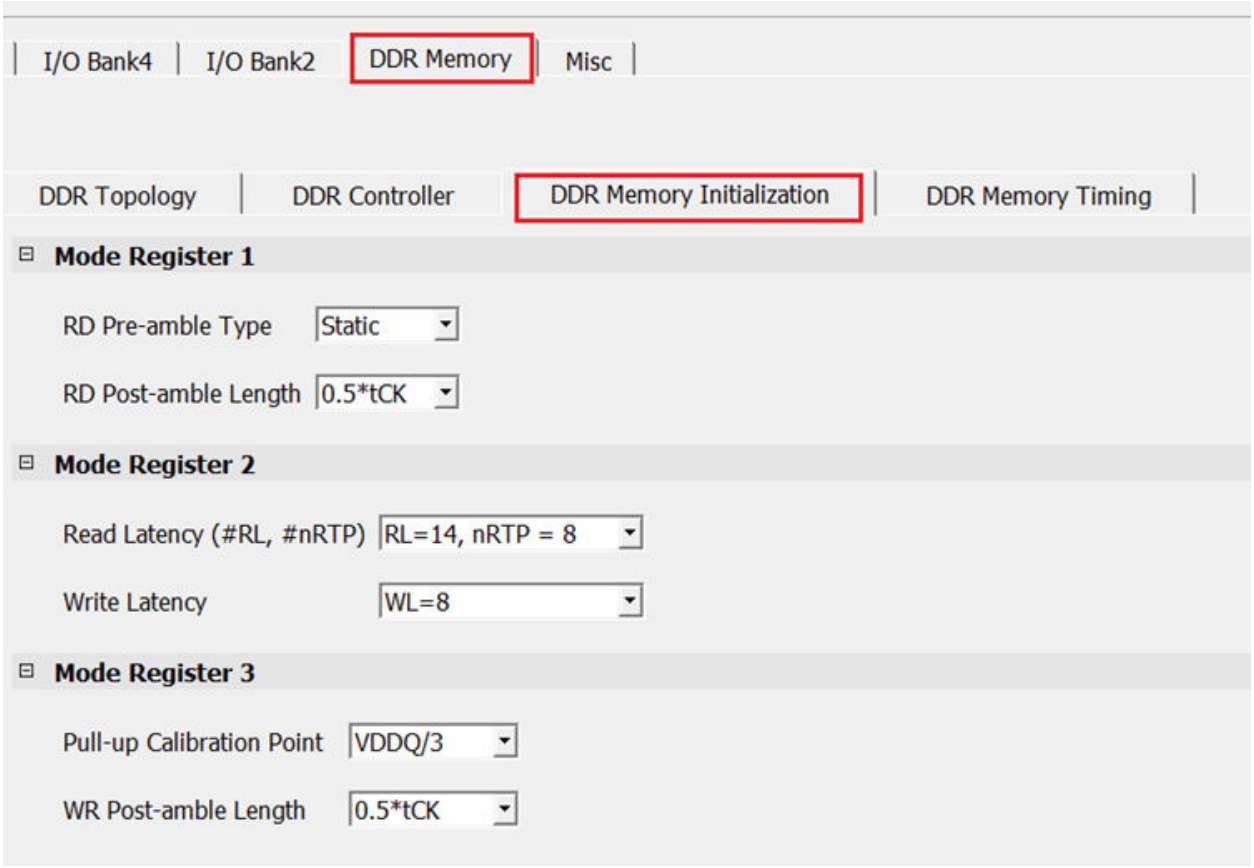
Figure 2-10. DDR Controller Tab



The **DDR Memory Initialization** tab controls the DDR mode register configuration according to the JEDEC specification. In the PolarFire SoC FPGA DDR architecture, these parameters are passed to the start-up code running on the E51 monitor core, which then performs the DDR initialization sequence and configures the mode registers.

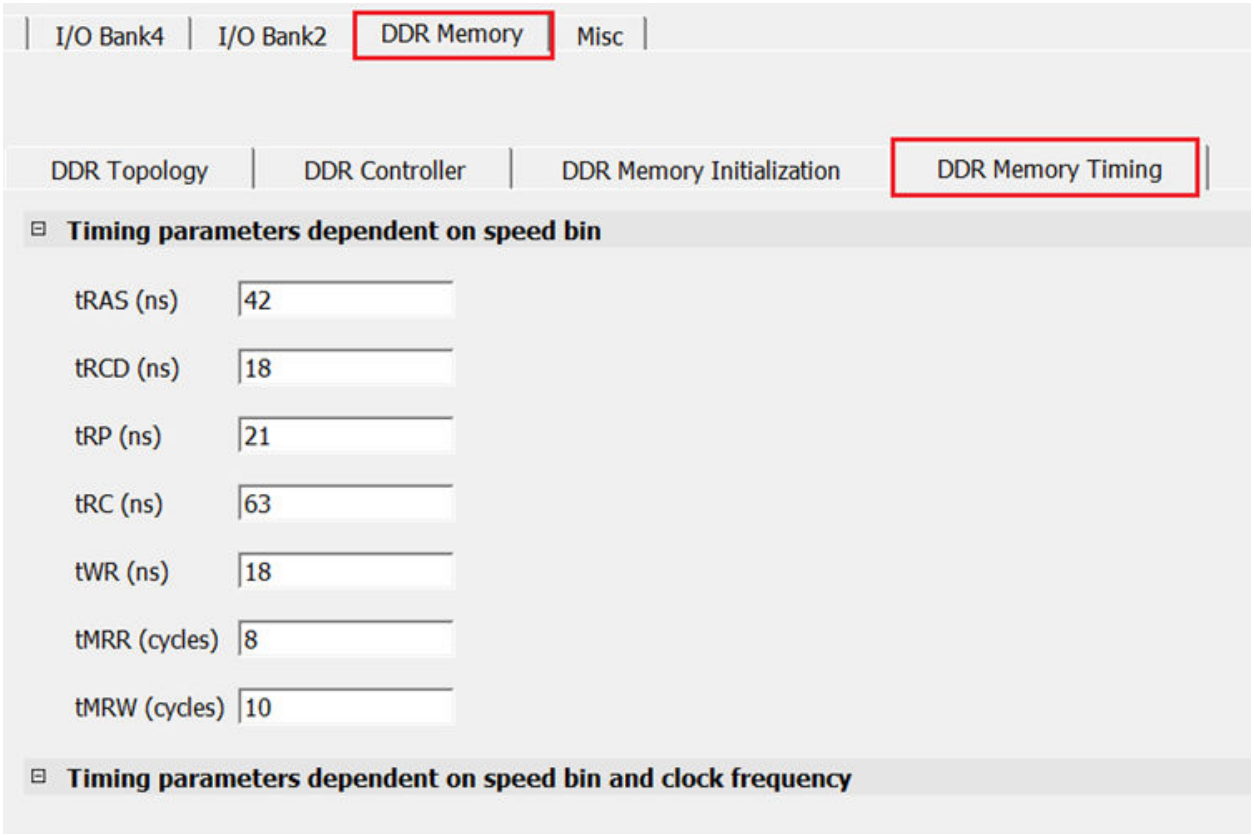
The following figure shows the memory initialization configuration.

Figure 2-11. DDR Memory Initialization



The **DDR Memory Timing** tab controls the timing parameters, which are translated to the appropriate configuration values for the DDR subsystem IP.

Figure 2-12. DDR Memory Timing

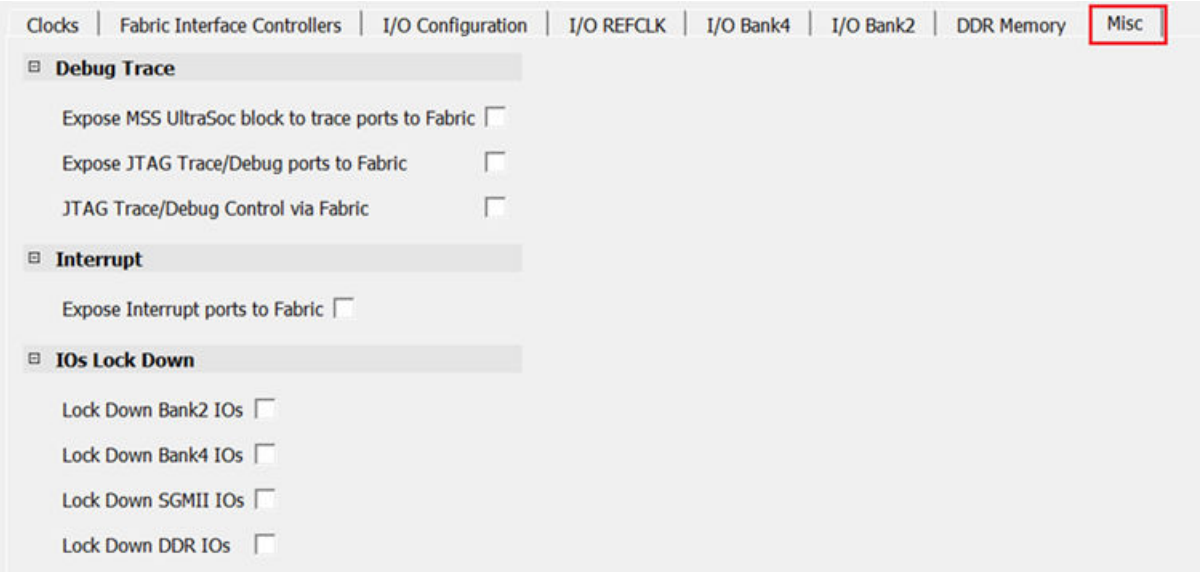


2.3.1.7 Misc

Use the **Misc** tab to enable the following options:

- Trace functionality
- JTAG (Debug) functionality
- Interrupts to/from MSS
- Lock down of Bank 2 and Bank 4 I/Os
- Lock down of DDR and SGMII I/Os

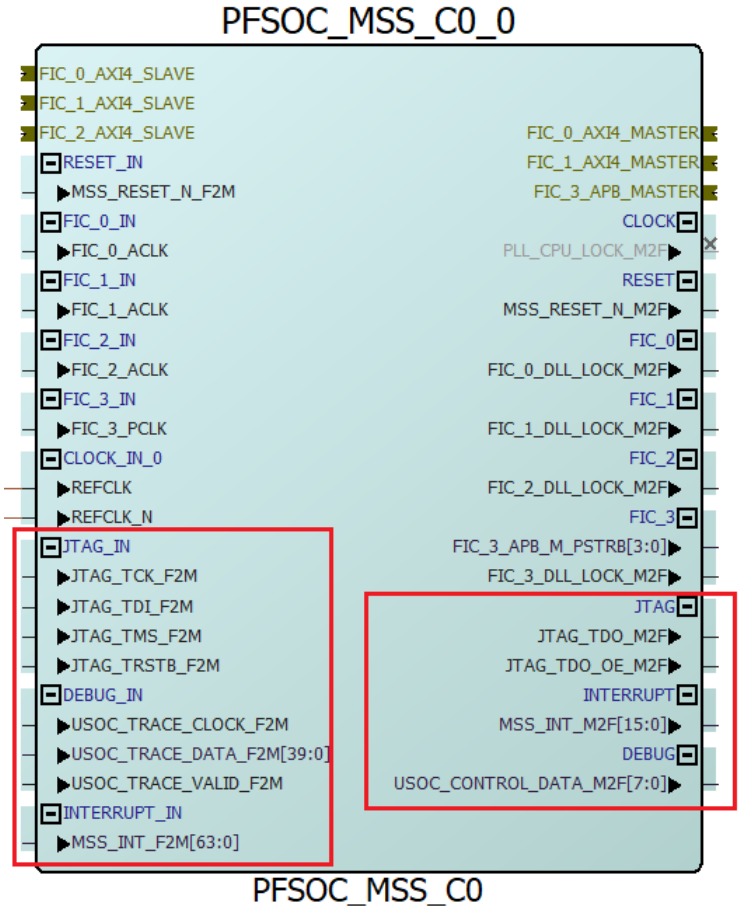
Figure 2-13. Misc Tab



For more information, see UG0888:PolarFire_SoC_FPGA_Trace_and_Debug User Guide.

By default, these options are marked as unused. When any of the options are enabled, the corresponding ports are exposed on the MSS block (see the following figure).

Figure 2-14. PFSOC_MSS_C0_0 Jtag Trace Enabled

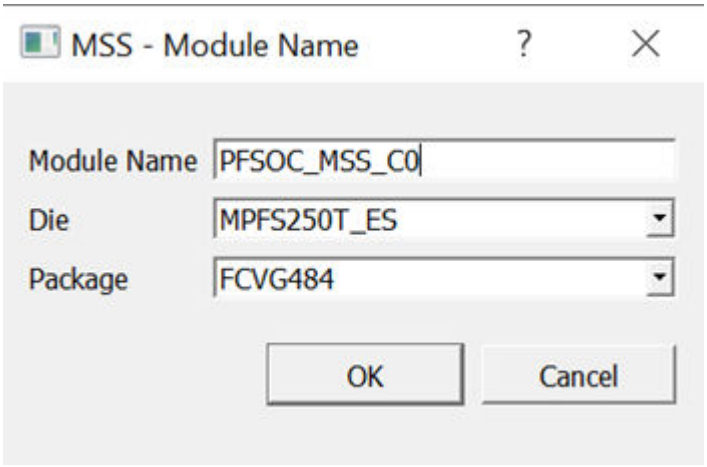


3. Creating a Project and Configuring MSS

To create a project and configure MSS:

1. Launch the PolarFire SoC MSS Configurator (`pfsoc_mss`) in one of the following ways:
   - Libero SoC installation directory
   - Standalone MSS installation area
   - Windows Start menu
2. Create a new project using **Project > New**.
3. Enter a module name (for example `PFSOC_MSS_C0`), and then select the appropriate die and package.

Figure 3-1. MSS - Module Name Dialog Box

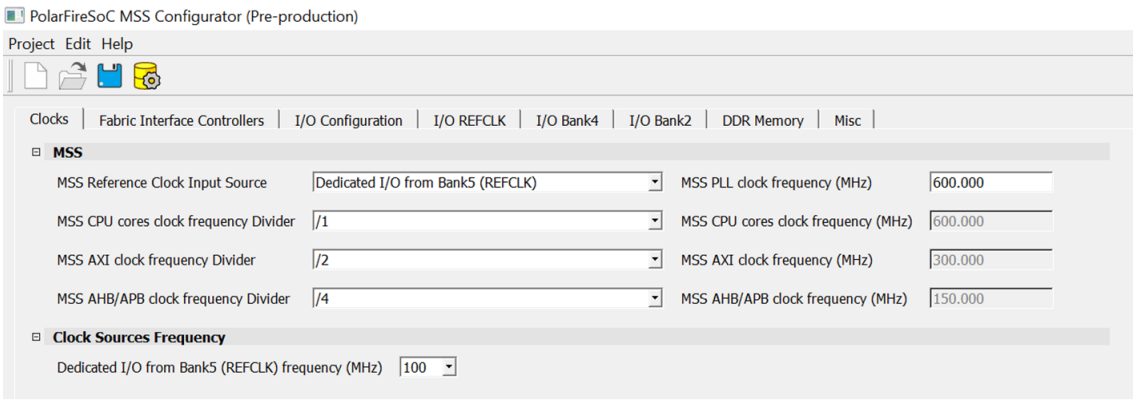


Notes: The module name you enter in this dialog box appears in the following places:

- File names of the PolarFire SoC MSS Configurator generated outputs at the specified output/generation directory.
- MSS component file(`<module_name>.cxz`)
- MSS XML configuration file (`<module_name>_mss_cfg.xml`)
- MSS configuration file corresponding to the current MSS configuration that is generated (`<module_name>.cfg`)
- MSS configuration report file (`<module_name>_Report.html`)
- Component/module name of the MSS component (`cxz`) that can be imported to a Libero SoC project.

The MSS configurator tabs appear (see the following figure).

Figure 3-2. MSS Configurator Tabs



4. Configure **Clocks**, **Fabric Interface Controllers**, **I/O Configuration**, **DDR Memory**, and **Misc settings**.

5. Click the **Save** option to save the MSS configuration to a .cfg file.
6. From the Save MSS Configuration dialog box:
   – Browse to a directory and create a folder. For example, create `C:\Microsemi\PFSOC_MSS_Configuration`.
   – Enter a file name (for example `PFSOC_MSS_C0)` and click **Save**.
   Note: The file name you enter is for the standalone MSS project only and is not used as the component name.

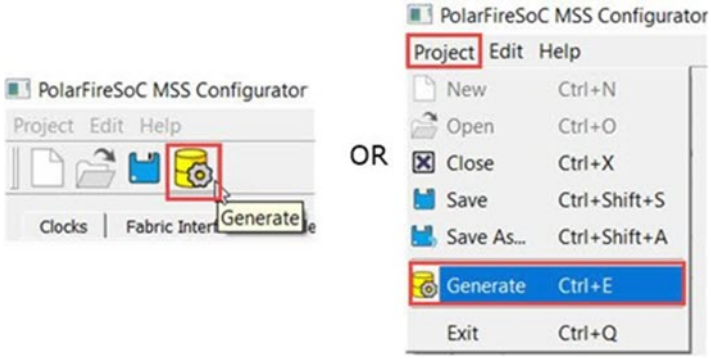
The MSS Configuration is created and saved to the file specified and the Log window shows the following message:
`INFO: Successfully saved MSS configuration in C:/Microsemi/PFSOC_MSS_Configuration/PFSOC_MSS_C0.cfg file`

4. Generating, Importing, and Exporting the MSS Component

4.1 Generating the MSS Component

To generate the MSS component, use the **Generate** option (see the following figure).

Figure 4-1. Generate Option



The configuration file (`module_name.xml`) required for the firmware project and the configuration report file (`module_name.html`) are also generated at this time.

The Log window shows the following messages indicating the generated files:

```
INFO: Successfully generated MSS configuration report to 'C:/Microsemi/PFSOC_MSS_Configuration
\PFSOC_MSS_C0_Report.html'
```

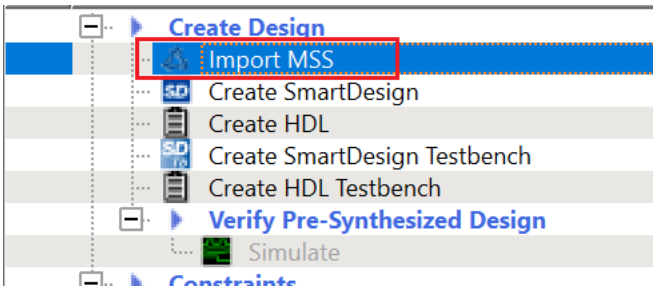
```
INFO: Successfully generated MSS component file to 'C:/Microsemi/PFSOC_MSS_Configuration/
PFSOC_MSS_C0.cxz'
```

4.2 Importing the MSS CXZ File to Libero SoC

To import the `PFSOC_MSS_C0.cxz` file:

1. Use the **Import MSS** option shown in the following figure.

   Figure 4-2. Import MSS to Libero

2. From Design Hierarchy, drag the MSS component to SmartDesign canvas.
3. Build the hierarchy.

Note: Any changes required in the MSS configuration must be performed in the PolarFire SoC MSS Configurator, and the updated `MSS CXZ` file must be re-imported and used in Libero SmartDesign.

4.3 Importing the MSS XML File to SoftConsole

Copy the XML file from:

```
<$Directory>:/Microsemi/PFSOC_MSS_Configuration/PFSOC_MSS_C0_mss_cfg.xml
```

to:

```
<$Installation Directory>:\Microchip\<$SoftConsole_Workspace>\Project_Name\src\platform\config
\xml
```

Note: This step can also be performed using the **Import** option from SoftConsole.

4.4 Exporting the FPGA Design Hardware Platform Information

When using PolarFire SoC, the overall application runs an embedded software application on the RISC-V cores that may use the FPGA fabric to expand the number of I/O peripherals, accelerate software functions using FPGA logic, or control FPGA fabric functions. In these cases, the processor communicates with the FPGA fabric via the MSS Fabric Interface Controllers (FIC) and interrupt ports. The embedded software application must contain the following information to establish this communication properly:

- Fabric blocks like LSRAM, DMA Controller, and PCIe are connected to the AXI interconnect IP on the Fabric side. MSS communicates with these fabric blocks via Fabric Interface Controllers, which connects to the AXI Interconnect IP. The memory addresses of these fabric blocks are specified in the AXI Interconnect IP Configurator. These memory addresses must be specified in the software application.
- In the Libero SoC design, the user must enable the required MSS interrupt ports and other interrupts can be grounded. The corresponding Interrupt Request (IRQ) handler routines must be invoked in the software application for interrupt handling.

Libero SoC v12.5 does not export the FPGA fabric peripheral memory map, interrupt mapping, or peripheral clock frequencies. Therefore, add this information manually in your embedded software projects. For example, if fabric blocks such as LSRAM and DMA Controller are used in the design and interfaced with the MSS through a FIC, then the memory addresses of these fabric blocks must be specified in the user application code for accessing them from MSS.

5. Simulating an FPGA Design Interacting with MSS

The MSS simulation model has been designed to verify the connectivity to the MSS has been properly established with the FPGA fabric logic.

The MSS Simulation model can be used to verify:

- The Fabric—MSS connectivity using the Fabric Interface Controllers (FICs).
- The Fabric—MSS interrupt (M2F and F2M) interface.

For information about how to set up and run the simulation for the PolarFire SoC MSS, see UG0926 User Guide PolarFire SoC FPGA MSS Simulation.

6. Programming the Application Bitstream

To program the application bitstream:

1. Use Libero SoC or FlashProExpress to program the FPGA fabric array, sNVM, eNVM and any security settings.
2. Use Libero SoC to program any eNVM client.

Note: SoftConsole must be used to program the Boot mode.

Alternatively, you can also perform the following steps:

1. Use SoftConsole to program the eNVM with the First Stage Boot image.
    1.1. Select the project you want programmed to eNVM in SoftConsole's **Project Explorer** pane.
    1.2. Click the **PolarFire SoC Boot Mode 1** external tool.

Programming progress messages appear in the Console.

For more information, see *PolarFire SoC Software Development and Tool Flow User Guide*.

7. Sample Project

To view a sample project, see AC489: Building the PolarFire SoC MSS Design .

8. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
A	09/2020	Initial Revision

9. Microchip FPGA Technical Support

Microchip FPGA Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, and worldwide sales offices. This section provides information about contacting Microchip FPGA Products Group and using these support services.

9.1 Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

- From North America, call **800.262.1060**
- From the rest of the world, call **650.318.4460**
- Fax, from anywhere in the world, **650.318.8044**

9.2 Customer Technical Support

Microchip FPGA Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microchip FPGA Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

You can communicate your technical questions through our Web portal and receive answers back by email, fax, or phone. Also, if you have design problems, you can upload your design files to receive assistance. We constantly monitor the cases created from the web portal throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

Technical support can be reached at soc.microsemi.com/Portal/Default.aspx.

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), log in at soc.microsemi.com/Portal/Default.aspx, go to the **My Cases** tab, and select **Yes** in the ITAR drop-down list when creating a new case. For a complete list of ITAR-regulated Microchip FPGAs, visit the ITAR web page.

You can track technical cases online by going to My Cases.

9.3 Website

You can browse a variety of technical and non-technical information on the Microchip FPGA Products Group home page, at www.microsemi.com/soc.

9.4 Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support at (https://soc.microsemi.com/Portal/Default.aspx) or contact a local sales office.

Visit About Us for sales office listings and corporate contacts.

The Microchip Website

Microchip provides online support via our website at www.microchip.com/. This website is used to make files and information easily available to customers. Some of the content available includes:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip design partner program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

Product Change Notification Service

Microchip's product change notification service helps keep customers current on Microchip products. Subscribers will receive email notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, go to www.microchip.com/pcn and follow the registration instructions.

Customer Support

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Embedded Solutions Engineer (ESE)
- Technical Support

Customers should contact their distributor, representative or ESE for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in this document.

Technical support is available through the website at: www.microchip.com/support

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods being used in attempts to breach the code protection features of the Microchip devices. We believe that these methods require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Attempts to breach these code protection features, most likely, cannot be accomplished without violating Microchip's intellectual property rights.
- Microchip is willing to work with any customer who is concerned about the integrity of its code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is "unbreakable." Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

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Quality Management System

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.

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