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## V2.0 MSS Configurator (Pre production) Release Notes

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### References

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- Configuration of the MSS clocks.
  - For detailed information about the MSS clocking features, see [UG0913: PolarFireSoC FPGA Clocking Resources User Guide](#).
- Configuration of the MSS interfaces to the FPGA fabric.
  - For detailed information about the MSS Fabric Interface Controller (FIC) features, see [UG0880: PolarFireSoC FPGA Microprocessor Subsystem \(MSS\) User Guide](#).
- Selection and assignment of the MSS peripherals to the MSS dedicated I/Os and/or the FPGA fabric dedicated peripheral interfaces.
  - For detailed information about the MSS Peripherals features, see [UG0886: PolarFireSoC FPGA Peripherals User Guide](#).
- Configuration of the MSS Bank voltages and I/O standards and attributes.
  - For detailed information about the MSS Banks and I/Os features, see [UG0916: PolarFireSoC FPGA I/O User Guide](#).
- Configuration of the MSS DDR memories (DDR3/L, DDR4, LPDDR3, and LPDDR4).
  - For detailed information about the MSS DDR4, DDR3, LPDDR3, and LPDDR4 features, see [UG0906: PolarFireSoC FPGA DDR Memory Controller User Guide](#).
- Configuration of the MSS debug features.
  - For detailed information about the MSS debug features, see [UG0888: PolarFireSoC FPGA Trace and Debug User Guide](#).

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## 1. Introduction

To provide a seamless experience for both embedded software developers targeting the MSS and the hardware engineers developing a hardware/software solution using the MSS and the FPGA array fabric, the MSS configurator application provides a common tool to configure the PolarFireSoC MSS platform that can be used by both the software engineer and/or the FPGA hardware engineer.

The MSS configurator application can be installed as a stand-alone application or as part of the Libero SoC design tool suite, and provides the following features.

- Configuration of the MSS clocks
- Configuration of the MSS interfaces to the FPGA fabric
- Selection and assignment of the MSS peripherals to the MSS dedicated I/Os and/or the FPGA fabric dedicated peripheral interfaces
- Configuration of the MSS Bank voltages and I/O standards and attributes
- Configuration of the MSS DDR memories (DDR3/L, DDR4, LPDDR3, and LPDDR4)
- Enable the User Crypto processor for “S” devices
- Partition L2 memory into Cache, Loosely Integrated Memory (LIM), or Scratchpad
- Presets for the PolarFireSoC Icicle Kit – Bare Metal and Quad Core Linux
- Configuration of the MSS debug features

For details about the high-level MSS architecture and its features, see the [PolarFire™ SoC product overview](#).

For details about this tool, see the [PolarFireSOC Standalone MSS Configuration User Guide](#).

Download MSS Configurator v2.0 software.

The following are available for download:

- [Stand-alone MSS configurator installer \(Linux\)](#)
- [Stand-alone MSS configurator installer \(Windows\)](#)

**Note:** Windows installations require administrative privileges.

### 2. Software Features and Enhancements

- Enable the User Crypto processor for “S” devices
- Partition L2 memory into Cache, LIM, or Scratchpad
- Presets for the PolarFireSoC Icicle Kit – Bare Metal and Quad Core Linux
- I/O attributes for SGMII I/Os
- Show I/O settings in the report
- Enhancements to I/O banks and Clocking views
- Option to export Verilog netlist
- Indication in the generated report whether fabric interaction will be required

### 3. System Requirements

PolarFireSoC MSS Configurator has the following system requirements.

#### 3.1 Supported 64-bit Operating Systems

- Windows 7 or Windows 10 OS
- RHEL 6.6-6.11 and RHEL 7.2-7.6
- CentOS 6.6-6.11 and CentOS 7.2-7.6
- Ubuntu 18.04
- OpenSUSE Leap 42.3 (SLES 12.3 equivalent)

#### 3.2 Random-Access Memory (RAM) Requirements

Minimum of 4 GB RAM

## 4. Known Issues

### 4.1 Known Issues and Limitations

The following table lists known issues and limitations associated with MSS Configurator v2.0.

**Table 4-1. Known Issues and Limitations Associated with MSS Configurator v2.0**

Family	Description
PolarFire SoC	<p>A bare metal example project using a <a href="#">platform</a> repository release tag earlier than 2020.12 must be updated to release 2020.12 or later when using an xml configuration file generated using MSS Configurator v2.0 or later.</p> <p>Otherwise, the SoftConsole compilation fails with the following error:</p> <pre>The following definitions are missing LIBERO_SETTING_WAY_MASK_M0 LIBERO_SETTING_WAY_MASK_M1 LIBERO_SETTING_WAY_MASK_M2 LIBERO_SETTING_WAY_MASK_M3 LIBERO_SETTING_WAY_MASK_M4</pre> <p>Workaround: Update the platform in your SoftConsole project with release 2020.12 or later of the platform repository. You can download it from: <a href="https://github.com/polarfire-soc/platform">https://github.com/polarfire-soc/platform</a>.</p> <p>Alternatively, you can manually update your MPFS HAL to add the following definitions to the /platform_config/mpfs_hal_config/mss_sw_config.h file in your project:</p> <pre>#define LIBERO_SETTING_WAY_MASK_M0 0x00000000UL #define LIBERO_SETTING_WAY_MASK_M1 0x00000000UL #define LIBERO_SETTING_WAY_MASK_M2 0x00000000UL #define LIBERO_SETTING_WAY_MASK_M3 0x00000000UL #define LIBERO_SETTING_WAY_MASK_M4 0x00000000UL</pre>
PolarFire SoC	<p>While using a platform repository older than 2021.1 release, the L2Cache configuration is set to fixed default values.</p> <p>Workaround: Use the <a href="#">platform</a> repository release 2021.1 or later in the embedded software project to use this new feature added in MSS Configurator v2.0.</p>

**5. Revision History**

<b>Revision</b>	<b>Date</b>	<b>Description</b>
B	12/2020	Contains updated content to reflect v2.0.
A	11/2020	Initial Revision

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