Libero® SoC v2021.1

Release Notes

Introduction

The Libero® system-on-chip (SoC) v2021.1 unified design suite is Microchip's flagship FPGA software for designing with Microchip's latest power efficient Flash FPGAs, SoC FPGAs, and rad-tolerant (RT) FPGAs. The suite integrates industry-standard Synopsys Synplify Pro synthesis and Mentor Graphics ModelSim® simulation with best-in-class constraints management, debug capabilities, and secure production programming support.

Use Libero SoC v2021.1 to design with the following Microchip FPGAs:

- RTG4™
- SmartFusion®2
- IGLOO® 2
- RT PolarFire
- PolarFire SoC

To design with Microchip's older Flash FPGA families, use Libero SoC v11.9 and its subsequent service packs.

To access datasheets, silicon user guides, tutorials, and application notes, visit www.microsemi.com, navigate to the relevant product family page, and click the **Documentation** tab. Development Kits & Boards are listed in the **Design Resources** tab.

Note: Libero SoC v2021.1 does not support Classic Constraint Flow. IGLOO2, SmartFusion2, and RTG4 projects using the "Classic" flow cannot be opened in this release. For information about how to migrate Classic Constraint Flow projects to the Enhanced Constraint Flow, refer to Migrating an Existing Project Created with Classic Constraint Flow to Enhanced Constraint Flow.

Related Release Notes

In addition to these release notes, you may find the information in the following release notes helpful.

- PolarFire SoC MSS Configurator v2021.1 Release Notes

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1. Libero SoC Release Notes

These release notes contain important information about the Libero® system on chip (SoC) v2021.1 unified design suite.

1.1 Customer Notification (CN) Support

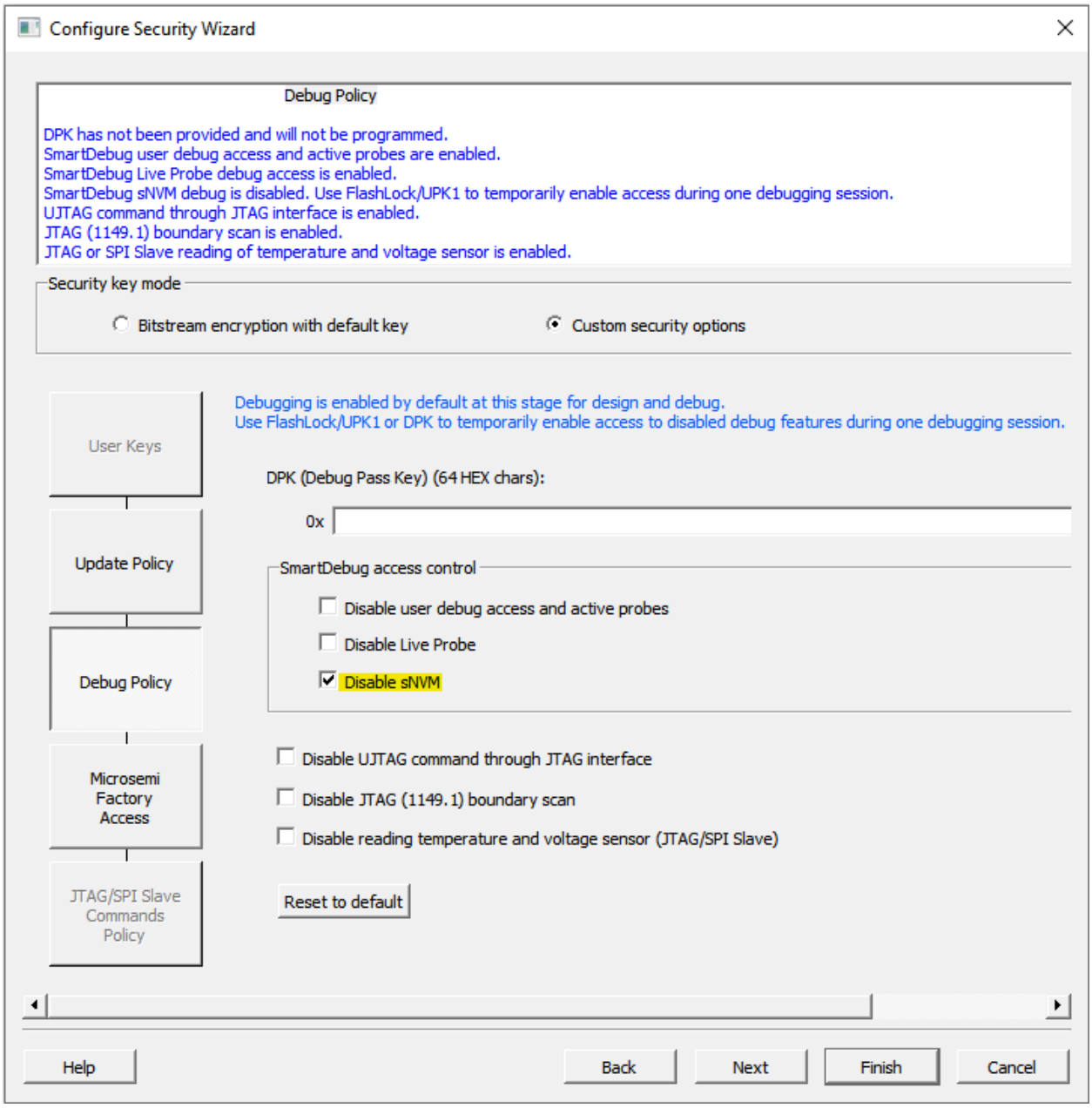
Libero SoC v2021.1 includes changes that address certain important issues.

1.1.1 Disabling SmartDebug Access to sNVM in Libero SoC Debug Policy Settings

For PolarFire, RT PolarFire, and PolarFire SoC devices, Libero SoC v2021.1 fixes an issue where the user setting to disable SmartDebug access to read the sNVM without the user passkey or debug passkey did not take effect. The issue existed for PolarFire devices since v12.0 and PolarFire SoC devices since v12.5. To enforce this debug policy, use v2021.1 to re-run the "Configure Security" step in Libero SoC, re-confirm the user/debug passkey, make sure **Disable sNVM** is checked, regenerate the programming bitstream and reprogram the device with the updated security settings.

For more information, see www.microsemi.com/company/quality/product-notifications/cn/asic-soc-fpga.

Figure 1-1. Disable sNVM Check Box



1.2 New Device Support

1.2.1 PolarFire SoC

Libero SoC v2021.1 introduces FCSG325 package for MPFS025/095T/TS/TL/TLS devices.

For more information, see 10.1 PolarFire SoC New Device Support Matrices.

1.2.2 RT PolarFire

Libero SoC v2021.1 introduces Preliminary timing and power support for RT PolarFire devices.

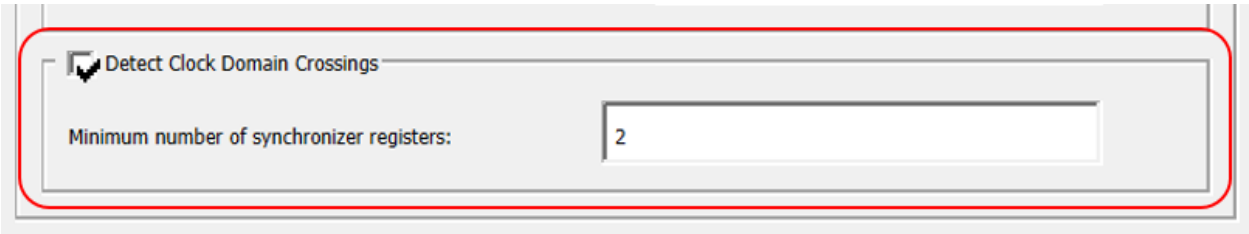
For more information, see 10.2 RT PolarFire Licensing and Device/Package Combination Matrix.

2. Software Features and Enhancements

2.1 New RTL Level Clock Domain Crossing Analysis and Place and Route

Libero SoC v2021.1 introduces a new **Detect Clock Domain Crossings** detection option for analyzing clock domain crossings (CDC) in the RTL design, detecting safe synchronizer circuits according to your specification, and implementing them in Place and Route (P&R). This option is available in the Synthesize Options dialog box and shown in the following figure.

Figure 2-1. Detect Clock Domain Crossings Option



A new report is generated by the Synplify Pro R-2020.09M-SP1-1 tool bundled with Libero SoC v2021.1 listing all CDC situations in the design. The generated CDC report will not contain any synchronizer circuits formed with macros instantiated from the catalog. The generated report, with the name `<root_name>_cdc.csv`, will be visible in the respective Synthesis node of the report view (**Design > Reports**). A summary of the placement of the safe synchronizer registers appears in the P&R log and SmartTime CDC report.

For more information, see the following documents:

- *Libero SoC Design Flow User Guide for PolarFire*
- *Libero SoC v2021.1 Design Flow User Guide for RTG4, SmartFusion2, and IGLOO2*

2.2 SmartTime CDC View Enhancements

SmartTime CDC view in Libero SoC v2021.1 adds an indication of crossings where all paths have safe synchronizers. In addition, you can now cross-probe from this view to the Timing Report Explorer.

For more information, see the *SmartTime User Guide*.

2.3 Interactive Timing Report Explorer Enhancements

The interactive Timing Report Explorer in Libero SoC v2021.1 enhances the expanded path view with a tree structure that is easy to navigate. In addition, you can cross-probe paths to the Chip Planner.

For more information, see the *SmartTime User Guide*.

2.4 New Components View

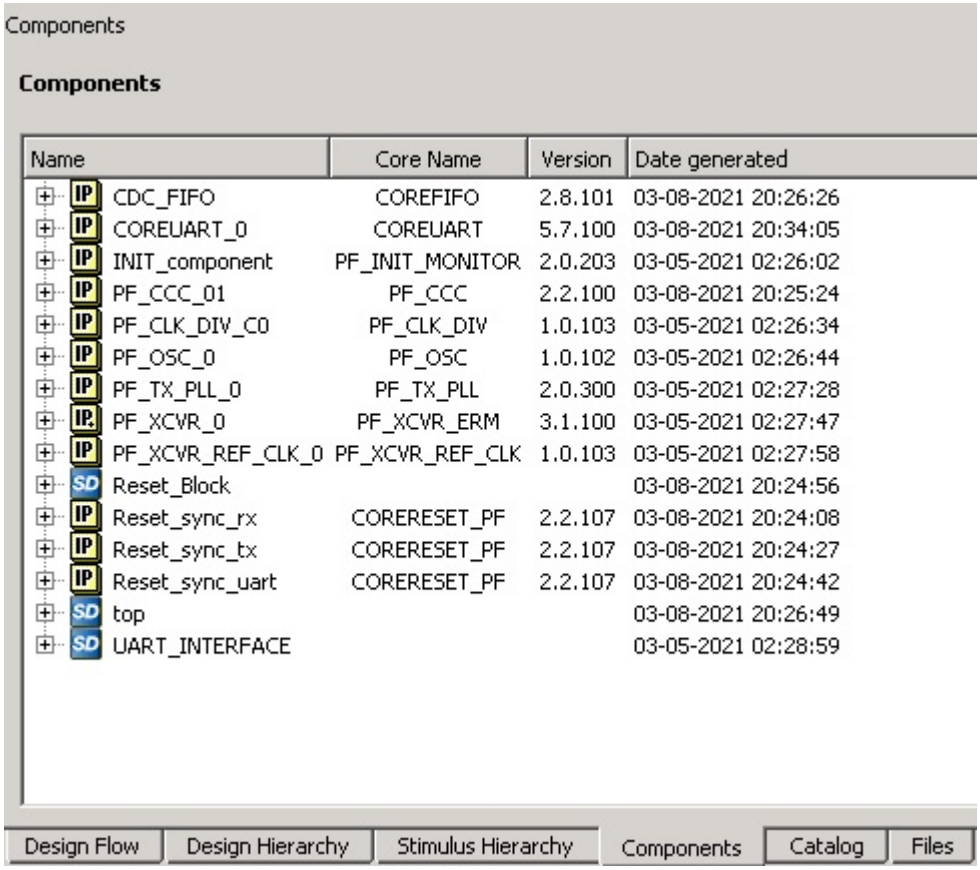
Libero SoC v2021.1 introduces a new Components view that lists all configured core components, blocks, and SmartDesign components in a project.

To open the view, click **View > Windows > Components**. When you open the Component view, a tab in the left area of the Libero SoC lists all configured components and SmartDesigns in the project. Right-clicking a component in the Component view tab displays a menu that is similar to the one that appears when you right-click entries in the Components section of the Design Hierarchy. A component manifest is available for all the components in the view, and can be viewed and accessed by expanding the manifest tree under each component. The **CoreName** and **Version** columns show the appropriate information. The timestamp shown for **Generation** appears in the **Date Generated** column and gets updated when the component regenerates.

For more information, see the following documents:

- *Libero SoC Design Flow User Guide for PolarFire*
- *Libero SoC v2021.1 Design Flow User Guide for RTG4, SmartFusion2, and IGLOO2*

Figure 2-2. Example of Components View



2.5 SmartDesign Enhancements

The SmartDesign canvas in Libero SoC v2021.1 enables the Connection mode by default. The canvas pans automatically when realizing a connection using the Connection mode.

For more information, see the *SmartDesign User Guide*.

2.6 System Verilog Multiple-File Compilation Unit

Libero SoC v2021.1 provides an option to enable the multiple-file compilation unit (MFCU) for System Verilog, so that constructs defined in one compilation unit are visible in a different compilation unit.

For more information, see the following documents:

- *Libero SoC Design Flow User Guide for PolarFire*
- *Libero SoC v2021.1 Design Flow User Guide for RTG4, SmartFusion2, and IGLOO2*

2.7 SmartPower Vectorless Activity Estimation

Libero SoC v2021.1 improves the vectorless activity estimation in SmartPower and reduces its computation time significantly.

For more information, see the *SmartPower User Guide*.

2.8 Synthesis TMR Report

Synplify Pro R-2020.09M-SP1-1 bundled with Libero SoC v2021.1 introduces a new TMR report that lists all of the registers mapped in the design to enable user confirmation that the `syn_radhardlevel=tmr` directive has been implemented. PolarFire, PolarFire SoC, SmartFusion2, and IGLOO2 support this report. The report is available in the Libero SoC **Reports** tab under **Synthesis reports**, and uses the naming format `<root>_tmr.rpt`.

This version also optimizes the TMR area of async-reset-async-set FFs.

For more information, see the *Synplify Pro ME R-2020.09M-SP1-1 FPGA User Guide*.

Figure 2-3. Sample TMR Report

```
Feature          Instance     RTL Name     Implementation-status     Instance type                    Comments
-------------------------------------------------------------------------------------------------------------------------------
register_tmr     dout1        dout1        IMPLEMENTED               register with async set reset    -
register_tmr     dout2        dout2        IMPLEMENTED               register with async set reset    -
===============================================================================================================================
```

2.9 Synplify Pro and Identify

The Synplify Pro and Identify tools bundled in Libero SoC v2021.1 have been upgraded to version R-2020.09M-SP1-1.

Libero SoC already has a synthesis option to optimize for Low power all memory inferred in the design. Users can now change memory inference to `low_power` implementation on an individual instance using the following directive:

```
reg [19:0] mem [0:2047] /* synthesis syn_ramstyle = "low_power" */;
```

If the Low power option is enabled at the design level, you can now change memory inference to `no_low_power` implementation on an individual instance using the following directive:

```
reg [19:0] mem [0:2047] /* synthesis syn_ramstyle = "no_low_power" */;
```

Synplify Pro R-2020.09M-SP1-1 now flags warning messages for unconnected Input pins across the RTL hierarchy.

- `W: CG184 : Removing wire <net_name>, as it has the load but no drivers`
- `W: CG781: Input <pin_name> on instance <inst_name> is undriven; assigning to 0. Simulation mismatch possible. Either assign the input or remove the declaration.`
- `W: CG360: Removing wire <net_name>, as there is no assignment to it.`
- `E: FX114: Pin <pin_name> of instance <inst_name> is undriven. Assign a valid signal to this pin.`

For more information, see the *Synplify Pro ME R-2020.09M-SP1-1 FPGA User Guide*.

2.10 Modelsim ME Pro

The Modelsim ME and Modelsim ME Pro bundled in Libero SoC v2021.1 have been upgraded to version 2020.4 OEM.

Note: Modelsim ME will no longer be bundled with Libero SoC after v2021.1.

2.11 Red Hat Enterprise Linux 8 and CentOS 8 Support

Libero SoC v2021.1 introduces support for Red Hat Enterprise Linux 8 and CentOS 8 (see 7. System Requirements).

For installation information, see the *Libero SoC Linux Environment Setup User Guide*.

3. New Silicon Features and Enhancements

3.1 PolarFire SoC

3.1.1 sNVM Client for Boot Mode2 and eNVM Client for Boot Mode3

Libero SoC v2021.1 provides an sNVM client for Boot mode2 and an eNVM client for Boot mode3.

These clients enable the generation of a complete programming file for applications using each of these Boot modes.

3.1.2 Simulation of MSS Streaming interface in User Cryptoprocessor for “S” Devices

Libero SoC v2021.1 introduces simulation support for the MSS Streaming interface in User Cryptoprocessor for PolarFire SoC “S” devices.

The streaming interface is used when Crypto operates in MSS, Shared-MSS, and Shared-Fab modes. The crypto block can be owned by either the Fabric or MSS, with ownership transferred during operation.

For more information, see the *PolarFire SoC MSS Configurator User Guide*.

3.1.3 Post Layout Simulation

Libero SoC v2021.1 enables post-layout simulation in PolarFire SoC designs of the fabric cells, Transceiver components, and the MSS interface.

3.1.4 Export Bitstream Advanced Options

Libero SoC v2021.1 adds advanced options to Export Bitstream for SPI bitstream files in PolarFire SoC designs

For more information, see the Libero online help.

3.1.5 SmartDebug MSS Read/Write Access

Libero SoC v2021.1 enables an option to write and read MSS registers on the fly while operating from the SmartDebug GUI.

Note: MPU/PMP must be enabled from MSS configurator for SmartDebug to access the MSS registers.

For more information, see the *SmartDebug User Guide*.

3.2 RT PolarFire

3.2.1 SmartDebug FPGA Hardware Breakpoint

Libero SoC v2021.1 adds FPGA Hardware Breakpoint auto-instantiation (FHB) support for the RTPF500T/TS/TL/TLS devices.

Note: The System Controller Suspended mode must be disabled for FHB operation.

For more information, see the *SmartDebug User Guide*.

3.3 PolarFire, RT PolarFire, and PolarFire SoC

3.3.1 Transceiver Incremental Calibration Option

Libero SoC v2021.1 extends the PolarFire Transceiver Enhanced Receiver Management (ERM) solution to add the incremental calibration options “On-Demand” and “On-Demand and First Lock.”

There are two algorithms available:

- Data Eye Clock Centering (CTLE/DFE)

- DFE Coefficient Calibration (DFE)

Each algorithm can be triggered independently – one port exposed per algorithm type.

For more information, see the *PolarFire FPGA Transceiver User Guide*.

3.3.2 Transceiver REF_CLK Connection to Fabric through Global Network

Libero SoC v2021.1 enables the REF_CLK output pin of PF_XCVR_REF_CLK to drive a fabric global net via a CLKINT instance.

For more information, see the *PolarFire FPGA Transceiver User Guide*.

3.3.3 Transceiver Simulation

Libero SoC v2021.1 introduces simulation capability of PolarFire Transceiver components at both post-synthesis and post-layout stages.

For more information, see the *PolarFire FPGA Transceiver User Guide*.

3.3.4 I/O Recalibration

Libero SoC v12.6 introduced the ability to recalibrate I/Os on-demand for each bank.

Libero SoC v2021.1 allows an individual I/O to opt out of recalibration. I/O recalibration is sometimes required to account for delays or to compensate Vt performance impact.

In PDC or I/O Attribute Editor, select the Drive and Termination Impedance calibration codes from the lane (never changed after first PoR calibration) to opt out of the recalibration done from the fabric. Example:

```
- set_io -port_name A -USE_LANE_CALIB_CODE Yes
```

For more information, see the *PolarFire FPGA User I/O User Guide* and the *UG0725: PolarFire FPGA Device Power-Up and Resets User Guide*.

3.3.5 I/O Configurator Enhancements

Libero SoC v2021.1 extends the PF_IO configurator to enable all possible combinations of I/O registers in both directions along with a dynamic schematic representation of the configured I/O.

The Compile report, I/O Editor, Pin report, and I/O Register Combining report also have been enhanced to include the source constraint information.

For more information, see the *PolarFire FPGA User I/O User Guide*.

3.3.6 Pin Report Board Layout Table

Libero SoC v2021.1.adds a new P&R Pin report (pinrpt_boardlayout.csv) formatted into a table where users can filter selections or sort on any column.

For more information, see the *Libero SoC Design Flow User Guide for PolarFire*.

3.3.7 SmartDebug I/O Tap Delays

Libero SoC v2021.1 permits debugging of source synchronous timing margins for dynamically tuned PF_IOD_GENERIC_RX IP interfaces.

To support this feature, the SmartDebug main page for PolarFire designs shows a **Debug IOD** button when there is a PF_IOD_GENERIC_RX IP instance configured as Dynamic or Fractional Dynamic mode in the design. The button is not shown for designs where the IP is configured in modes other than the ones mentioned above. After the Instance is selected and **Get Training Data** is clicked, the tap delay values are shown for the CORERXIODBITALIGN IP instances that are used to train the instance selected. For the Libero SoC v2021.1 release, CORERXIODBITALIGN IP v2.2.100 is the latest version available.

For more information, see the *SmartDebug User Guide for PolarFire*.

3.3.8 DDR4 Throughput Enhancement

Libero SoC v2021.1 adds bank group interleaving to the DDR4 interface to improve the throughput.

For more information, see the *PolarFire FPGA Memory Controller User Guide*.

3.3.9 New Post-layout Editing of I/O Attributes and Delay Parameters

Libero SoC v2021.1.introduces a new tool in the Design Flow that allows you to tune I/O attributes and external timing without needing to rerun Place and Route. Input is provided using a PDC file. From the Design Flow menu, double-click **Edit Post Layout Design** to open a file selection dialog box for selecting the input file.

In batch flow, you can issue the command `edit_post_layout_design <input.pdc>`.

The PDC file contains one or more invocations of two PDC commands:

- `edit_io`
- `edit_instance_delay`

For more information about these commands, see the *PDC Command User Guide - PolarFire*.

To assist you in knowing which instances can have delays updated by this tool, the Place and Route tool generates a new report file named `<root>_delayinstance.rpt`. This report has an **Editable?** column, with **Yes** and **No** values that indicate whether a delay parameter can be edited by this tool.

The PDC commands fail if the syntax is incorrect, the referenced instances do not exist, or the values are out of legal ranges. If the batch command fails, the layout state of the design does not change. If the batch command succeeds, the layout state changes to reflect the values in the PDC commands, pin report and delay instance report files are regenerated to reflect the latest values, and the downstream tools Verify Timing, Verify Power, Generate FPGA Array Data, and Generate Back Annotated Files are invalidated.

For more information, see the *Libero SoC Design Flow User Guide for PolarFire*.

3.3.10 Synthesis Inference of MATH SIMD Operations

Synplify Pro R-2020.09M-SP1-1 bundled with Libero SoC v2021.1 introduces a new directive to pair two 9x9 multiplications into a single `MATH` block.

Example:

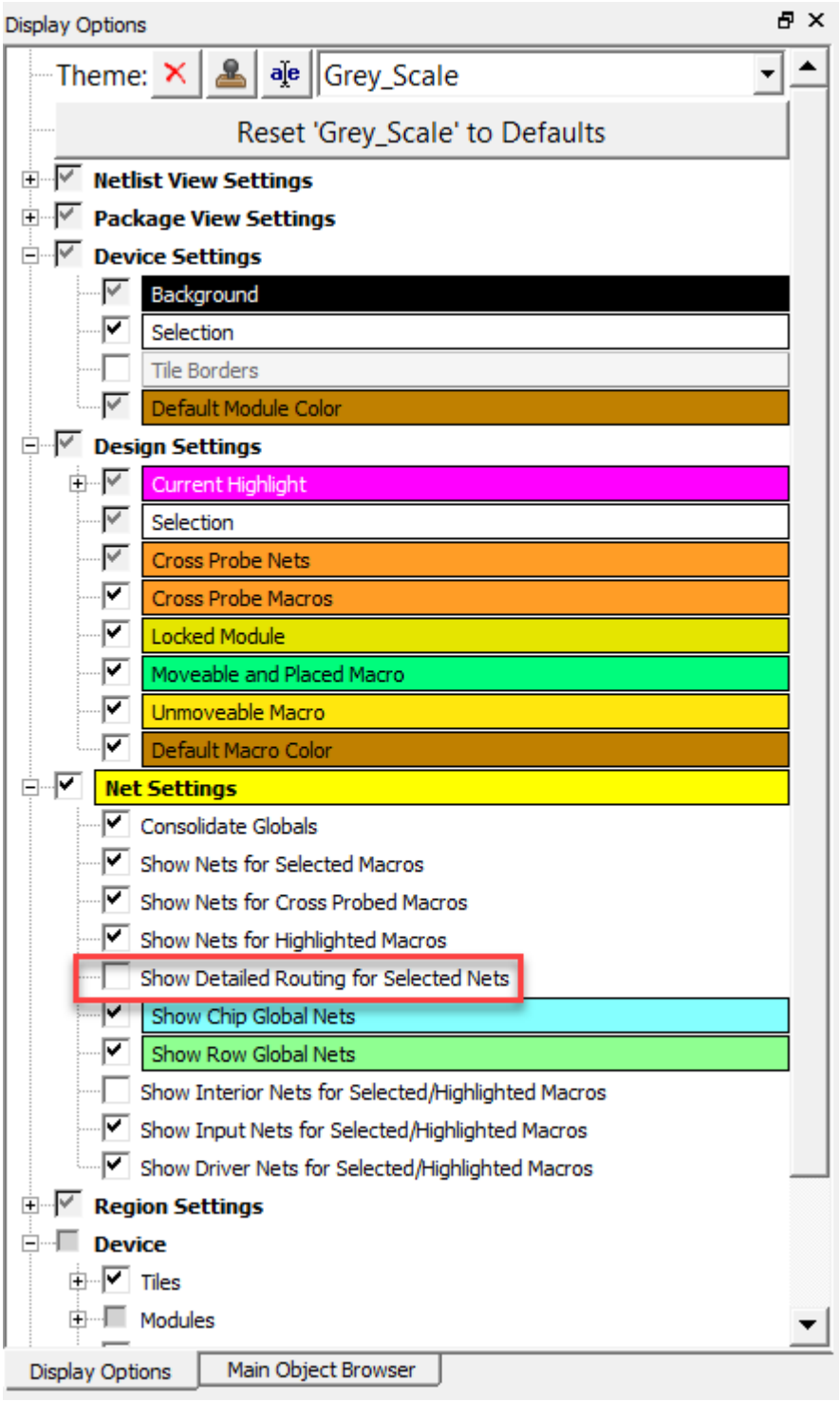
```
module mult_simd(clk, din1, din2, din3, din4, dout1, dout2);
    parameter n = 1;
    input clk;
    input [8:0] din1, din2, din3, din4;
    output [17:0] dout1 /* synthesis syn_multstyle = "simd:1" */;
    output [17:0] dout2 /* synthesis syn_multstyle = "simd:1" */;
    reg [17:0] dout1;
    reg [17:0] dout2;
    always @( posedge clk )
    begin
        dout1 <= din1 * din2 ;
        dout2 <= din3 * din4 ;
    end
endmodule
```

For more information, see the *Synplify Pro ME R-2020.09M-SP1-1 FPGA User Guide*.

3.3.11 Chip Planner Routing View

Libero SoC v2021.1 adds the capability to view post-layout routing in the Chip Planner tool.

Figure 3-1. Show Detailed Routing for Selected Nets



For more information, see the *Chip Planner User Guide*.

3.3.12 SPI Flash Partial Programming

Libero SoC v2021.1 adds partial programming capability to SPI Flash.

For more information, see the *Libero SoC v2021.1 Design Flow User Guide for PolarFire*.

3.3.13 PolarFire Transceiver Sourced Fabric Clocks and Jitter Compensation

PolarFire Transceiver components can source three clocks into the fabric:

- PF_XCVR_LANE#_TX_CLK
- PF_XCVR_LANE#_RX_CLK
- PF_REFCLK _FAB_REF_CLK

These clocks contain high-frequency jitter that Libero does not consider in the timing report and SmartTime. Therefore, users should add clock-uncertainty constraints to these clocks in their designs. The following table shows recommended values for clock uncertainty per clock, resource, and speed-grade.

Table 3-1. Recommended Values for Clock Uncertainty

Clock Type	STD	-1
FAB_REF_CLK on Global	275 ps	200 ps
FAB_REF_CLK on Regional	N/A	N/A
TX_CLK_G on Global	300 ps	225 ps
TX_CLK_R on Regional	225 ps	150 ps
RX_CLK_G on Global	325 ps	250 ps
RX_CLK_R on Regional	250 ps	175 ps

The following example shows a clock-uncertainty constraint that can be added to the user's timing SDC file.

Figure 3-2. Sample Clock-Uncertainty Constraint

```
set_clock_uncertainty -setup 0.150 [ get_pins { PF_XCVR_ERM_LANE2/I_XCVR/LANE0/TX_CLK_R } ]
set_clock_uncertainty -setup 0.175 [ get_pins { PF_XCVR_ERM_LANE2/I_XCVR/LANE0/TX_CLK_R } ]
# TX_CLK and RX_CLK on Globals
set_clock_uncertainty -setup 0.300 [ get_pins { PF_XCVR_ERM_LANE2/I_XCVR/LANE0/TX_CLK_G } ]
set_clock_uncertainty -setup 0.325 [ get_pins { PF_XCVR_ERM_LANE2/I_XCVR/LANE0/TX_CLK_G } ]
# FAB_REF_CLK on Global
set_clock_uncertainty -setup 0.275 [get_clocks PF_DDR4_C0_0/CCC_0/pll_inst_0/OUT1]
```

The automatic management of these constraints will be added in a future release of Libero SoC.

Note: It is also important to add the other required jitter sources as clock uncertainty into your design constraints. See the datasheet for the jitter to be added for components such as PLL, DLL, and RC Oscillator. For input pins that are direct or are inputs to the DLL (but not for a PLL), add the input jitter on the clock input pin to your timing constraints.

4. Migrating Designs to Libero SoC

4.1 Core Enhancements and Upgrades

The following table lists the core enhancements and upgrades.

Table 4-1. Core Enhancements and Upgrades

Core	2021.1 Version	Status	Description
CORERXIODBITALIGN	2.2.100	Production	SmartDebug I/O Tap Delays.
PFSOC_INIT_MONITOR	1.0.205	Pre-production	Fixed synthesis error because of floating AND gate.
RTG4_SRAM_AHBL_AXI	1.0.117	Production	Made change to not expose Port-B Side of ECC signals when using USRAM option.
SmartFusion2/IGLOO2 TPSRAM	1.0.102	Production	Added support for initializing memory files through TCL.
SmartFusion2/IGLOO2 DPSRAM	1.0.102	Production	Added support for initializing memory files through TCL.
SmartFusion2/IGLOO2 URAM	1.0.102	Production	Added support for initializing memory files through TCL.
PF_RGMII_TO_GMII	1.3.102	Production	Repackaged with latest PF_IOD_GENERIC_RX and PF_IOD_GENERIC_TX core versions.
PF_QDR	1.8.105	Production	PF_QDR: CoreQDR BFM simulation: X observed during read for upper addresses.
PF_INIT_MONITOR	2.0.204	Production	Fixed synthesis error due to floating AND gate.
PF_IO	2.0.102	Production	Separate register mode for input/output/oe.
PF_IOD_GENERIC_TX	2.0.109	Production	The PF_IOD GUI does not allow non-integer frequencies.
PF_IOD_OCTAL_DDR	2.0.102	Production	PF_IOD_OCTAL_DDR configuration issues.
PF_IOD_GENERIC_RX	2.1.102	Production	The PF_IOD GUI does not allow non-integer frequencies.

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Core	2021.1 Version	Status	Description
PF_XCVR (Hidden)	2.1.101	Production	Incremental DFE support.
PF_LPDDR3	2.3.112	Production	Add a field to the LPDDR3 Configurator GUI to select the PLL Offset value.
PF_DDR4	2.5.102	Production	DDR4 - QoR - Throughput enhancement (bank group interleaving).
CORESMARTBERT	2.8.101	Production	No functional change. Repackaged with PF_XCVR v2.1.101. RN and HB were updated in CoreSmartBERT v2.8.101 compared to CoreSmartBERT v2.8.100.
PF_XCVR_ERM	3.1.107	Production	Incremental DFE support.

For more information about updating a core version, see 4.2 Updating a Core Version.

4.2 Updating a Core Version

Perform the following procedure to update a core version:

1. Download the latest version of the core into your vault.
2. Upgrade each configured core in your design to the latest version by right-clicking on the core component in the design hierarchy and selecting **Replace Component Version**.
3. Regenerate the core.
4. Derive the Timing Constraints again from the Constraint Manager tool to use the latest generated core timing constraints.
5. Rerun the design flow.

5. Resolved Issues

The following table lists the customer-reported defects and enhancement requests resolved in Libero SoC v2021.1 that have case numbers. Resolution of previously reported “Known Issues and Limitations” are also noted in this table.

Table 5-1. Customer-reported Defects and Enhancement Requests with Case Numbers

Case Number	Description	Resolution
1129393	Synplify Pro should generate the CDC report in .csv format.	Libero's report now shows the CDC report with column filtering and sorting capabilities.
493642-2279076374	Tri-state arcs are missing from the BA SDF.	The missing Tri-state arcs in the BA sdf has been resolved by adding 4 delay triplets to iopath arc (`E -> PAD`). Cells affected are `IOPAD_TRI` and `IOPAD_BI`.
493642-2573858783	`SD_CONNECT`: Canvas should pan automatically when the edge of the canvas is reached.	Fixed the issue where canvas does not automatically pan when the selection or connection tool reaches the edge of the canvas.
493642-2589545643	The Archive Project function creates folders with the wrong creation date.	The archive function has been fixed to show the correct date and time.
493642-2600387353	`HDL_LANGUAGE`: DH: A VHDL recursive error is reported, but the design flow is passed.	The priority of this message has been reduced from an error to a warning.
493642-2606808569	Request to add the command `smartpower_set_thermalmode` to the *Tcl Commands User Guide*	Updated the *Tcl Commands User Guide* to include the `smartpower_set_thermalmode` command documentation.
493642-2651664363	Absolute/relative path: `export_script` does not export the relative path for the create_hdl_core TCL command.	Libero now exports the relative path for the HDL+ component as part of the Project Export procedure.
493642-2686416398	`SERDES_REFCLK IO` std selection using `serdes_vddi` should be more user friendly.	A tool tip has been added for the `SERDES_VDDI` rail in the RTG4 Power Estimator.
493642-2700670264	RTG4: unused bank power missing	The I/O bank static calculation formula has been updated for all rails in the RTG4 power estimator.
493642-2707049852	Retain the Design Initialization flow settings for different runs.	User-selected Memory initialization and Storage selection information in Fabric RAMs of Design and Memory Initialization are retained (i.e., user-selected information in Fabric RAMs are shown if the user returns to the **Design Initialization** tab and then goes to the **Fabric RAMs** tab).

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Case Number	Description	Resolution
493642-2736369334	DDR IO Margin\Training Iterator: Training failure not indicated.	When checking for the CTRLR_READY signal and flagging it as error if it is not HIGH, the training Iterator stage shows as failed and the tooltip reads **Controller Ready Not High**.
493642-2736850582	PF_SOC: MSS: Option to disable SD card pins SD_WP and SD_POW in the PolarFire SoC MSS configurator.	Added the Boolean parameter Disable SD_WP and SD_POW ports below the SD usage combo box. If this parameter is enabled, ports usage is disabled. Default is false.
493642-2740070097	The Tcl script does not have a command to import memory files.	Users can specify imported memory file information when configuring IGLOO2 TPSRAM, DPSRAM, and URAM through Tcl using the parameter IMPORT_FILE. This parameter accepts absolute and relative paths as inputs.
493642-2743422823, 493642-2776783309	MT25QL128 and MT25QU128ABA1EW7-0SIT SPI Flash Programming support in Libero SoC v12.4.	The SPI-Flash Programming section under **Known Issues** in Libero SoC v12.4 has been updated.
493642-2744828403	Providing support for JTAG reading of data integrity bits in PolarFire.	Users can now see the Data Integrity Bits value when running the DEVICE_INFO action in Libero and FlashPro Express.
493642-2747892376	Input to output timing paths in SmartTime v12.4.	Updated path tracing to report paths ending on the output port used as a clock.
493642-2748440670	RTG4: PLL loses lock during simulationF.	The message displayed during simulations is added below the Miscellaneous Options section in the *RTG4 FCCC with Enhanced PLL Calibration Configuration User Guide*.
493642-2771623606	PolarFire SPM: Enhance the SPM GUI to clarify programming and debugging restrictions.	The **Disable Auto Programming and IAP Services** option moved from the **Disable programming interfaces** group. The option behavior has not changed
493642-2781407336	RTG4 CCC simulation with dynamic delays sometimes has a phase shift of 180 degrees.	Fixed the PLL simulation model to sync the PLL output and FB clock with input REF CLK when a new value of RF_DLINE is loaded into the FCCC_PDLY_CR register.
493642-2786902308	Job: fpga_mapper terminates with the error status 253.	This issue has been resolved in the Synplify Pro bundled with this Libero release.

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Case Number	Description	Resolution
493642-2788133376	SPI Data Storage client with **Filled with 1s** option is not programming the external SPI properly.	The **Filled with 1s** option is now supported.
493642-2794138019	Misleading message in the log for RTG4 SEDES design.	Clarified message for the currently selected device package.
493642-2796571518	Support for the FlashPro TCL command `enable_prg_type` support for FlashPro 5.	The command can be used to enable FlashPro 5, FlashPro 6, and embedded FlashPro 6.
493642-2798908881	RTG4_UPROM: Issue updating RTG4 UPROM using the TCL script in Libero SoC v12.5.	The issue related to updating RTG4 UPROM contents using the TCL command `UPDATE_UPROM` has been resolved.
493642-2800897360	NetlistViewer runs out of memory because it fails to recognize a RAM in VHDL.	The NetlistViewer issue has been resolved.
493642-2804329140	I/O Editor crashes when clicking on a Pin group.	The I/O Editor issue has been resolved.
493642-2805303278	SmartFusion2 simulation PLL issues.	Fixed the PLL simulation model to deassert PLL lock when the reference clock stops during the simulation.
493642-2807685157	`BUFD_DELAY` in RTG4 is notated with big red question mark.	This issue has been resolved.
493642-2808626348	Timing path sorting is not working in the detail view.	Updated the condition to show the correct expanded path information for the selected timing path in SmartTime tables.
493642-2809774357	`PF_INIT_MONITOR`: Synthesis fails in Libero SoC v12.6 after updating `PF_INIT_MONITOR`.	Synthesis fails because of an undriven `AND` gate. The `AND` gate instance with undriven input pins has been removed.
493642-2811312932	SDC processing takes too much time for customer designs.	Improved constraint checking runtime.
493642-2811320316, 493642-2819141478	Issue exporting the firmware in Libero SoC v12.6 through TCL script.	Added the Tcl command export_firmware.
493642-2817907985	`PF_QDR`: CoreQDR BFM simulation: X observed when reading upper addresses.	The QDR BFM simulation model has been updated to work properly at upper addresses.
493642-2817917898	Refresh command in Tcl script unchecks SDC files for Timing Verification.	Timing constraints associated with the verify timing tool are now retained after Build Design hierarchy or Refresh option (F5) in No Synth flow.

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Case Number	**Description**	**Resolution**
493642-2818533273, 493642-2820758688	SmartFusion2: Issue updating the eNVM content in Libero SoC v12.6 using the TCL script.	Issues related to updating `IGLOO2MSS_ENVM` contents using the TCL command `UPDATE_ENVM` have been resolved.
493642-2813231063	Repair min-delay violations take a long time in Libero SoC v12.6.	The repair algorithm has been improved to optimize for congestion.
493642-2818836281	Probe insertion changes some project settings.	This issue is fixed in this release. The device configuration settings from Libero are retained after probe insertion.
493642-2820145985	Place and Route error occurs with fixed macro locations in Libero v12.6.	The clustering algorithm was updated to handle fixed cells with TMR separation.
493642-2821156844	`RTG4_UPROM`: Libero deletes `UPROM.cfg`.	The `UPROM.cfg` file is no longer being deleted after re-opening an RTG4 UPROM configurator.
493642-2825769475	SmartTime is missing the User Set.	Updated path tracing to report paths that are part of the clock network.

Table 5-2. Customer-reported Defects and Enhancement Requests (No Case Numbers)

Description	Resolution
PolarFire -1 speed-grade devices limit the maximum DDR3 GPIO rate to 800 Mbps.	The maximum rate for GPIO DDR3 for PolarFire -1 devices is 1067 Mbps
PolarFire SoC Icicle embedded programmer had a longer programming time in Linux than in Windows.	PolarFire SoC Icicle embedded programmer no longer has a longer programming time in Linux than in Windows.
The PF_IOD GUI does not allow non-integer frequencies.	The Validate rules on `DATA_RATE` for both RX and TX IOD GENERIC cores have been changed to accept floating values for `DATA_RATE`.
Instantiating a tamper macro to reset a device by asserting its `RESET` input without configuring or enabling its features causes Libero to generate an error when the `.spi` file from this image is used to configure design initialization. The error message says that the golden image cannot contain security. The tamper macro has no security feature enabled (only reset input/functionality is used) and no silicon signature and customer security is enabled. Although the SPI bitstream should not contain any security components, it does.	Users can now load an SPI file as a Recovery/Golden client in the configure design initialization tool when exported from a Libero design that instantiates the tamper macro without enabling any features.
Runtime issue for RTG4: Compile takes approximately 2 hours to complete.	Fixed algorithm to reduce runtime for this corner case.
SPI Flash init configuration and golden image with tamper macro.	The security component is not added to the bitstream if no tamper macro settings are selected. This allows the bitstream to load as a golden client.
RTG4 Global net report fanout is incorrect.	The value of the **Fanout** column has been corrected to show the real fanout of the net.

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Description	Resolution
Construct does not allow loading of SPI Flash file automatically.	In FlashPro Express, users can now load a SPI Flash file for PolarFire and PolarFire SoC devices after creating a new job project by constructing a JTAG chain automatically.
The PF_XCVR_REF_CLK GLOBAL path to Fabric logic is missing.	Libero now enables the path from the XCVR Ref Clk to the Fabric.
PF_DDR_OCTAL: Add individual tap adjustments for multiple memory chips.	See 3.3.9 New Post-layout Editing of I/O Attributes and Delay Parameters.
I/O registers assigned with PF_IO macro are not reported.	Compile, Pin, and IOFF reports for G5 have been updated to display I/O registers assigned with the PF_IO macro.
The SmartPower VCD + Vectorless: large frequency value is annotated after import.	The SmartPower code now annotates pin toggle rates using the correct clock domain for this corner case.
Clock and logic frequency are limited to 300 MHz.	Power estimator has been revised to allow frequencies up to 425 MHz to be specified in the **Clock** and **Logic** tabs.
Although PCIE K_BRIDGE_SPEED is not locked, if it had a value of 1 for PCIE#_CONFIG_PCIE_#_K_BRIDGE_SPEED_LOCK, it was reported as an error.	This issue has been resolved and is no longer reported as an error.
Internal Error/RTG4:Libero crashes when trying to modify Op Cond on 3.3v.. assertion at OperatingCondition.cpp", line 458.	Changing the temperature range, core voltage range, or default I/O voltage range (for all voltages) from MIL to Custom or Custom to MIL in the Project Settings UI and saving the changes no longer causes Libero to crash.
Data exported using the Record Action function is incorrect.	Record Actions now reports the proper values.
Load probe feature always opens to the default location.	SmartDebug now opens the last opened directory instead of the default location.
Charts do not show whether training fails in DDR Debug mode.	SmartDebug now displays training charts even if training fails.
A training iteration counter has been added to the SmartDebug GUI.	The SmartDebug GUI now displays an iteration counter and reports a warning when the reset counter value exceeds 10.
Incorrect result on write calibration in DDR Debug function.	SmartDebug includes additional checks to identify write-calibration failures.
SD_WRITER: Missing connection for bus slice.	Libero now detects missing slice nets and write assignments on component generation.
PF_IO: Complete matrix of registered versus non-registered BIDIR I/O.	Libero configurator now allows Input IOFF, Output IOFF, or Enable IOFF for bidirectional I/Os to be selected individually.
PF_IOD_OCTAL_DDR configuration issues.	Libero IO configurator now allows single-ended DQS to be selected for AP SRAM memory.
PF_IOD GUI does not allow non-integer frequencies.	The PF IOD configurator now accepts non-integer frequencies.

6. Known Issues and Limitations

The following table lists known issues and limitations associated with Libero SoC v2021.1.

Table 6-1. Known Issues and Limitations Associated with Libero SoC v2021.1

Family	Description
	Libero
All families	`HDL_LANGUAGE: GLOBAL_INCLUDE_PATH`: When a module is present in an include file, the file is shown as a linked file inside the project. When there is a broken Global Include Path for such projects, the include file is also shown with a broken link. If the project is closed and re-created, the correct Global Include Path displays correctly. If the Global Include path under Project Settings is changed, two links are shown for include file inside the project: • One with the new Global Include Path, as shown inside the project. • The other is the broken link with the previous Global Include Path. There are no functionality issues, but an extra broken link appears in the project. Remove this link when the Global Include Path in Project Settings is changed.
PolarFire	Crash in `g5layout_mapper.cxx`, with Block Flow and `Core_JTAG_Debug` In this scenario: • The design uses floating input ports `TCK`, `TDI`, `TMS`, and `TRSTB`, and • The UJTAG macro is connected to top ports: `TCK_0`, `TDI_0`, `TMS_0`, and `TRSTB_0`. When the block was created, it refers to the first top ports (`TCK`, ...). Later, the ports are floating, which confuses the system, causing the programming step to fail. Workaround: Make sure the top ports of the dedicated ports of the UJTAG are the same in the block and the top design. In this case, delete the first set of floating ports (`TCK`, ...), then rename the ports `TCK_0` to `TCK`, `TDI_0` to `TDI`, `TMS_0` to `TMS`, and `TRSTB_0` to `TRSTB`.

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Family	Description

PolarFire	An enhancement to Synthesis Compiler in this SynplfiyPro 2020.09MSp1 release (Libero v2021.1 release) is related to the initial value support for memory initialization and is not technology specific. Testcases with MiV core fail in synthesis with following error message: `@E: CS162 :"./component/work/MIV_RV32IMA_L1_AXI_C0/MIV_RV32IMA_L1_AXI_C0_0/core/miv_rv32ima_l1_axi_data_arrays_0_ext.v":81:24:81:38|Loop iteration limit 2000 exceeded - add '//synthesis loop_limit 4000' before the loop construct`
	Workaround: In the **Libero GUI -> Synthesis -> Configure Option -> Additional Parameters** box, add:
	`set_option -looplimit 4000`
	OR
	Add the following `SYNPLIFY_OPTIONS` options:
	`configure_tool -name {SYNTHESIZE} -params {BLOCK_MODE:false} -params {BLOCK_PLACEMENT_CONFLICTS:ERROR} -params {BLOCK_ROUTING_CONFLICTS:LOCK} -params {CLOCK_ASYNC:800} -params {CLOCK_DATA:5000} -params {CLOCK_GLOBAL:2} -params {PA4_GB_COUNT:24} -params {PA4_GB_MAX_RCLKINT_INSERTION:16} -params {PA4_GB_MIN_GB_FANOUT_TO_USE_RCLKINT:1000} -params {RAM_OPTIMIZED_FOR_POWER:0} -params {RETIMING:false} -params {SEQSHIFT_TO_URAM:0} -params {SYNPLIFY_OPTIONS: set_option -looplimit 4000} -params {SYNPLIFY_TCL_FILE:}`
	Set this option and run synthesis. It should pass.

PolarFire	Opening two or more views in Netlist Viewer (for example, Hierarchical RTL View and Flattened Post-Compile View) may cause a crash due to memory usage. Avoid opening multiple views for large designs. The DRC check in the I/O Editor does not validate all the constraints set in the tool. You must run Place and Route to validate these constraints.
PolarFire	If you enable **Auto Rotate** and **Net** under **Auto Rotate**, and then uncheck the box in the **Net** color selection, the net color in the Net view is not consistent with that of the Planner.
PolarFire SoC	`MPFS250T-1FCVG484 DDR3 SOUTH_SW_OPT` pinouts has been removed because they are identical to `SOUTH_SW_OPT` pinouts for `MPFS460T*-FCG1152_EvalE` and `MPFS250T*-FCVG784_EvalE`. We do not support optimal pinouts on Eval packages.
RTG4	DRC does not run in the Tcl flow when generating `RTG4FCCCECALIB`, but works properly in GUI mode.

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Family	Description
RTG4	Due to a GUI defect, you cannot configure an RTG4 FCCC PLL with external feedback using differential input to FPGA. Workaround: Configure the I/Os that are used in external feedback mode as differential using Tcl mode. To configure the I/O as differential, set the parameter `IO_HARDWIRED_<pad_id>_IS_ DIFF` to true. The other parameters remain the same for selecting a pad in external feedback mode: • `PLL_FB_SRC` → `IO_HARDWIRED_<pad_id>` • `PLL_EXT_FB_GL` → `EXT_FB_GL<GL_ID>`
Synthesis/Simulation	
All families	Microchip identified a date dependent issue with Synplify Pro ME and Identify ME R2020.09MSP1-1 (Windows) software bundled with Libero SoC v2021.1. Starting August 31, 2021, when the Synplify Pro ME and Identify ME tool is launched on Windows in the batch mode, the `This software has expired` error appears, preventing design synthesis and debug. Workaround: Download and install the updated versions of Synplify Pro ME R2020.09MSP1-1 for Windows and Identify ME R2020.09MSP1-1 for Windows stand-alone software for Libero SoC v2021.1 to remove the date dependency. When running Synthesis and Identify within Libero SoC v2021.1, you need to add a new Synthesis and Identify tool profile pointing to the `synplify_pro.exe` and `identify_debugger.exe` within the updated installation.

All families	With multiple synthesis implementation created, if users open SynplfiyPro interactively, run synthesis, and return to Libero, the `*.prj` file writes the synthesis options multiple times for the active synthesis implementation. This occurs every time Synplify Pro is invoked interactively and run.
	`project -result_file "synthesis_1/top.vm"`
	`impl -active "synthesis_1"`
	`set_option -rom_map_logic 1`
	`set_option -automatic_compile_point 1`
	`......`
	`impl -active "synthesis_1"`
	`set_option -rom_map_logic 1`
	`set_option -automatic_compile_point 1`
	`......`
	Workaround: Users can refer to run_options.txt file in synthesis and Libero -> Report View to find out which options are used by Synplify Pro. Then users can run synthesis for that particular active implementation.

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Family	Description
PolarFire	Some testcases passed with earlier Synplify Pro releases fail with the latest version with the following error message: `@E: DE117 :"/soft/sqa101/zeus/ Testing_Libero_2021_1/hdl/apollo_csr.sv":20:46:20:46| Found forward referencing of interface variable apollo.writedata` The compile order is misleading and the error can be bypassed with the following workaround: Put the following option `message_override -warning DE117` through **Libero -> Synthesis -> Configure Options -> Additional Parameters**. With this modification, the message is downgraded to a warning and synthesis passes.
PolarFire	When automatic compile point is enabled, synthesis passes successfully, but Place and route errors our pointing to the derived constraint file: `Error: SDC0025: C:\validate\PF_Mi_V_Tut\constraint\PROC_SUBSYSTEM_derived_constraints.sdc:17: Invalid false path constraint: the -through value [get_nets {AXI4_Interconnect_0/ARESETN* }] is incorrect.` Workaround: Either turn off (uncheck) **Automatic Compile Point** while running synthesis through the **Libero > Synthesis > Configure Options** dialog box. Keep the remaining options and all constraints as they are. OR Keep everything the same, but update the line below in the file `*derived_constraints.sdc` to use `get_pins` instead of `get_nets`. `set_false_path -through [ get_pins { AXI4_Interconnect_0/ARESETN* } ]`
PolarFire	The PLL may generate inaccurate frequency for certain frequency combinations of fractional modes, which can cause PLL outputs to drift over a period.
Timing/Power	
All families	Libero 12.5, 12.6, and 2021.1 releases have different clock constraint values in data required time calculations when the invert switch is enabled and disabled. The analysis shows different behavior comparing to 12.3 release.
PolarFire	The max clock frequency on the regional clocks (`RX_CLK_R/TX_CLK_R` on the serdes and `RX_CLK` on `lanectrl`) in `MPF300XT` do not match the datasheet.
PolarFire	The violation report shows violations (red cross), but the timing report does not (green check). This indicates there is indeed a timing violation and the red cross is correct.

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Family	Description
PolarFire	Since Libero v12.4, SmartTime stops propagating clocks when a generated clock is reached. For example, in a design whose clocks are `clk1` --> `gen1` --> `gen2`, specifying gen2 using gen1 as master caused no issues. If `gen2` is specified using `clk1` as master, however, the generation fails because `clk1` is stopped by `gen1` and never reaches `gen2`. Workaround: Specify the second generated clock using the first generated clock as master.
PolarFire	In CentOS8, the Export Report for MPE feature causes a crash in SmartPower. However, the report is exported successfully and can be used in MPE.
PolarFire	In the SmartTime tool, the search option using **Apply filter** does not work.
SmartFusion2	On Linux, the timing tool crashes when trying to verify that paths exist between the specified `-from` and `-to` values when using `[ all_registers -clock some_clock ]`. Workaround: Use `[ get_clocks some_clock ]` instead of `all_register -clock some_clock`.
SmartDebug	
PolarFire, PolarFire SoC	When a dual-mode PCIe design is considered in SmartDebug, the following issues are observed in the PCIe debug feature: • For dual-PCIe designs with `PCI0` and `PCIe1` controllers, only `PCIe1` appears in the UI. `PCIe0` is not shown. • When **PCIe0 Lane** is selected, the `LTSSM` state is shown for `PCIe1`, but the `LTSSM` state for `PCIe0` is not shown. • Data Rate, Link Width, and other settings are shown for `PCIe1` only, but not for `PCIe0`.
Programming	
PolarFire	Libero v2021.1 supports the following Micron SPI Flash memory devices: • Using FlashPro5: MT25QL01G only • Using FlashPro6: all members of N25Q and MT25Q device families For information about support for Flash memory devices from other vendors and device families using FlashPro6, contact Microchip Technical Support.
PolarFire, PolarFire SoC	Running Export SPI Flash Image in Libero 2021.1 exports a `*.bin` file that can be programmed only by using FlashPro Express and will not work with any third-party solutions. **Workaround:**Download the Python script and run it to generate a new version of the `*.bin` file that can be used with third-party solutions. The script accepts two parameters: • SPI Flash `*.bin` filepath exported from Libero 2021.1 • New output `*.bin` filepath

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Family	Description
PolarFire, PolarFire SoC	If the SPI-Memory device has already been programmed, programming operation with updated data fails if the target memory region to be programmed includes the last 64KByte sector which is memory region (0x7F0000 - 0x7FFFFF).
PolarFire, PolarFire SoC	Although sNVM and eNVM are sanitized when enabled, since the action is part of the bitstream, FlashPro 6 does not report a `Sanitizing sNVM...` or `Sanitizing eNVM...` message during erase operations in a PPD flow.
PolarFire and PolarFire SoC	Running the programming SPI Flash actions tool fails if Generate Bitstream has not been run and displays the following error message: `Please re-run 'Generate Bitstream' tool and then execute 'Run Programming Device Action' tool.` This affects PolarFire in Libero versions 12.1 through 12.5 and PolarFire SoC in Libero versions 12.5 and 12.6. Workaround: Run the Generate Bitstream tool and run the programming SPI Flash actions tool again.
PolarFire SoC	eFP6: some testcase fails with the following error message: `Error: Failed to send data to eFP6. Err = -4|Error: eFP6 connection failed.` Workaround: Power cycle the iCicle board and rescan the programmers.
PolarFire SoC	For PolarFire SoC Libero designs that contain eNVM, running `VERIFY_DIGEST` after programming device fails and displays the message `eNVM digest verification: FAIL`. Workaround: Deselect the procedure **DO_ENABLE_ENVM** in the `VERIFY_DIGEST` action.
PolarFire SoC	For PolarFire SoC Libero designs that generate or export eNVM-only bitstreams, the generated bitstream file/job includes an ERASE action that is not applicable and does nothing. This issue affects Libero versions 12.4 and later. For Libero version 12.6, this issue applies for eNVM only case + no eNVM sanitization option.
PolarFire SoC	For PolarFire SoC Libero version 12.4 and later designs that generate or export eNVM-only bitstreams, the generated bitstream file/job will include an ERASE action that is not applicable and does nothing. **Note:** For Libero version 12.6, this issue applies to the eNVM-only case + no eNVM sanitization option.
PolarFire SoC	For Libero designs with sNVM clients configured, with no custom user security options selected, and whose design is programmed on the device, modifying sNVM client content and sNVM client Fabric/MSS read/write permissions, running a `VERIFY` action fails and displays the message `Failed to verify Security` instead of `Failed to verify SNVM`. This issue affects Libero versions 12.4 and later.

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Family	Description

SmartFusion, RTG4, PolarFire, PolarFire SoC	Some users see the following error message during programming:
	`Error: programmer 'S201QVCGH' : device 'RT4G150' : FP5 Scan: JTAG_ExecuteCommandSequence`
	`FP5: Error code = 4 - General device IO error.`
	`......`
	`Error: programmer 'S201QVCGH' : device 'RT4G150' : Executing action VERIFY FAILED.`
	`Error: programmer 'S201QVCGH' : FP5 SyncWithProgrammerAtPort: OpenSpecifiedHiSpeedDeviceBySerialNumber - PortB FP5: Error code = 2 - Device not found.`
	`......`
	This is most likely a USB connection issue. If for some reason the connection is interrupted, this error occurs.
	The error message may be different, depending on where the packet is dropped during verify. However, the error code will always be set to 4, which is “General device IO error.”

SmartFusion2, IGLOO2	In FlashPro 5, the Device Info log shows the wrong checksum and design name during SPI Slave programming.
SmartFusion2, IGLOO2	If `UEK2` is not selected in the SPM main window, the Key Mode Policy window still allows users to disable `UEK2`. This is not the correct behavior. `UEK2` in Key Mode Policy should be grayed out if `UEK2` is not entered.
Installation and System Limitations	
FlashPro6	Users with FlashPro6 drivers previously installed on their system may see the following message at the end of the installation: `The installation of Program Debug Tool v12.5 is finished, but some errors occurred during the install. Please see the installation log for details.` Resolution: Uninstall existing FlashPro6 drivers and restart the system before installing Libero SoC version 12.5. If the software is already installed, ignore the above message if installation logs do not report errors.
All families	The following link provides information about FlexNet error codes: https://knowledge.autodesk.com/search-result/caas/sfdcarticles/sfdcarticles/Common-FlexNet-error-codes.html
All families	If the installer does not boot in graphical mode, additional X window system libraries might be required. For RHEL/CentOS, the following system package is recommended: `$ sudo yum install -y libXau libX11 libXi libxcb libXext libXtst libXrender`

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Family	Description
All families	Many antivirus and Host-based Intrusion Prevention System (HIPS) tools flag executables and prevent them from running. To avoid this block, modify your security setting by adding exceptions for specific executables in the antivirus tool. For assistance, contact the tool provider. Many users run Libero SoC PolarFire successfully with no modification to their antivirus software. Microchip is aware of issues for some antivirus tool settings that occur when using Symantec, McAfee, Avira, Sophos, and Avast tools. The combination of operating system, antivirus tool version, and security settings all contribute to the end result. Depending on the environment, Libero SoC, ModelSim ME, and/or Synplify Pro ME operation may or may not be affected. To ensure that all public releases of Libero software are not infected, each software package is tested with several antivirus applications before being released. To ensure further security, the Microchip software development and testing environment is protected by antivirus tools and other security measures.
All families	The following warnings in the log might appear when the Libero floating license starts: • `(snpslmd) Warning: Incompatible vendor daemon found. The vendor daemon <actlmgrd> is not supported in <SCL_2017.12> version. Warning: Please upgrade to the latest SCL version. Go to http://www.synopsys.com/licensing for more information.` • `(snpslmd) Warning: Incompatible vendor daemon found. The vendor daemon <mgcld> is not supported in <SCL_2017.12> version. Warning: Please upgrade to the latest SCL version. Go to http://www.synopsys.com/licensing for more information.` These warning messages can be ignored safely. The Libero floating license will start properly.

7. System Requirements

The Libero SoC v2021.1 release has the following system requirements.

7.1 Supported 64-bit Operating Systems

- Windows 7 or Windows 10 OS
- RedHat Enterprise Linux 6.6-6.11, Red Hat Enterprise Linux 7.2-7.6, and Red Hat Enterprise Linux 8.2
- CentOS 6.6 - 6.11, CentOS 7.2 - 7.6, and CentOS 8.2
- OpenSUSE Leap 42.3 (SLES 12.3 equivalent)
- Ubuntu 18.04 (Synopsys and Mentor do not directly support the Ubuntu platform. FlashPro5 programmer is not supported with Ubuntu.)

Note: Setup instructions for using Libero SoC v2021.1 on Red Hat Enterprise Linux OS, CentOS, or Ubuntu are available in the *Libero SoC Linux Environment Setup User Guide*. As noted in that document, installation now includes running a shell script (`bin/check_linux_req.sh`) to confirm the presence of all required runtime packages.

Support for the following operating systems will stop after the Libero SoC v2021.1 release. For more information, see PDN20028 and PDN21004.

- Red Hat Enterprise Linux 6.6-6.11
- CentOS 6.6-6.11
- Windows 7

7.2 Random-Access Memory (RAM) Requirements

Minimum of 16 GB RAM.

8. Download Libero SoC Software

The following are available for download:

- Libero SoC v2021.1 (Linux)
- Libero SoC v2021.1 (Windows)
- Libero licenses
- MegaVault (Linux)
- MegaVault (Windows)
- Program & Debug (Linux)
- Program & Debug (Windows)
- Stand-alone MSS configurator installer (Linux)
- Stand-alone MSS configurator installer (Windows)
- snpslmd (Linux)
- snpslmd (Windows)

Note: Windows installations require administrative privileges.

After a successful installation, clicking **Help-> About Libero** shows Release: 2021.1.

9. Documents Updated in this Release

The following documents have been updated for the v2021.1 release:

- *Libero SoC Linux Environment Setup User Guide*
- *Libero SoC v2021.1 Design Flow User Guide for PolarFire*
- *Libero SoC v2021.1 Design Flow User Guide for RTG4, SmartFusion2, and IGLOO2*
- *Libero SoC v2021.1 Tcl Commands Reference Guide for SmartFusion2, IGLOO2, and RTG4*
- *Libero SoC v2021.1 Tcl Commands Reference Guide for PolarFire*
- *SmartTime v2021.1 User Guide for PolarFire*
- *SmartPower v2021.1 User Guide* for all families
- *SmartDebug v2021.1 User Guide for PolarFire*
- *Synplify Pro ME R-2020.09M-SP1-1 FPGA User Guide*

10. Appendix A: New Device Support Matrices

The following sections provide matrices for new RT PolarFire devices.

10.1 PolarFire SoC New Device Support Matrices

The following table lists the licensing and device/package combinations for PolarFire SoC devices.

Table 10-1. PolarFire SoC Licensing, Timing/Power, and Programming Combinations Based on Speed Grade and Temperature

(T/TL/TS/TLS), Speed Grade, Temperature	Part Number	Libero Licensing				Libero Timing/Power	Programming
		Eval	Silver	Gold	Platinum		
T, STD, EXT	MPFS025T-FCSG325E	Yes	Yes	Yes	Yes	Advance	No
	MPFS095T-FCSG325E	Yes	Yes	Yes	Yes	Advance	No
TL, STD, EXT	MPFS025TL-FCSG325E	Yes	Yes	Yes	Yes	Advance	No
	MPFS095TL-FCSG325E	Yes	Yes	Yes	Yes	Advance	No
T, -1, EXT	MPFS025T-1FCSG325E	Yes	Yes	Yes	Yes	Advance	No
	MPFS095T-1FCSG325E	Yes	Yes	Yes	Yes	Advance	No
T, STD, IND	MPFS025T-FCSG325I	Yes	Yes	Yes	Yes	Advance	No
TL, STD, IND	MPFS025TL-FCSG325I *	Yes	Yes	Yes	Yes	Advance	No
	MPFS095TL-FCSG325I *	Yes	Yes	Yes	Yes	Advance	No
T, -1, IND	MPFS025T-1FCSG325I *	Yes	Yes	Yes	Yes	Advance	No
TLS, STD, IND	MPFS025TLS-FCSG325I	Yes	—	—	Yes	Advance	No
	MPFS095TLS-FCSG325I *	Yes	—	—	Yes	Advance	No
TS, STD, IND	MPFS025TS-FCSG325I *	Yes	—	—	Yes	Advance	No
	MPFS095TS-FCSG325I	Yes	—	—	Yes	Advance	No
TS, -1, IND	MPFS025TS-1FCSG325I *	Yes	—	—	Yes	Advance	No
	MPFS095TS-1FCSG325I *	Yes	—	—	Yes	Advance	No

10.2 RT PolarFire Licensing and Device/Package Combination Matrix

Libero SoC v2021.1 introduces Preliminary timing and power support for RT PolarFire devices.

Table 10-2. RT PolarFire Licensing and Device/Package Combinations

(T/TL/TS/TLS), Speed Grade, Temperature	Part Number	Libero Licensing				Libero Timing/Power	Programming
		Eval	Silver	Gold	Platinum		
T, STD, MIL, 1.0/1.05V	RTPF500T-CG1509M	Yes	—	—	Yes	Preliminary	Yes
T, -1, MIL, 1.0/1.05V	RTPF500T-1CG1509M	Yes	—	—	Yes	Preliminary	Yes
TS, STD, MIL, 1.0/1.05V	RTPF500TS-CG1509M	Yes	—	—	Yes	Preliminary	Yes
TS, -1, MIL, 1.0/1.05V	RTPF500TS-1CG1509M	Yes	—	—	Yes	Preliminary	Yes
TL, STD, MIL, 1.0/1.05V	RTPF500TL-CG1509M	Yes	—	—	Yes	Preliminary	Yes
TLS, STD, MIL, 1.0/1.05V	RTPF500TLS-CG1509M	Yes	—	—	Yes	Preliminary	Yes

The performance of DDR4 interface cannot exceed 1333 Mbps.

The performance Transceiver protocols cannot exceed 10.3125 Gbps.

11. Revision History

Revision	Date	Description
F	9/2021	In 6. Known Issues and Limitations, added issue that running the Synplify Pro ME and Identify ME tool on Windows in the batch mode, generates the `This software has expired` error.
E	7/2021	In 6. Known Issues and Limitations, added issue that running Export SPI Flash Image in Libero 2021.1 exports a `*.bin` file that can be programmed using only FlashPro Express and will not work with any third-party solutions.
D	06/2021	In 6. Known Issues and Limitations, removed references to internal information.
C	05/2021	In 2.1 New RTL Level Clock Domain Crossing Analysis and Place and Route: • Mentioned that the report can be viewed under **Design > Reports**. • Corrected the name of the generated report that can be viewed in the respective Synthesis node of the report view.
B	05/2021	Removed known issue about disabling program bitstream action (JTAG/SPI Slave) because this is no longer an issue.
A	04/2021	Initial Revision

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