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# PolarFire SoC MSS Configurator (Preproduction) v2021.2

## Release Notes

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### Introduction

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To provide a seamless experience for both embedded software developers targeting the MSS and the hardware engineers developing a hardware/software solution using the MSS and the FPGA array fabric, the MSS configurator application provides a common tool to configure the PolarFire SoC MSS platform that can be used by both the software engineer and/or the FPGA hardware engineer.

The MSS configurator application can be installed as a stand-alone application or as part of the Libero SoC design tool suite, and provides the following features.

- Configuration of the MSS clocks
- Configuration of the MSS interfaces to the FPGA fabric
- Selection and assignment of the MSS peripherals to the MSS dedicated I/Os and/or the FPGA fabric dedicated peripheral interfaces
- Configuration of the MSS Bank voltages and I/O standards and attributes
- Configuration of the MSS DDR memories (DDR3/L, DDR4, LPDDR3, and LPDDR4)
- Enable the User Crypto processor for “S” devices
- Partition L2 memory into Cache, Loosely Integrated Memory (LIM), or Scratchpad
- Presets for the PolarFire SoC Icicle Kit – Bare Metal and Quad Core Linux
- Configuration of the MSS debug features
- Configuration of the Memory Partition and Protection

For details about:

- The high-level MSS architecture and its features, see the [PolarFire™ SoC product overview](#)
- This tool, see the [PolarFire SoC Standalone MSS Configuration User Guide](#).
- PolarFire SoC MSS simulation, see the [PolarFire SoC MSS Simulation User Guide](#).

Use the following links to download the MSS Configurator v2021.2 software:

- [Stand-alone MSS configurator installer \(Linux\)](#)
- [Stand-alone MSS configurator installer \(Windows\)](#)

**Note:** Windows installations require administrative privileges.

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### 1. Software Features and Enhancements

- Option to configure both the I/Os shared by SD and eMMC peripherals if dynamic reconfiguration is needed by the application.
- Option to have eMMC and CAN clock sourced from the fabric (in addition to MSS PLL output source). This is applicable for non-ES devices.
- Package pin information for RefClk, DDR, and SGMII I/Os added to the MSS Configurator report.
- MSS RefClk I/Os, Bank2 and Bank4 I/Os and SGMII I/Os have been merged into a new tab called MSS I/O Attributes.

## 2. System Requirements

### 2.1 Supported 64-bit Operating Systems

- Windows 10
- RedHat Enterprise Linux 6.6-6.11, Red Hat Enterprise Linux 7.2-7.6, and Red Hat Enterprise Linux 8.2
- CentOS 7.2 - 7.6, and CentOS 8.2
- OpenSUSE Leap 42.3 (SLES 12.3 equivalent)
- Ubuntu 18.04 (Synopsys and Mentor do not directly support the Ubuntu platform. FlashPro5 programmer is not supported with Ubuntu. The Job Manager tool is not supported.)

### 2.2 Random-Access Memory (RAM) Requirements

Minimum of 4 GB RAM

## 3. Known Issues

### 3.1 Known Issues and Limitations

The following table lists known issues and limitations associated with MSS Configurator v2021.2.

**Table 3-1. Known Issues and Limitations Associated with MSS Configurator v2021.2**

Family	Description
PolarFire SoC	<p>A bare metal example project using a <a href="#">platform</a> repository release tag earlier than 2020.12 must be updated to release 2020.12 or later when using an xml configuration file generated using MSS Configurator v2.0 or later.</p> <p>Otherwise, the SoftConsole compilation fails with the following error:</p> <pre>The following definitions are missing LIBERO_SETTING_WAY_MASK_M0 LIBERO_SETTING_WAY_MASK_M1 LIBERO_SETTING_WAY_MASK_M2 LIBERO_SETTING_WAY_MASK_M3 LIBERO_SETTING_WAY_MASK_M4</pre> <p>Workaround: Update the platform in your SoftConsole project with release 2020.12 or later of the platform repository. You can download it from: <a href="https://github.com/polarfire-soc/platform">https://github.com/polarfire-soc/platform</a>.</p> <p>Alternatively, you can manually update your MPFS HAL to add the following definitions to the <code>/platform_config/mpfs_hal_config/mss_sw_config.h</code> file in your project:</p> <pre>#define LIBERO_SETTING_WAY_MASK_M0 0x00000000UL #define LIBERO_SETTING_WAY_MASK_M1 0x00000000UL #define LIBERO_SETTING_WAY_MASK_M2 0x00000000UL #define LIBERO_SETTING_WAY_MASK_M3 0x00000000UL #define LIBERO_SETTING_WAY_MASK_M4 0x00000000UL</pre>
PolarFire SoC	<p>While using a platform repository older than 2021.02 release, the L2Cache configuration is set to fixed default values.</p> <p>Workaround: Use the <a href="#">platform</a> repository release 2021.02 or later in the embedded software project to use this new feature added in MSS Configurator v2.0 and later.</p>
PolarFire SoC	<p>While using a platform repository older than 2021.05 release, the Memory Partition and Protection configuration is not supported.</p> <p>Workaround: Use the <a href="#">platform</a> repository release 2021.05 or later in the embedded software project to use this new feature added in MSS Configurator v2021.1 and later.</p>
PolarFire SoC	<p>While using a platform repository older than 2021.05 release, the switching between eMMC and SD I/O configurations is not supported.</p> <p>Workaround: Use the <a href="#">platform</a> repository release after 2021.05 in the embedded software project to use this new feature added in MSS Configurator v2021.2 and later.</p>

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## 4. References

See the following reference documents for further details:

- Configuration of the MSS clocks.
  - For detailed information about the MSS clocking features, see [UG0913: PolarFire SoC FPGA Clocking Resources User Guide](#).
- Configuration of the MSS interfaces to the FPGA fabric.
  - For detailed information about the MSS Fabric Interface Controller (FIC) features, see [PolarFire SoC FPGA MSS Technical Reference Manual](#).
- Selection and assignment of the MSS peripherals to the MSS dedicated I/Os and/or the FPGA fabric dedicated peripheral interfaces.
  - For detailed information about the MSS Peripherals features, see [UG0886: PolarFire SoC FPGA Peripherals User Guide](#).
- Configuration of the MSS Bank voltages and I/O standards and attributes.
  - For detailed information about the MSS Banks and I/Os features, see [UG0916: PolarFire SoC FPGA I/O User Guide](#).
- Configuration of the MSS DDR memories (DDR3/L, DDR4, LPDDR3, and LPDDR4).
  - For detailed information about the MSS DDR4, DDR3, LPDDR3, and LPDDR4 features, see [UG0906: PolarFire SoC FPGA DDR Memory Controller User Guide](#).
- Configuration of the MSS debug features.
  - For detailed information about the MSS debug features, see [UG0888: PolarFire SoC FPGA Trace and Debug User Guide](#).

**5. Revision History**

<b>Revision</b>	<b>Date</b>	<b>Description</b>
D	08/2021	Contains updated content to reflect v2021.2.
C	04/2021	Contains updated content to reflect v2021.1.
B	12/2020	Contains updated content to reflect v2.0.
A	11/2020	Initial Revision

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