Release Notes

Libero SoC v2025.1

Introduction (Ask a Question)

The Libero® SoC Design Suite offers high productivity with its comprehensive, easy-to-learn, easy-to-adopt development tools for designing with Microchip FPGA and SoC device families. It provides you with an integrated hardware tool suite incorporating RTL entry through bitstream programming, a rich IP library, and complete reference designs and development kits. Libero SoC Design Suite includes SmartHLS™ compiler software for abstracted high-level synthesis development flow, which shortens design time, simplifies verification, and accelerates time to market for designs using our FPGAs.

Use Libero SoC v2025.1 for designing with the following Microchip devices:

- RT PolarFire, RT PolarFire SoC and RTG4™ Rad-Tolerant FPGAs
- PolarFire® SoC and SmartFusion® 2 SoC FPGAs
- PolarFire and IGLOO® 2 FPGAs

To design with older Microchip FPGA family devices, use Libero SoC v11.9 or Libero IDE v9.2 and its subsequent service packs.

To access datasheets, silicon user guides, tutorials, and application notes, visit the Microchip website, navigate to the relevant product family page, and then click the **Documentation** tab. Development kits and boards are listed in the **Kits and Hardware** tab.

Important: Libero SoC v2025.1 does not support Classic Constraint flow. IGLOO2, SmartFusion2, and RTG4 projects using the "Classic" flow cannot be opened in this release. A migration path is available for transitioning from the Classic Constraint Flow to the Enhanced Constraint Flow. For more information, see Migrating an Existing Project Created with Classic Constraint Flow to Enhanced Constraint Flow.

Attention: For your reference, Microchip provides a comprehensive library of Libero SoC Design Suite release notes, available here.

Download Libero 2025.1 Software (Ask a Question)

You can download the Libero SoC v2025.1 Design Suite and related software from the Libero® SoC Design Suite 12.x and Later Versions page.

Important: Administrative privileges are required for installing the Libero SoC v2025.1 Design Suite software on the Windows operating system.

Verifying Software Downloads Using MD5 and SHA256 Checksum (Ask a Question)

To verify software downloads using MD5 and SHA256 checksum, use the appropriate procedure for your operating system:

- For Windows® operating systems, type the following at the command prompt: `certutil -hashfile [FILENAME] [HASH]`
- For Linux® operating systems, enter the following command on terminal: `md5sum <path_to_installer>` or `sha256sum <path_to_installer>`

Floating License Daemon Support (Ask a Question)

Microchip now supports 64-bit floating licensing daemons with FlexLM v11.19 for Libero SoC Design Suite (actlmgrd) that include Synopsys Synplify Pro/Identity Pro® ME (snpslmd) and Siemens ModelSim/QuestaSim® ME (saltd,which replaces the previous mgcld).

Before opening Libero SoC v2025.1, perform the following procedure to upgrade your systems:

1. Upgrade existing daemons from v11.16 to v11.19. The v11.19 daemons available for downloading appear under the **Daemons Downloads** link on the following Microchip web page: www.microchip.com/libero.
2. Install the upgraded license available on your microchipDIRECT account (Microchip updated all existing active floating licenses to support the new saltd daemons): www.microchipdirect.com/fpga-software-products.

This bundle is backward-compatible with all previous Libero SoC releases.

Starting with Libero SoC v2024.2, the latest 64-bit license daemons with FlexLM v11.19 are required for all floating license users. For all current floating license users who recently received a new license file due to renewal or upgrade, please download and set up the latest daemons as well.

System Requirements (Ask a Question)

This section provides information on supported operating systems, system memory requirements, and other recommendations.

Supported Operating Systems (Ask a Question)

Libero SoC Design Suite supports the following 64-bit operating systems:

- Microsoft® Windows 10.0 and Windows 11.0
- Red Hat® Enterprise Linux (RHEL) 8.0-8.10, AlmaLinux® 8.3-8.10
- Ubuntu® 20.04.6 LTS

Attention:

- Libero SoC v2025.1 is the last release to support Windows 10.
- Siemens ModelSim Pro does not directly support the Ubuntu platform. However, users can successfully install and run ModelSim Pro and QuestaSim Pro ME on Ubuntu by installing the necessary libraries. Libero provides the script *check_linux_req.sh* to install required system packages for Ubuntu.
- Libero SoC design suite has been tested on x86 and x64 processor-based machines only.

System Memory Recommendations (Ask a Question)

A minimum of 32 GB of Random-Access Memory (RAM) is recommended for implementing designs on MPF500T, MPFS460T, and RT PolarFire FPGA and SoC devices. For all other devices, a minimum of 16 GB of RAM is recommended.

Table of Contents

1. New in This Version (Ask a Question)

This section contains information about new features, new devices, and enhancements introduced in the Libero Design Suite v2025.1.

1.1. Changes That Address Important Issues (Ask a Question)

1.1.1. RTG4 (Ask a Question)

1.1.1.1. PLL Calibration Updates for RTG4FCCCECALIB v2.2.100, FDDR v2.0.200, and SerDes v2.0.200 Cores (Ask a Question)

- Updated the rules for selecting the high-VCO frequency used to implement the enhanced PLL calibration introduced along with CN19009 and its addendums.
  - Prior to v2.2.100, the allowed ratio of high-VCO frequency to actual-VCO frequency used during PLL calibration was between 1.5x to 1.9x of the user configured actual-VCO frequency.
  - Starting with v2.2.100, the allowed High-VCO frequency selected by the RTG4FCCCECALIB core is limited to the reduced range of 1.25x to 1.5x of the actual-VCO frequency. The change was applied to mitigate a rarely encountered loss of lock at cold operating temperatures for specific core configurations using VCO speed-up ratios on the higher side of the previously allowed range.
- Reduced the enhanced PLL calibration high-VCO dwell time from 150 us to 100 us in the RTG4 SerDes PCIe/XAUI SPLL calibration sequence used with a CoreABC initialization subsystem, to ensure continued successful PCIe endpoint enumeration on newer generation host CPUs. The same update was applied to the RTG4FCCCECLAIB and FDDR cores to ensure consistency for all cores using PLL calibration.
- Recommended actions related to the PLL Calibration updates:
  - No action is required for:
    - Designs that have successfully completed full functional and system testing on each production unit over the full operating conditions.
    - Designs not using the PLL in RTG4FCCECALIB, the FDDR FPLL, or the SerDes SPLL (PCIe/XAUI).
  - For ongoing designs using fabric PLLs in systems where the operating temperature can fall below 0°C, perform the following steps and re-run the design flow:
    - Upgrade the design to Libero SoC v2025.1, and observe a warning message in the log window.
    - Update instances of RTG4FCCCECALIB to v2.2.100 and regenerate the core.
    - Update instances of RTG4FDDRC or RTG4FDDRC_INIT to v2.0.200 and regenerate the core.
      - For RTG4FDDRC, manually copy the updated FDDR_init.txt initialization program into the user CoreABC initialization subsystem.
    - Update instances of RTG4 SerDes cores using the SPLL (for PCIe or XAUI interfaces) to v2.0.200.
      - Includes RTG4 cores: PCIE_SERDES_IF, PCIE_SERDES_IF_INIT, NPSS_SERDES_IF, NPSS_SERDES_IF_INIT
      - For SERDES cores without auto initialization, including PCIe, copy updated SERDES_*_init_abc.txt program into CoreABC.

    Note: The Libero SoC v2025.1 design flow will error out during netlist Compile if older core versions are detected.

- For new designs, use Libero SoC v2025.1 and the latest RTG4FCCCECALIB v2.2.100, FDDR v2.0.200, and SerDes v2.0.200 cores.

1.1.1.2. FDDR 16-bit and 8-bit Width Modes with ECC Enabled (Ask a Question)

- Updated IP core top-level DQ_ECC port bit mapping to device package pin FDDR_DQ_ECC[#] for proper ECC functionality.
- RTG4 DDR DQ works as expected when SECDED is enabled.
- When opening a pre-2025.1 RTG4 design that uses the RTG4 FDDR in x16 or x8 modes, the design is invalidated to a pre-synthesis state.
- Applicable for designs that contain instances of the RTG4FDDRC or RT4FDDRC_INIT core configured for 16-bit or 8-bit DQ width with ECC enabled.
- The core component must be updated to an RTG4 version 2.0.200 or later and regenerated to continue with the design flow.
- Review the latest RTG4 Package Pin Assignment Table (PPAT) available on the Microchip website to ensure the board layout has connected the correct FDDR_<E|W>_DQ_ECC<#> package pin to the DDR memory device holding ECC data, depending on the DQ bit-width in use.

1.1.2. PolarFire, PolarFire SoC, RT PolarFire, and RT PolarFire SoC (Ask a Question)

1.1.2.1. DDR3, DDR4, LPDDR3 Fabric Core Updates (Ask a Question)

- Support for ZQCS command
- Re-initialization enabled to restart DDR training
- Fast simulation training IP
- Removal of ODT activation setting on read
- Support for CK/CA additive offset “0” value in the configurator for the DDR3/DDR4/LPDDR3 controller. Additionally, the Read ODT option has been removed from the configurator

1.1.2.2. PF_XCVR CDR 3G, HD SDI (Ask a Question)

- Updated transceiver register presets for “Lock to Data with 2X Gain” receiver mode to account for a wider variety of board noise environments.
- The XCVR CDR PLL mode in the transceiver lane now locks successfully when the Lock Mode is set to Lock to Data with 2x Gain, even under pathological data patterns.

1.1.2.3. IOD LANECTRL Isolation from Unrelated Active DLL (Ask a Question)

Enhanced DRC to ensure that IOD LANECTRL instances are isolated from unrelated active DLL instances when a design has multiple IOD interfaces such as MIPI, Generic TX, and Generic RX interfaces.

1.1.2.4. IOD RX_CLK_ODT_EN for LVDS Failsafe (Ask a Question)

- Connected RX_CLK_P to HS_IO_CLK when “Clock to Data Relationship” is dynamic, centered, or aligned.
- New ODT_EN LVDS Failsafe functionality for 'IOD_RX' core allows users to avoid time-zero failures when the clock-to-data relationship is not fractional.

1.1.2.5. CoreFIR_PF: Constant Coefficient of Inferred MACC_PA_BC_ROM (Ask a Question)

Synplify Pro versions V-2023.09M (Libero SoC v2024.1) and V-2023.09M-3 (Libero SoC v2024.2) could write a hexadecimal prefix for a binary format constant coefficient of an inferred MACC_PA_BC_ROM instance in the generated VM netlist. This primarily affected user-defined coefficients of CoreFIR_PF components. Synplify Pro version V-2023.09M-5 in Libero SoC v2025.1 now generates proper format of the inferred constant coefficients.

1.1.3. PolarFire SoC Standalone MSS Configurator (Ask a Question)

1.1.3.1. MSS_DDR 16-bit Width with ECC Enabled (Ask a Question)

Updated MSS Configurator component XML to enable correct ECC byte-lane and ensure successful DDR memory training.
Note: MPFS HAL versions later than v2.3.105 is required from the PolarFire SoC GitHub to use this change.

1.1.4. RT PolarFire SoC (Ask a Question)

1.1.4.1. CG1509 Package Update (Ask a Question)

Updated package pin functions for RTPFS460ZT/ZTS/ZTL/ZTLS CG1509.

1.2. New Device Support (Ask a Question)

1.2.1. PolarFire (Ask a Question)

1.2.1.1. New PolarFire FPGA Core Devices (Ask a Question)

Libero SoC v2025.1 introduces the following PolarFire core devices with programming support.

Device	Temp-range	Speed-grade	Voltage	Timing/Power
MPF050TC	EXT, IND, TGrade2	STD	1.0V, 1.05V	Production
MPF100TC	EXT, IND, TGrade2	STD	1.0V, 1.05V	Production
MPF200TC	EXT, IND, TGrade2	STD	1.0V, 1.05V	Production
MPF300TC	EXT, IND, TGrade2	STD	1.0V, 1.05V	Production
MPF500TC	EXT, IND, TGrade2	STD	1.0V, 1.05V	Production

1.2.1.2. New PolarFire FPGA TS Automotive TGrade2 Devices (Ask a Question)

Libero SoC v2025.1 introduces the following PolarFire TS Automotive TGrade2 devices.

Device	Temp-range	Speed-grade	Voltage	Timing/Power
MPF100TS	TGrade2	STD, -1	1.0V, 1.05V	Production
MPF200TS	TGrade2	STD, -1	1.0V, 1.05V	Production
MPF300TS	TGrade2	STD, -1	1.0V, 1.05V	Production
MPF500TS	TGrade2	STD, -1	1.0V, 1.05V	Production

1.2.2. PolarFire SoC (Ask a Question)

1.2.2.1. New PolarFire SoC Core Devices (Ask a Question)

Libero SoC v2025.1 introduces the following PolarFire SoC core devices with programming support.

Device	Temp-range	Speed-grade	Voltage	Timing/Power
MPFS025TC	EXT, IND, TGrade2	STD	1.0V, 1.05V	Production
MPFS095TC	EXT, IND, TGrade2	STD	1.0V, 1.05V	Production
MPFS160TC	EXT, IND, TGrade2	STD	1.0V, 1.05V	Production
MPFS250TC	EXT, IND, TGrade2	STD	1.0V, 1.05V	Production
MPFS460TC	EXT, IND	STD	1.0V, 1.05V	Production

1.2.2.2. New PolarFire SoC TS Automotive TGrade2 Devices (Ask a Question)

Libero SoC v2025.1 introduces the following PolarFire SoC TS Automotive TGrade2 devices.

Device	Temp-range	Speed-grade	Voltage	Timing/Power
MPFS025TS	TGrade2	STD	1.0V, 1.05V	Production
MPFS095TS	TGrade2	STD, -1	1.0V, 1.05V	Production

New PolarFire SoC TS Automotive TGrade2 Devices (continued)				
Device	Temp-range	Speed-grade	Voltage	Timing/Power
MPFS160TS	TGrade2	STD, -1	1.0V, 1.05V	Production
MPFS250TS	TGrade2	STD, -1	1.0V, 1.05V	Production

1.2.2.3. Military Production Timing and Power (Ask a Question)

In the Libero SoC v2025.1 release, the following Military temperature range device achieves production timing and power.

Device	Temp-range	Speed-grade	Voltage	Timing/Power
MPFS460TS	MIL	STD	1.0V, 1.05V	Production

1.2.3. RT PolarFire (Ask a Question)

- The Libero SoC v2025.1 release introduces a new FC1509 package for RTPF500ZT/ZTS/ZTL/ZTLS devices.
- SSN analysis is added for CG1509 package for RTPF500ZT/TS/TL/TLS and RTPF500T/TS/TL/TLS devices.

1.2.4. RT PolarFire SoC (Ask a Question)

- Libero SoC v2025.1 introduces a new FC1509 package for RTPFS460ZT/ZTS/ZTL/ZTLS devices.
- Programming and SmartDebug support have been added for RTPFS460ZT/ZTS/ZTL/ZTLS and RTPFS160ZT/TS/TL/TLS devices.
- PFSOC_SCSM: SC_WAKE control is enabled by dynamic signals from fabric logic to allow temporary exit from System Controller Suspend mode to perform System Services.

1.3. Software Features and Enhancements (Ask a Question)

1.3.1. Enhanced copy and paste functionality for SmartDesign HDL+ cores (Ask a Question)

Starting with the Libero SoC v2025.1 release, HDL+ core instances can be selected and copied from a SmartDesign and pasted into a new SmartDesign in any order, regardless of their original creation and instantiation sequence, without corrupting the SmartDesign canvas component and resulting in crashes.

Additionally, crashes related to hierarchical SmartDesign creation with HDL+ core instances being selected have also been resolved.

1.3.2. Added STAPL Support to Program Micron MT25QL01G SPI-Flash (Ask a Question)

Libero SoC v2025.1 supports the export of STAPL files to program Micron MT25QL01G and MT25QL02G SPI-flash devices.

1.3.3. Enhanced the Automatic Programmer Detection Functionality (Ask a Question)

The Libero SoC 2025.1 release enhanced the programmer detection functionality in batch mode to automatically use the single programmer that is connected to the machine without having to explicitly specify it in TCL commands.

1.3.4. Availability of Multiple Servers in LM_LICENSE_FILE Environment Variable (Ask a Question)

Libero SoC v2025.1 supports automatic license checkout from a secondary floating license server specified in the LM_LICENSE_FILE environment variable. If the primary server is exhausted, the secondary server is used to check out a license. A Libero instance can also be opened on another machine using the secondary server.

1.3.5. Synplify Pro ME Upgrade (Ask a Question)

The Libero SoC v2025.1 release supports Synplify Pro ME version V-2023.09M-5, which introduces additional support for the following features in large memory blocks:

- RTG4 Dual-port Write-byte Enable
- Improved DSP inference report
- Complete TMR report
- Enhanced Performance QoR

1.3.6. Identify ME Tool Upgrade (Ask a Question)

Libero SoC v2025.1 supports Identify ME version V-2023.09M-5, which introduces additional support for RTG4 Pre-arm trigger. This version provides debug support for the following devices as well:

- RT PolarFire
- RT PolarFire SoC

1.3.7. ModelSim ME Pro and QuestaSim Pro ME Simulator Tools Upgrade (Ask a Question)

The Libero SoC v2025.1 release supports the upgraded v2024.3 versions of ModelSim ME Pro and QuestaSim ME simulation tools.

To enable better simulation runtime, QuestaSim ME optimizes designs during compilation by default. This optimization can sometimes result in the removal of signals or objects that the user might want to observe during simulation. The historical vsim argument called `-novopt` is now deprecated; instead, the simulator supports the `-voptargs` parameter, which allows users to add arguments that specify the level of optimization applied and the level of design object visibility during simulation. For example, the vsim argument `-voptargs=+acc` can be used to enable access to design objects that might otherwise be optimized away. For additional information, refer to the appropriate user guide from Siemens EDA (formerly Mentor Graphics).

Note: Libero SoC v2025.1 is the final release to use ModelSim ME Pro as the default simulator.

1.3.8. Improved Smart Time Analysis (Ask a Question)

The Libero SoC 2025.1 release has the following significant enhancements to the SmartTime tool:

- Ability to override the jitter value with clock uncertainty
- Support for Negative Uncertainty Values in SDC Editor
- Refined exception constraint resolution using *get_clocks*
- Generated clock duty-cycle update

1.3.9. Improved Error Messages Related to Networking (Ask a Question)

Feedback messages from network connectivity checks have been improved. In particular, the messaging for failures related to the *download_latest_cores* command has been enhanced for better clarity and troubleshooting.

1.3.10. New QT Installer for Libero SoC and Standalone Installers for Program and Debug, PolarFire SoC MSS, and MegaVault (Ask a Question)

The Libero SoC 2025.1 release introduces a new QT-based installer that serves as a single point installation source for all Libero SoC products and, at the same time, significantly reduces installation time. This also addresses an installation issue relating to long paths on Windows.

1.4. PolarFire, PolarFire SoC, RT PolarFire, and RT PolarFire SoC (Ask a Question)

1.4.1. PF_XCVR: Disable Scrambler in 64b66b (Ask a Question)

The Libero SoC v2025.1 release includes updates to support additional configurations for 64b6xb PCS mode. The new Gear Box option allows users to independently enable the following options for 64B66B / 64B67B modes:

- Scrambler/descrambler: This option can include or bypass the embedded scrambled/descrambler.
- Disparity (64b67b only)
- BER monitor state machine
- 32-bit data width

1.4.2. Octal DDR PHY DRC Limit Update (Ask a Question)

Starting with the Libero v2025.1 release, the FMAX for OCTAL_SPI IOD interfaces is increased from 400 Mbps to 500 Mbps for STD and -1 for all the GPIO and HSIO banks.

1.4.3. SUBLVDS 3.3V, 2.5V GPIO: Added 3mA Output Drive Setting (Ask a Question)

Starting with the Libero SoC v2025.1 release, Libero I/O editor support has been enhanced to add 3 mA output drive for SUBLVDS25 and SUBLVDS33 drive strength settings.

1.4.4. PF_IO Updates (Ask a Question)

Starting with the Libero SoC v2025.1 release, the PF_IO configurator enables the clock edge selection for the RX/TX/OE registers for both rising and falling clock edges.

1.4.5. Improved I/O Delays for QDR, SpaceWire (Ask a Question)

Libero SoC v2025.1 introduces enhancements to I/O delays for QDR and SpaceWire interfaces using LVDS 2.5V, HSTL 1.2V, and 1.5V standards. These improvements provide more accurate delay estimates for applicable designs.

1.4.6. PF_IOD_GENERIC_TX Hold Violations Repair (Ask a Question)

Libero SoC v2025.1 adds support to automatically repair hold violations for source-sync TX interfaces during Place and Route with Repair Minimum Delay Violations enabled. In some low hold violation situations, the repair min-delay violations process checks whether tap delay is OFF, in which case the repair process starts from tap delay 0 instead of expiring without taking any action.

1.4.7. Compile and Layout Reports: I/O Register Usage (Ask a Question)

Libero SoC v2025.1 clarifies I/O register usage details in the Compile and Layout reports.

1.4.8. Board Layout Report Updates (Ask a Question)

Starting with the Libero SoC v2025.1 release, the unused condition for some package pins has been updated.

1.4.9. I/O Bank Report Updates (Ask a Question)

Starting with the Libero SoC v2025.1 release , the I/O Bank report section has been updated to add auto-calibration information for all PolarFire and PolarFire SoC devices.

1.4.10. Ability to Perform Static Timing Analysis at IND Temp-range for MIL and T2 Devices (Ask a Question)

With the Libero SoC v2025.1 release, projects targeting PolarFire family FPGA and SoC device part numbers offered in MIL or automotive T2 temperature grade now include a **Project Settings** option for selecting the IND range for Analysis Operating Conditions used by static timing and power

analysis. This enhancement allows designers using MIL or T2 devices in systems that do not operate beyond the IND range to analyze static timing and power at more applicable conditions.

1.4.11. New SPI-Flash Programming Support (Ask a Question)

Starting with the Libero SoC v2025.1 release, SPI-Flash programming support has been added for the space-grade MRAM part number, AS302G208-0108X0MCEY, from Avalanche Technology.

1.4.12. Simulation Model Enhancements (Ask a Question)

The Libero SoC 2025.1 release has the following updates and enhancements to PolarFire Simulation models and addresses a few bugs in simulations:

- LSRAM ECC error injection: The PF_TPSRAM configurator now supports ECC error injection during pre-synthesis simulation by setting a defined mask address, as described in the PolarFire Family Fabric User Guide.
- PF_IOD_GENERIC_RX: Simulation of L0_LP_DATA and L0_LP_DATA_N at high-speed data transition
- PF_IOD_TX_CCC: Updated 3.5 clock ratio
- Added post-layout simulation for I/O registers with SDF
- IOREG BA Simulation Support for inverted clocks with Neg edge register values

1.4.13. Enhanced SmartDebug (Ask a Question)

Libero SoC v2025.1 introduces MSS DDR I/O training results,a new feature to SmartDebug.

This release also adds the following enhancements:

- Signal integrity settings persistence
- XCVR eye monitor: Persistent eye plot
- Fabric DDR I/O margin training results

1.5. RTG4, SmartFusion2, and IGLOO2 (Ask a Question)

1.5.1. RTG4FCCCECALIB: Update Core Configuration GUI to Dynamically Disable Unused Fields in Specific Modes (Ask a Question)

In the Libero SoC v2025.1 release, the RTG4FCCCECALIB core configuration GUI has been enhanced. Frequency fields in the Basic and Advanced tabs are now grayed out and disabled when the requested mode does not use the PLL or GPDs.

For example, when using the Clock Recovery Circuit as the source for a specific CCC output, the reference clock and requested output frequency fields are disabled. Similarly, when the PLL is bypassed, such as when using the internal 50MHz RC Oscillator or a direct CCC input as the source for a specific CCC output, the unused **Exact Frequency** checkbox is disabled.

1.5.2. SERDES Cores: Transmit De-Emphasis Re-calculated Per TX Amplitude Setting (Ask a Question)

The Libero SoC 2025.1 release enhances the GUI option in Serdes configurator to automatically compute correct Signal Integrity register values when the protocol of lane is XAUI/EPCS for SmartFusion2, IGLOO2, and RTG4 families.

1.5.3. Block Design Methodology: Propagate Chip-Level Hardwired Connections to the Top Module (Ask a Question)

Libero SoC v2025.1 adds support to propagate chip-level hardwired connections (for example, OSC_RC50MHZ, CCC to DELCAL) to the top module in block mode for SmartFusion2, IGLOO2, and RTG4 devices. This support resolves previous compile and layout issues specific to block design methodology.

1.5.4. SmartFusion2, IGLOO2: eNVM Simulation Model with Silicon Delay (Ask a Question)

The Libero SoC 2025.1 release adds parameters to eNVM simulation model that allow users to account for silicon delays stated in the device datasheet.

1.5.5. SmartFusion2, IGLOO2: Added SVF Programming (Ask a Question)

Libero SoC v2025.1 adds SVF programming support for SmartFusion2 and IGLOO2 devices.

1.5.6. RTG4 Report State of System Controller Suspend Mode Setting in the Programming Bitstream (Ask a Question)

The Libero SoC 2025.1 release enables the System Controller Suspend Mode project setting used in the design bitstream to be a part of all reports for the following tool actions for RTG4 devices:

- Generate Bitstream
- Export Bitstream
- Export FlashPro Express job
- Run PROGRAM action
- FlashPro Express when running PROGRAM action

2. Migrating Designs to Libero SoC (Ask a Question)

2.1. Core Enhancements and Upgrades (Ask a Question)

The following table lists core enhancements and upgrades in Libero SoC v2025.1. For more information about updating a core version, see section Updating a Core Version.

Table 2-1. Core Enhancements and Upgrades

Core	2025.1 Version	Status	Comments
CORESMARTBERT	2.11.100	Production	Core update to use the latest XCVR core version.
PF_DDR3	2.4.131	Production	Core update for ZQCS command, Reinitialization, ODT Removal, CK/CA additive offset value correction and cleaning up simulation warnings. See section PolarFire, PolarFire SoC, RT PolarFire, and RT PolarFire SoC.
PF_DDR4	2.5.120	Production	Core update for ZQCS command, Reinitialization, ODT Removal, CK/CA additive offset value correction and cleaning up simulation warnings. See section PolarFire, PolarFire SoC, RT PolarFire, and RT PolarFire SoC.
PF_INIT_MONITOR	2.0.308	Production	New FC1509 package added for RTPF500ZT/ZTS/ZTL/ZTLS RT PolarFire devices and for RTPFS460ZT/ZTS/ZTL/ZTLS RT PolarFire SoC devices.
PF_IO	2.0.105	Production	Core update for the clock edge selection for the RX/TX/OE register.
PF_IOD_TX_CCC	1.0.131	Production	Core update to produce TX_CLK_G output in 3.5 clock ratio.
PF_LPDDR3	2.3.125	Production	Core update for ZQCS command, Reinitialization, ODT Removal, CK/CA additive offset value correction and cleaning up simulation warnings. See section PolarFire, PolarFire SoC, RT PolarFire, and RT PolarFire SoC.
PF_XCVR_ERM	3.1.206	Production	Core updates for XCVR SDI presets - SD, HD and 3G.
PFSOC_INIT_MONITOR	1.0.309	Production	VDDI and calibration status enabled in PFSOC_INIT_MONITOR IP.
RTG4FCCCECALIB	2.2.100	Production	Allowed High-VCO frequency selected by the RTG4FCCCECALIB core is limited to the reduced range of 1.25x to 1.5x of the actual-VCO frequency. See section RTG4.
RTG4FDDRC		Production	Fix for DDR x16/x8 w/ ECC issue, FDDR FPLL calibration sequence update. See section RTG4.
RTG4FDDRC_INIT	2.0.200	Production	Fix for DDR x16/x8 w/ ECC issue, FDDR FPLL calibration sequence update. See section RTG4.
RTG4 PCIE_SERDES_IF	2.0.200	Production	Updated the enhanced PLL calibration to reduce the High-VCO frequency limit and to reduce the high-VCO dwell time from 150 us to 100 us in the RTG4 SerDes PCIe/XAUI SPLL calibration sequence. See section RTG4.
RTG4 PCIE_SERDES_IF_INIT	2.0.200	Production	Same as above.
RTG4 NPSS_SERDES_IF	2.0.200	Production	Same as above.
RTG4 NPSS_SERDES_IF_INIT	2.0.200	Production	Same as above.

2.2. Updating a Core Version (Ask a Question)

Perform the following procedure to update a core version:

1. Download the latest version of the core into your vault.
2. Upgrade each configured core in your design to the latest version by right-clicking the core component in the design hierarchy and selecting **Update Component Version**. The component is regenerated automatically.

Important: The **Update Component Version** option is now available on instances of core components in a SmartDesign canvas as well. In addition, the selected core version is downloaded automatically from the Update Component Version dialog itself if needed.

3. Review the SmartDesign components and user RTL files in which the core component has been instantiated. If the port-list of the core component is modified after updating to the new core version, right-click the core component's instance in the SmartDesign and select **Update Instance** to update its port-list. Check for any pin/port disconnections in the SmartDesign or for any new pins exposed on the core component's instance, and then connect them or tie them off as needed and regenerate the SmartDesign component.
4. Build Design Hierarchy and Derive the Timing Constraints again from the Constraint Manager tool to use the latest generated core timing constraints.
5. Rerun the design flow.

3. Resolved Issues (Ask a Question)

The following table lists the customer-reported defects and enhancement requests resolved in Libero SoC v2025.1 that have case numbers. Resolution of previously reported “Known Issues and Limitations” are also noted in this table.

Table 3-1. Customer-reported Defects and Enhancement Requests with Case Numbers

Case Number	Summary	Resolution
129520	After having constrained the output path with QDR Chip Setup / Hold and skew requirements, Libero layout could not find valid timing windows.	A calculated tightening of the derating for specific IOPADs allowed an improvement of QDR slack: • OCV deratings tightened based on Monte-Carlo Spice simulations. • Silicon to software derating tightened to account for IOPAD specificity (large drivers and wires). • Deratings limited to HSTL12/HSTL15 output pad (QDR) and LVDS25 output pad (SpaceWire).
140419	There was optimization issue for `-ignore_clock_latency` timing constraint.	When using **set_max_delay -ignore_clock_latency**, Place and Route ignores the clock path, and tries to minimize the placement for the data path.
141172	• The report incorrectly referenced timing as relative to the assertion of `FPGA_POR_N` signal, which is an active-low signal. • The report provided a single PUFT-related timing value without clarifying whether it represents the minimum, maximum, or typical value	The PUFT timing numbers in the Libero Reports have been enhanced and the message related to PUFT timing numbers has been updated.
141478	Different edges were chosen for setup and hold analysis when recompiling the same design without modifications.	An ambiguity has been removed in multicycle calculation when **-start** is used with **-setup** and **-hold** but with a different set of anchors.
141222	Incorrect clock edges were generated for hold analysis with **-invert** switch.	The **-invert** switch is used to correctly select the generated clock edges.
141198	Incorrect master clock was observed when clocks were muxed.	The issue has been fixed during clock propagation where a clock continues past another clock source.
141197	Incorrect information was observed in the CDC report for muxed clocks. There was an issue in the search for common ancestors in the CDC report that reported safe CDC as unsafe.	The issue has been fixed and such scenarios are now properly reported as safe.
140822	Verify timing crashed when a timing constraints file was supplied with 'create_generated_clock' missing all of the parameters divide_by / multiply_by or edges.	Validation has been added to the timing constraints to ensure divide_by / multiply_by or edges is included as a parameter.
140867	PF_IO: Libero v2024.2 has unconnected macros in PF_IO TRIBUFF / BIBUFF configuration.	The issue has been fixed.
140770	When connected to IOD interfaces, IOPADN:D and IOPADN:E were floating.	IOPADN:D and IOPADN:E are no longer floating and are now connected to their respective IOPADP:D and IOPADP:E pins for outbuf, tribuf and bibuf diff macros, if connected to IOD interfaces.

Table 3-1. Customer-reported Defects and Enhancement Requests with Case Numbers (continued)

Case Number	Summary	Resolution
137818	DDR simulations were failing due to Questasim optimization in Questasim ME Pro 2024.2 version.	This is now fixed in Questasim ME Pro 2024.3 version.
140667	An internal error in c_ver.exe occurred in SynplifyPro V202309M (Libero 2024.1) resulting in synthesis failure.	This is now fixed in SynplifyPro V-2023.09M-5 version.
140977	Output generation delay was specifically observed when both clock and reset signals were toggled at same time.	PF_CLK_DIV simulation model has been updated to resolve the delay in Output clock Generation after reset is asserted back.
140911	3mA out drive as an option for SUBLVDS25 and SUBLVDS33 GPIOs was missing.	3mA out drive has now been added as an option for SUBLVDS25 and SUBLVDS33 GPIOs.
140361	Libero was crashing during the **Generate FPGA Array** action.	This issue was occurring because the action was trying to open a SmartDesign that was corrupted due to the use of copy / paste functionality to instantiate HDL+ cores within the SmartDesign. This issue related to the copy / paste functionality of HDL+ cores has been resolved.
140306	There was discrepancy between the port name and pin number for the differential I/O in the Global Net report.	This issue has been resolved by indicating always using the P side of the differential I/O port in the report.
140882	In the generated vm netlist, INIT string of MACC_PA_BC_ROM was incorrectly written in binary format, even though it is pre-fixed as 288'h in Synplify V-2023.09M (2024.1) and Synplify V-2023.09M-3(2024.2).	This INIT string of MACC_PA_BC_ROM in the generated netlist is now correctly written in hex format in SynplifyPro V-2023.09M-5.
140296	The SSN Analyzer was experiencing crashes when used with the MPF300T-FCG784N device.	This issue has been fixed as the supported SSN Analyzer for FCG784N device used FCG784 SSO data, as both packages are identical in terms of SSO.
140136	Synthesis failed due to an internal error, @E: BN705, during optimization stage.	This is now resolved in SynplifyPro V-2023.09M-5.
140181	Synplify tool incorrectly reported warnings of insufficient block RAM resources even though the design didn't fully utilize block RAMs of the specific device.	This incorrect warning is now removed in SynplifyPro V-2023.09M-5.
140239	There was an issue with reading the DSN value of RTG4 devices at the end of the programming action.	The programming algorithm has been changed to read the DSN value before exiting programming mode.
140082	Disabling ODT for Rank0 in the PolarFire DDR3 controller IP had no effect—the I/O Editor and IBIS model continue to reflect ODT as enabled, resulting in no distinction in generated files or write behavior.	PF_ DDR3/DDR4/LPDDR3 core has been updated to remove the "ODT Activation Settings on Read" option.
140153	There was an issue with DDR3 IBIS Model generated using Libero SoC V2024.2.	The APIs responsible for dumping the model selector for BIDIR I/Os have been corrected.
140258	There was BA simulation errors with the 'ODT_DYNAMIC_UNIT' macro.	The 'ODT_DYNAMIC_UNIT' simulation model has been updated to enable BA simulation.
140041	'Generate bitstream' was failing when using an eNVM client memory file filled with 0s which exceeds 37KB size.	The software has been updated to efficiently check if the first page of eNVM is filled with zeroes.

Table 3-1. Customer-reported Defects and Enhancement Requests with Case Numbers (continued)

Case Number	Summary	Resolution
139884	'#N/A' was seen when MPE report was imported in Power Estimator, specifically for Transceiver related fields.	Fix has been added in Power Estimator to correctly identify XCVR lanes as well as populate certain fields with default values in places of updating with "--".
139848	In the Aldec simulation flow, the incorrect asim command was getting generating.	The `run.do` generation has been updated to use `PolarFire asim` command for both PolarFire and PolarFireSoC devices. This resolves the previous requirement for manual `vmap` adjustment.
140190	The output clock and data of the PF_IOD_GENERIC_TX were not centered in some cases because of an active DLL.	The issue has been fixed by adding an inactive DLL and connecting to the interface, if needed.
139519	Compile was not checking if some pins were connected to top ports in the block mode.	The check has been added to handle such cases correctly.
139301	Synthesis failed due to an internal error, @E: BN707, during the optimization stage.	This is now resolved in SynplifyPro V-2023.09M-5.
139341	Libero did not error out for invalid SPI-Flash stage 3 key binding in combinations with custom security settings.	Libero now errors out for invalid combinations of SPI-Flash stage 3 key binding with respect to custom security settings.
139180	System Controller Suspend Mode information was missing in the logs.	The System Controller suspend mode information have now been added to the logs.
139229	SmartTime created 2 clock domains when using differential IO.	This issue has been fixed to create only one clock domain in such scenario.
139049	Enabling the **Enable RX_CLK_ODT_EN** for LVDS failsafe option in the RX configurator and selecting "Clock to data relationship" as Dynamic, Centered, or Aligned (but not Fractional), resulted in a non-functional design on silicon.	The issue has been fixed and users should rerun Place and Route to see the fix.
138867	Libero was crashing when trying to generate a SmartDesign component in a design.	This issue was occurring because the action was trying to open a SmartDesign that was corrupted due to the use of copy / paste functionality to instantiate HDL+ cores within the SmartDesign. This issue related to the copy / paste functionality of HDL+ cores has been resolved.
138956	Complie netlist failed because of an issue with the synthesis-generated netlist.	This is now resolved in SynplifyPro V-2023.09M-5.
138852	There were discrepancies in I/O register combining reports between the IOREG, compile and layout reports.	The compile report and layout log have been enhanced to report more details about the IOREG combining and data have been made consistent across all reports.
140526	There was issue with PF_DDRx support for ZQCS commands.	The issues in system generated core have been fixed and validation completed for all PF_DDRx cores.
138620	Identify Instrumentor failed with Internal Error in c_vhdl.exe for certain designs.	This issue has been resolved In Identify V-2023.09M-5.
138631	There were issues with Globals Assigner Convergence.	Optimization objectives have now been relaxed to avoid long runtimes.
138318	**System Suspend Mode** option was shown in the compile report in the RTG4 designs; users were allowed to change it later in the flow leading to confusion.	This option has been removed from the compile report since it can be changed later in the flow.

Table 3-1. Customer-reported Defects and Enhancement Requests with Case Numbers (continued)

Case Number	Summary	Resolution
138226	An error occurred during BA simulation on an MPF design containing a register triggered on the negative edge combined with an output.	PF_IOREG simulation model is now updated with missing timing arcs to cover different edges of clocks in BA simulation.
138474	**Generate bitstream** was failing when content was filled with zeros greater than 37 KB present.	The software has been updated to efficiently check if first page of eNVM is filled with zeroes.
141664	Multiple top-level candidates in the design were encountered which stopped the compilation.	Top module information now passes all the time in the `synplify prj` file and all conditional dependencies have been removed.
137765	There was issue with cross-probing from SmartTime to Netlist viewer.	In Libero SoC 11.X releases, the 'Show in Chip Planner' functionality in SmartTime highlighted the selected object in the Floorplan view and created a Logical Cone in the Netlist Viewer with that object in the Chip Planner. In Libero 12.X and 202X.X releases, the cross-probing feature has been retained, but the logical cone creation part has been removed. This is because the cone already exists at the bottom of the SmartTime window. Now, the 'Show in Chip Planner' functionality in SmartTime highlights the selected item on the NLV canvas within the Chip Planner application. Additionally, it ensures that the **Zoom and Center** toggle is switched on for cross-probing to work as expected.
138111	The Transceiver Configurator-generated settings for 'Lock To Data with 2x gain' for 100T were incorrect.	PF_XCVR: The CDR mode lock to data with 2x gain settings has been updated for more robust functionality.
137621	SI values entered in configurators resulted in invalid resolutions without warning users to maintain valid ratio constraints.	The formula to compute values has been enhanced to all the supported Amplitude values (100/400/800/1200 mv).
137099	There was huge difference in resource utilization for two identical set of HDLs.	The resource utilization of these two identical set of HDLs are now comparable in SynplifyPro V-2023.09M-5.
136902	The constraints were not being considered in a project after unlinking and re-importing the constraint files.	Constraint file references remain part of top module even when the file that caused the issues is deleted. This issue has been resolved.
137134	New SPI Flash Device support with FlashPro 6.	Added support for Space Grade QSPI MRAM AS302G208-0108X0MCEY.
137028	SynplifyPro tool reports incorrect warning about `syn_radhardlevel` directive not being applied inspite of the attribute being implemented correctly	This incorrect warning is now removed in SynplifyPro V-2023.09M-5.
136789	Synthesis fails with internal error in m_generic.exe.	This crash is now fixed in SynplifyPro V-2023.09M-5.
136573	'PF_IOD_TX_CCC IP' core with 3.5 clock ratio not producing the 'TX_CLK_G' output.	This issue was present for clock ratio 3.5 with data rate less than 400 Mbps as the connectivity was missing. This has been fixed.
136216	Generated clocks were not analyzed in SmartTime UI.	This issue has been fixed in SmartTime initialization that prevented generated clock from being calculated.

Table 3-1. Customer-reported Defects and Enhancement Requests with Case Numbers (continued)

Case Number	Summary	Resolution
138338	IO Editor didn't allow different VICM range setting on per IO-pair basis within a bank.	The constraint on different VICM range has been relaxed in I/O Bank Assigner.
135489	RTG4CCCECALIB Spacewire application's Clock recovery mode.	Basic tab's Exact Value for Frequency has been disabled and Actual Value has been removed. The Reference clock frequency is disabled when PLL is in bypass mode.
135423	PF_IOD: The **L0_LP_DATA** and **L0_LP_DATA_N** of the PF_IOD_GENERIC_RX IP were toggling during the high-speed data transition.	PF_IOD_GENERIC_RX simulation model is now updated for a user to control on toggling of **L0_LP_DATA** and **L0_LP_DATA_N** during high-speed data transition through vsim commands.
135492	New STAPL feature support is added to program Micron MT25QL01G SPI-Flash devices.	A new feature has been added to export STAPL files to program Micron MT25QL01G and MT25QL02G devices.
134870	User control is enabled over page read and write timings. The vsim commands are utilized to emulate silicon-like timing accuracy.	The eNVM simulation model has been updated to offer user control on timings of page read and write operations.
134335	Constraint Manager GUI did not accept negative values for simple clock uncertainty, resulting in negative edge uncertainty values being excluded from detailed timing analysis calculations.	Negative clock uncertainty has been added for jitter calculations.
141243	The design contained modules instantiating themselves that resulted in crash and generated error: 'Unable to find the file '.edf', cannot add it to Libero project'.	This issue is now handled without a crash.
138709	In the FDDR IP with the DQ 16-bit with SECDED enabled, the single DDR memory address location couldn't be accessed and ended up with a trap handler issue in the SoftConsole.	FDDR IP for 16-bit and 8-bit modes with ECC enabled have been updated to map top-level DQ_ECC ports correctly to FDDR_DQ_ECC[#] package pins for proper ECC functionality.
141676	RTG4 FDDR Controller in 8-bit or 16-bit width mode with ECC enabled had a bug.	The bug has been fixed by adding a message in compile for the RTG4 FDDR Controller in 8-bit or 16-bit width mode with ECC enabled to catch the attention of users to check the documentation on how to connect the ECC pins.
131218	Libero crashed when trying to open a project.	This issue was occurring because the action was trying to open a SmartDesign that was corrupted due to the use of copy / paste functionality to instantiate HDL+ cores within the SmartDesign. This issue related to the copy / paste functionality of HDL+ cores has been resolved.
131579	In PF_XCVR v3.1.200, enabling the scrambler / descrambler option in 64b / 66b mode had no effect on the generated simulation model, which led to mismatched simulation behavior.	A new Gear Box option for 64B66B / 64B67B modes now adds support for expanded 64b6xb PCS configurations to independently enable scrambler / descrambler, disparity (64b/67b only), BER monitor, and 32-bit data width.
131051	Libero was crashing when opening a project.	This issue was occurring because the action was trying to open a SmartDesign that was corrupted due to the use of copy / paste functionality to instantiate HDL+ cores within the SmartDesign. This issue related to the copy / paste functionality of HDL+ cores has been resolved.

Table 3-1. Customer-reported Defects and Enhancement Requests with Case Numbers (continued)

Case Number	Summary	Resolution
131060	In x16 ECC configuration, the MSS configurator incorrectly assigned ECC bits to DQ[16–19] instead of DQ[32–33], and misleadingly indicated usage of DQ[18–19] for write calibration, which is handled by the core in both x16 and x32 configurations.	MSS_DDR 16-bit with ECC enabled update ensures correct ECC byte-lane assignment in the MSS Configurator component XML and enables proper DDR memory training.
134041	PF_IOD: There was timing check issue with the Octal PHY.	The check arcs related to pause and reset have been removed from LANECTRL simulation model to remove the unwanted warnings that appeared during BA simulation.
130222	There was timing check issue with the Octal PHY.	Timing check related to PAUSE / RESET of LANECTRL is not applied in status timing analysis. These check arcs have been removed from timing model.
130074	There was issue with Libero Smart Debug Eye Monitor with PolarFire XCVR design.	Intermittent eye collapse issues have been resolved during lane tests and traffic. Intermittent 0- Eye opening is now observed if there is signal integrity setting mismatch between Tx and Rx.
92700	PF_DDR3/4: Warnings were observed in Fast training mode simulations.	PF_DDR3 / DDR4 / LPDDR3 cores are now updated to remove simulation warnings related to Read Gate Training & Fast simulation warnings.
127207	Libero crashed when trying to open a project.	This issue was occurring because the action was trying to open a SmartDesign that was corrupted due to the use of copy / paste functionality to instantiate HDL+ cores within the SmartDesign. This issue related to the copy / paste functionality of HDL+ cores has been resolved.
128190	Incorrect error message was printed when 'download_latest_core' command was called with no internet access.	A functionality has been added to check the internet access. If there is no access, the user is notified.
126645	Libero crashed when trying to open a project.	This issue was occurring because the action was trying to open a SmartDesign that was corrupted due to the use of copy / paste functionality to instantiate HDL+ cores within the SmartDesign. This issue related to the copy / paste functionality of HDL+ cores has been resolved.
124376	Libero does not checkout the license from the 2nd floating server specified in 'LM_LICENSE_FILE' when all seats of the first floating server are occupied.	See section Availability of Multiple Servers in LM_LICENSE_FILE Environment Variable.
120591	New feature support to show MSS DDR memory training results.	A new feature is introduced to display MSS DDR memory training results.
123950	The `get_clocks` command has been resolved to registers in exception constraints, resulting in the command ignoring input and output delays.	`get_clocks` command for the **-from** and **-to** options for all exception constraints (`set_false_path`, `set_max_delay`, `set_min_delay`, `set_multicycle_path`) have been resolved on clock objects instead of all clock pins(or data pins for **-to** options) of the registers from that clock domain. Resolving `get_clocks` on clock objects solves the exceptions matching on input to register and register to output paths.

The following table lists the customer-reported defects and enhancement requests resolved in Libero SoC v2025.1 that do not have case numbers. Resolution of previously reported “Known Issues and Limitations” are also noted in this table.

Table 3-2. Customer-reported Defects and Enhancement Requests (No Case Numbers)

Summary	Resolution
CoreAXI4SRAM is an invisible core in the catalog.	CoreAXI4SRAM is now hidden in the catalog.
Libero web links have been updated from 'Microsemi' to 'Microchip'.	The start page has been updated with new links and the connection checking logic has been changed to support new links.
PF_LSRAM simulation model is enhanced to support ECC error injection.	• Verilog task & Python script-based solution has been introduced to emulate/simulate the ECC flag assertion. • Users can now use this solution with any existing Libero project but only with 2025.1 simulation libraries. • The changes in user design afre only limited to `run.do`.
Invalid temperature ranges are now accepted using TCL to generate a new project.	A new check has been added in the TCL command to restrict users from setting a custom range for the PolarFire and PolarFireSoC families. The same check has already been added for UI for hiding the custom range in 'Project' settings.
Programmer Detection should be automatic for new projects and TCL script.	The parameter `-programmer`for command `auto_construct_job_project` is now optional. If the parameter is omitted and a single programmer is connected to the host machine, the command executes successfully.
Libero SmartDebug SI settings persistence shows modified settings in subsequent SmartDebug launches which may not match actual settings in the device.	The SmartDebug SI settings feature now includes a pop-up message prompting users to choose between user-configured settings and modified settings when loading parameters. Additionally, a radio button on the SI settings UI allows users to switch between these two options.
Projects targeting PolarFire family FPGA and SoC device part numbers offered in MIL or automotive T2 temperature grade now supports IND range for Analysis Operating Conditions used by static timing and power analysis.	**Project Settings** option is now used to select the IND range for Analysis Operating Conditions used by static timing and power analysis. This enhancement allows designers using MIL or T2 devices in systems that do not operate beyond the IND range to analyze static timing and power at more applicable conditions.
Lane controller timing model doesn't match user configuration options.	Lane controller timing model is updated by adding delay step into arc delay calculation.
Enabled Repair Hold Violations of Source-sync Interface during P&R with Repair Minimum Delay Violations.	See section PF_IOD_GENERIC_TX Hold Violations Repair.
P&R interpretation of single asynchronous clock group timing constraint.	Clocks belonging to a single asynchronous clock group timing constraint won't be asynchnronous to each other.
Timing of some path constraints on output ports were missing in placer.	Timing propagation has been enabled to handle max / min-delay constraints on output ports. Also, the bus index has been added in importer to locate relevant port names.
Timing analysis ignored generated clock with register clock pins as source.	Generated clock now correctly analyzes in this scenario.
Clock generation was 0 when the source is a bidirectional port.	This issue has been fixed when a generated clock is set on a bidirectional I/O that prevented the clock generation to be calculated correctly in min-delay analysis.
Identify tool to support pre-armed triggers for RTG4 devices.	Identify V-2023.09M-5 now supports pre-configuring or pre-arming triggers that allows capturing error events that occur immediately after reset during startup or initialization before the system is operational.
RAM inference was incorrect and registers were getting inferred in addition to LSRAMs.	Register packing now happens correctly and only LSRAMs are inferred in SynplifyPro V-2023.09M-5.

Table 3-2. Customer-reported Defects and Enhancement Requests (No Case Numbers) (continued)

Summary	Resolution
Simulator and port width mismatches simulation warnings.	PF_DDR3/DDR4/LPDDR3 cores are now updated to remove simulation warnings related to Read Gate Training & Fast simulation warnings.
New part numbers added.	The new part numbers, MPFS025TS-FCSG325T2, PolarFireSoC, MPFS025TS, FCSG325, STD, and TGrade2, have been added to the software.
There were issues in meeting min-delay timing without RTL changes.	The search scope has been expanded for inserting delay buffers in min-delay repair.
In the absence of 'sdf' file, the P & N path tool different delay values until they were compared at IODPAP_IN_VCCI macro & hence, comparison was showing some unknows.	The IOPADN_IN_VCCI simulation model is updated by correcting the default delay of 10 ps
License checks have been added post creation for partner IPs.	Libero SoC now have licensing checks for partner IPs at the time of creation as well as after creation.

4. Known Issues and Limitations (Ask a Question)

For information about currently known issues and limitations related to the Libero SoC Design Suite, visit Libero SoC Design Suite Release Notes - Known Issues and Limitations.

5. Additional References (Ask a Question)

5.1. Related Release Notes (Ask a Question)

In addition to this release notes, you may find the information in the following release notes helpful.

- PolarFire SoC MSS Configurator v2025.1 Release Notes
- Programming and Debug Tools v2025.1 Release Notes
- SmartHLS Release Notes

5.2. Documents Updated in This Release (Ask a Question)

Libero documentation is updated frequently. To view the updated information, see Libero SoC Design Suite Help Documentation.

Important: To download the Libero SoC Design Suite help documentation and refer to it offline, visit Download Libero SoC Design Suite Help Documentation.

6. Revision History (Ask a Question)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
B	07/2027	In section ModelSim ME Pro and QuestaSim Pro ME Simulator Tools Upgrade, mentioned that QuestaSim ME optimizes designs during compilation by default, but that this optimization can sometimes result in the removal of signals or objects that the user might want to observe during simulation.
A	06/2025	Initial Revision

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