Release Notes
Libero SoC v2025.2

Introduction (Ask a Question)

The Libero® SoC Design Suite offers high productivity with its comprehensive, easy-to-learn, easy-to-adopt development tools for designing with Microchip FPGA and SoC device families. It provides you with an integrated hardware tool suite incorporating RTL entry through bitstream programming, a rich IP library, and complete reference designs and development kits. Libero SoC Design Suite includes SmartHLS® compiler software for abstracted high-level synthesis development flow, which shortens design time, simplifies verification, and accelerates time to market for designs using our FPGAs.

Use Libero SoC v2025.2 for designing with the following Microchip devices:

- RT PolarFire, RT PolarFire SoC and RTG4™ Rad-Tolerant FPGAs
- PolarFire® SoC and SmartFusion® 2 SoC FPGAs
- PolarFire and IGLOO® 2 FPGAs

To design with older Microchip FPGA family devices, use Libero SoC v11.10 or Libero IDE v9.3 and its subsequent service packs.

To access datasheets, silicon user guides, tutorials, and application notes, visit the Microchip website, navigate to the relevant product family page, and then click the **Documentation** tab. Development kits and boards are listed in the **Kits and Hardware** tab.

Important: Libero SoC v2025.2 does not support Classic Constraint flow. IGLOO2, SmartFusion2, and RTG4 projects using the "Classic" flow cannot be opened in this release. A migration path is available for transitioning from the Classic Constraint Flow to the Enhanced Constraint Flow. For more information, see Migrating an Existing Project Created with Classic Constraint Flow to Enhanced Constraint Flow.

You can find a comprehensive library of Libero SoC Design Suite Release Notes to explore previous and current release updates.

Download Libero SoC v2025.2 Software (Ask a Question)

You can download the Libero SoC v2025.2 Design Suite and related software from the Libero® SoC Design Suite 12.x and Later Versions page.

Important: Administrative privileges are required for installing the Libero SoC v2025.2 Design Suite software on the Windows® operating system.

1.1. Verify Software Downloads Using MD5 and SHA256 Checksum (Ask a Question)

To verify software downloads using MD5 and SHA256 checksums, use the appropriate procedure for your operating system:

- For Windows operating systems, enter the following at the command prompt: `certutil -hashfile [FILENAME] [HASH]`.
- For Linux® operating systems, enter the following command on terminal: `md5sum <path_to_installer>` or `sha256sum <path_to_installer>`.

1.2. Floating License Daemon Support (Ask a Question)

Microchip now supports 64-bit floating licensing daemons with FlexLM v11.19 for Libero SoC Design Suite (actlmgrd) that include Synopsys Synplify Pro®/Identify Pro® ME (snpslmd) and Siemens ModelSim/QuestaSim® ME (saltd,which replaces the previous mgcld).

Before opening Libero SoC v2025.2, perform the following procedure to upgrade your systems:

1. Upgrade existing daemons from v11.16 to v11.19. The v11.19 daemons available for downloading appear under the **Daemons Downloads** link on the following Microchip web page: www.microchip.com/libero.
2. Install the upgraded license available on your microchipDIRECT account (Microchip updated all existing active floating licenses to support the new saltd daemons): www.microchipdirect.com/fpga-software-products.

This bundle is backward-compatible with all previous Libero SoC releases.

Starting with Libero SoC v2024.2, the latest 64-bit license daemons with FlexLM v11.19 are required for all floating license users. For all current floating license users who recently received a new license file due to renewal or upgrade, please download and set up the latest daemons as well.

System Requirements (Ask a Question)

This section provides information about supported operating systems, system memory requirements, and other recommendations.

2.1. Supported Operating Systems (Ask a Question)

Libero SoC Design Suite supports the following 64-bit operating systems:

- Microsoft® Windows 11.0
- Red Hat® Enterprise Linux (RHEL) 8.3-8.10, AlmaLinux® 8.3-8.10
- Ubuntu® 22.04.3 LTS

Attention:

- Support for Windows 10 has been discontinued in Libero SoC starting with the 2025.1 release.
- Siemens ModelSim Pro does not directly support the Ubuntu platform. However, users can successfully install and run ModelSim Pro and QuestaSim Pro ME on Ubuntu by installing the necessary libraries. Libero provides the script *check_linux_req.sh* to install required system packages for Ubuntu.
- Libero SoC design suite has been tested on x86 and x64 processor-based machines only.

2.2. System Memory Recommendations (Ask a Question)

A minimum of 32 GB of Random-Access Memory (RAM) is recommended for implementing designs on MPF500T, MPFS460T, and RT PolarFire FPGA and SoC devices. For all other devices, a minimum of 16 GB of RAM is recommended.

Table of Contents

1. New in This Version (Ask a Question)

This section contains information about new features, devices, and enhancements introduced in the Libero v2025.2 Design Suite.

1.1. Changes That Address Important Issues (Ask a Question)

1.1.1. PolarFire, PolarFire SoC, RT PolarFire, and RT PolarFire SoC (Ask a Question)

1.1.1.1. IOD TX Ratio 5, Single-ended Data Output (Ask a Question)

Enhanced the Design Rule Check (DRC) process to ensure that the N-side of the IOD pair is correctly restricted and not available for use when configured for single-ended data output.

1.1.1.2. Preferred Clock Input (Ask a Question)

1.1.1.2.1. MPF500T/TS/TL/TLS, RTPF500T/TS/TL/TLS, RTPF500ZT/TS/TL/TLS (Ask a Question)

Enabled the REF_CLK I/O from Transceiver QUAD4 of these devices.

1.1.1.2.2. MPFS460T/TS/TL/TLS, RTPFS460ZT/TS/TL/TLS (Ask a Question)

Enabled the REF_CLK I/O from Transceiver QUAD4 of these devices.

1.1.1.2.3. MPFS025T/TS/TL/TLS (Ask a Question)

Enabled the preferred clock input I/Os to the two PLLs located at the SE corner of these device.

1.1.1.2.4. Periphery Placement (Ask a Question)

Implemented automatic assignment of DLL and PLL blocks when cascaded.

1.1.2. PolarFire SoC Standalone MSS Configurator (Ask a Question)

1.1.2.1. New Physical Memory Protection (PMP) Lockdown Strategies (Ask a Question)

The Libero SoC 2025.2 release has the following significant enhancements to the PMP Lockdown Strategies:

- Reorganized the PMP interface layout for more efficient configuration reducing complexity.
- Added an **Expert Mode** option that allows direct configuration of PMP register settings by advanced users who require direct control over PMP and MPU configurations.

1.1.2.2. DDR Partition (Ask a Question)

Reorganized the DDR memory partition settings to a dedicated tab, improving usability and making it easier to manage and visualize memory allocation within MSS DDR.

1.1.2.3. I²C Voltage (Ask a Question)

Expanded the MSS I/O support to operate at 2.5 V when interfacing with I²C peripherals, increasing flexibility and supporting a broader range of external I²C devices.

1.1.2.4. CAN Voltage (Ask a Question)

Expanded the MSS I/O support to operate at 1.2 V, 1.5 V, 1.8 V, and 2.5 V to enable additional Low Voltage CMOS I/O standards for MSS CAN controller I/O connection to external CAN transceiver, where supported by user board design and transceiver specifications.

1.1.2.5. Enhanced Simulation Support for Processor BFM and Tiny QoS AXI Initiator (Ask a Question)

The **mss_cpu_core** can access the non-cache region of MSS DDR through the **M14** port of the **AXI** switch. To mimic the processor behavior during simulation, you can choose to enable either the Processor BFM for the **mss_cpu_core** or a tiny QoS AXI Initiator, depending on your verification needs.

2. Software Features and Enhancements (Ask a Question)

2.1. SPI Flash Clients (Ask a Question)

Libero SoC v2025.2 now provides enhanced flexibility when configuring SPI Flash clients.

- If the SPI bitstream client is not present, you can create SPI data storage clients at any address, including those below 0x400, allowing for more versatile memory mapping.
- Inserted a "Key Mode" column to the "SPI Flash Clients" table to display the key (KLK/UEK1/UEK2) used for encrypting SPI bitstream file, providing clearer visibility into expected pre-programmed security settings.

2.2. Serial Flash Memory (Ask a Question)

The Libero SoC 2025.2 release supports multiple Serial Flash devices:

- Winbond W25Q64JV: Added support on FlashPro6 and STAPL file generation for programming with any STAPL player from third-party vendors.
- Micron MT25QL128ABA: Added STAPL file generation support for programming with any STAPL player from third-party vendors.

2.3. Tool Upgrades (Ask a Question)

The Libero SoC v2025.2 release supports the upgraded version, W-2025.03M-SP1-1, of Synplify Pro ME and Identify ME Debugger tools.

3. PolarFire, PolarFire SoC, RT PolarFire, and RT PolarFire SoC (Ask a Question)

3.1. Simulation Model Enhancements (Ask a Question)

The Libero SoC v2025.2 release has the following updates and enhancements to PolarFire Simulation models:

- Added post-layout back-annotated simulation support for Differential input I/O.
- Added simulation support for wide-mode programmable input delay taps in PF_IO and PF_IOD_GENERIC_RX cores.

3.2. IOD Octal DDR Enhancements (Ask a Question)

Libero SoC v2025.2 introduces several enhancements to improve configurability, timing, and simulation accuracy for IOD Octal DDR:

- **PLL_POWERDOWN_N** is now exposed by default to facilitate enabling of the PLL only when the **REF_CLK** input is stable.
- Added **DQS_DELAY_TAP** options up to 139 for expanded tuning flexibility.
- Any tap value in the full range of 1–255 allowed for the DQS delay setting.
- Added support for non-integer clock frequency entry to accommodate a wider range of design requirements.
- Improved timing constraints generation to ensure better coverage and timing robustness.
- Improved performance by inserting two-stage pipeline and register duplication for Async-assert, Sync-deassert Reset.

3.3. IOD RX Updates (Ask a Question)

The Libero SoC v2025.2 release enables Expose fractional clock parallel data in the Fractional Dynamic mode.

3.4. Added Failsafe ODT_EN Support for SPACEWIRE_RX (Ask a Question)

Libero SoC v2025.2 adds the option to expose the **Failsafe ODT_EN** port for the **SPACEWIRE_RX** core interface.

3.5. Added DLL Register in the Design Initialization Report (Ask a Question)

The Libero SoC v2025.2 release adds DLL register details in the Design Initialization report.

3.6. Added Support for Initial Static Delay on Dynamically Tuned I/O Interfaces (Ask a Question)

Libero SoC v2025.2 allows **IN_DELAY** and **OUT_DELAY** options in PDC and I/O Editor for Dynamic I/O interfaces (except DDR, LPDDR, QDR, CDR) to set the initial startup delay value, which can be dynamically tuned during operation.

3.7. Enhanced PF_SRAM_AHBL_AXI with High-Reliability Options (Ask a Question)

Libero SoC v2025.2 adds new options for high reliability to enable fault tolerance logic, synchronous reset, and timeout counts for read and write operations on the AHBL or AXI interface.

3.8. Enabled Fault Tolerance for PF_SYSTEM_SERVICES (Ask a Question)

The Libero SoC v2025.2 release adds new options for high reliability to enable fault tolerance logic in the PF_SYSTEM_SERVICES core.

3.9. CoreAXI4Interconnect and CoreAHB-Lite Cores (Ask a Question)

Libero SoC v2025.2 refreshes the Memory Map definitions with the new initiator and target terminologies for CoreAXI4Interconnect and CoreAHB-Lite cores.

3.10. Expanded Live Probe Trigger Controls in SmartDebug (Ask a Question)

Libero SoC v2025.2 adds support for selecting trigger signal's edge in SmartDebug when a signal is assigned to Live Probe that acts as a trigger.

3.11. Upgraded Silver License to Add Support for MPF200T-FCG784 (Ask a Question)

The Libero SoC 2025.2 release upgrades the Silver license for MPF200T device (FCG784 package), with extended device range enabled.

4. RTG4 (Ask a Question)

4.1. Enhanced RTG4_SRAM_AHBL_AXI with High-Reliability Options (Ask a Question)

Libero SoC v2025.2 adds new options for high reliability to enable fault tolerance logic, synchronous reset, and timeout counts for read and write operations on the AHBL or AXI interface.

5. Migrating Designs to Libero SoC (Ask a Question)

5.1. Core Enhancements and Upgrades (Ask a Question)

The following table lists core enhancements and upgrades in Libero SoC v2025.2. For more information about updating a core version, see the section Updating a Core Version.

Table 5-1. Core Enhancements and Upgrades

Core	2025.2 Version	Status	Comments
PF_CCC	2.2.222	Production	Added fix for incorrect configurator-generated settings for PolarFire DLL in Phase Generation Mode.
PF_IO	2.0.106	Production	Added support for Delay mode feature with two options, **Narrow** and **Wide**, with delay tap range support of 0-127 and 0-255, respectively.
PF_IOD_GENERIC_RX	2.1.116	Production	Added support for fractional clock parallel data in fractional dynamic mode.
PF_IOD_OCTAL_DDR	2.0.113	Production	Improved configurability, timing, and simulation accuracy for IOD Octal DDR. See the IOD Octal DDR Enhancements section.
PF_RGMII_TO_GMII	1.3.111	Production	Repackaged to include the latest PF_IOD_GENERIC_RX version.
PF_SRAM_AHBL_AXI	1.2.115	Production	High-reliability options added for PF_SRAM_AHBL_AXI with CoreAHBLSRAM_PF v3.0 and CoreAXI4SRAM v3.0. See the Enhanced PF_SRAM_AHBL_AXI with High-Reliability Options section.
PF_SYSTEM_SERVICES	3.0.104	Production	High-reliability options added for PF_SYSTEM_SERVICES with CoreSysServices_PF v4.0. See the Enabled Fault Tolerance for PF_SYSTEM_SERVICES section.
PF_SPACEWIRE_RX_PHY	1.0.110	Production	Added the option to expose the Failsafe ODT_EN port for the SPACEWIRE_RX core interface. See the Added Failsafe ODT_EN Support for SPACEWIRE_RX section.
RTG4_SRAM_AHBL_AXI	1.0.123	Production	High-reliability options added for RTG4_SRAM_AHBL_AXI with CoreAHBLSRAM_PF v3.0 and CoreAXI4SRAM v3.0. See the Enhanced RTG4_SRAM_AHBL_AXI with High-Reliability Options section.

5.2. Updating a Core Version (Ask a Question)

Perform the following procedure to update a core version:

1. Download the latest version of the core into your vault.
2. Upgrade each configured core in your design to the latest version by right-clicking the core component in the design hierarchy and selecting **Update Component Version**. The component is regenerated automatically.

> **Important:** The **Update Component Version** option is now available on instances of core components in a SmartDesign canvas as well. In addition, the selected core version is downloaded automatically from the Update Component Version dialog itself if needed.

3. Review the SmartDesign components and user RTL files in which the core component has been instantiated. If the port-list of the core component is modified after updating to the new core version, right-click the core component's instance in the SmartDesign and select **Update Instance** to update its port-list. Check for any pin/port disconnections in the SmartDesign or for any new pins exposed on the core component's instance, and then connect them or tie them off as needed and regenerate the SmartDesign component.

4. Build Design Hierarchy and Derive the Timing Constraints again from the Constraint Manager tool to use the latest generated core timing constraints.
5. Rerun the design flow.

6. Resolved Issues (Ask a Question)

The following table lists the customer-reported defects and enhancement requests resolved in Libero SoC v2025.2 that have case numbers. Resolution of previously reported “Known Issues and Limitations” are also noted in this table.

Table 6-1. Customer-reported Defects and Enhancement Requests with Case Numbers

Case Number	Summary	Resolution
1590177	Request to add DLL configuration registers in the Libero Initialization Report.	The Design Initialization Report has been updated to include DLL register configurations.
1322248	Request to add argument to the `save_log` TCL command for error, warning and info messages.	Previously, the `save_log` TCL command dumped all log messages (info, warnings, and errors) into the output file. To allow message filtering, additional optional parameters (`-info`, `-warning`, `-error`) have been added, enabling users to select specific message types. This enhancement is backward compatible, as existing scripts continue to work without modification. This change doesn't break the older scripts as the newly added parameters are purely optional.
01593231 01637384	Design Rule Check (DRC) relaxation was requested by customer on MSS I/O Bank2 for CAN interface with 2.5 V to avoid Single-Event Latchup (SEL) concerns with 3.3V MSS I/O voltages on RT PolarFire SoC devices.	DRC has been updated to support 2.5 V for CAN and I2C for all dies (including ES), packages and speed-grade. Additional LVCMOS I/O voltage support has also been added.
811815	PF_IOD: The SDF timing arcs were not correctly generated to support BA simulation for static IODs.	Static timing check arcs for certain reset pins in IOD cell types have been removed from the SDF writer, resolving the issue.
1635458	Issues were observed with the IBIS model generated using Libero SoC v2025.1 version specific to the LVDS ODT model.	IBIS is now exporting data correctly and so, issue has been closed.
860315	Bottleneck analysis results were inconsistent in the Libero v2021.2 version.	Clock domain-based bottleneck reports can now be generated by selecting the clock from the "Set" category. An issue where this filtering did not work correctly has been resolved.
1578386	PF_IOD_OCTAL_DDR core was missing default constraints.	All timing exception constraints can now be generated automatically. External timing constraints (such as `input_delay`, `output_delay`, `max_delay`, and `min_delay`) are not generated, as they depend on user board requirements.
1485133	Anomalies were observed in the PMP set up for PolarFire SoC using MSS Configurator.	The PMP (Physical Memory Protection) view has been updated to address these issues, and correct behavior is now observed.
1475435	An internal error (“Assertion Failed”) occurred after synthesis in a customer design.	The issue has been fixed by skipping the `X_INTERFACE_INFO` attribute when reading the VM netlist.

Table 6-1. Customer-reported Defects and Enhancement Requests with Case Numbers (continued)

Case Number	Summary	Resolution
1614843	Timing exception `set_disable_timing` was not working as expected for the IOD_TX blocks.	An issue with disabling CDC using the `set_disable_timing` constraint has been resolved. When multiple `set_disable_timing` constraints were specified for different cells with the same `-to` and `-from` options, only the first constraint was applied and the others were ignored. This behavior has been corrected.
1606506	Filters did not display all clocks in the Timing Report Explorer.	Timing Report Explorer has been fixed to display all clocks in the clock filtering list for Min report.
1558211	On Linux systems, the operating system was terminating the "mdrg5" and "smartsta" processes during Place & Route (P&R) and when launching SmartTime.	This issue has been addressed by reducing the peak memory consumption of SmartTime. The customer test case exhibited a very high number of logic levels. While memory usage has been reduced, it is still recommended to limit logic depth in designs to avoid excessive memory consumption.
1563635	The TCL command for exporting IBIS files with the "Model Selector" option selected was not available.	An `-msel On|Off` argument has been added to the IBIS export TCL command to enable or disable "Model Selector" export option, resolving the issue.
1556802	False Loss Lock indication was observed incorrectly in the Fabric CCC simulation.	Enhancement has been made in the SF2 Fabric CCC module, specifically in the PLL simulation model lock-loss generation functionality, resolving the issue.
1603020	Additional arguments for Synplify Elite were being ignored.	For Synplify Elite/Premiere, user-provided additional arguments entered in the tool profile dialog box were not being passed to Synplify. This issue has been fixed, and the additional arguments are now passed as expected.
1613338	The I/O couldn't be set to the desired pin in Libero, even though the pin appeared as available in the Constraint Manager and validated by DRC.	For the IOD TX Ratio 5 single-ended data output, the N side of the IOD pair is not available for use. This configuration requires both the P and N sides of the pair due to architectural overlay constraints. The TX_DATA overlay utilizes the IOD N (effectively consuming the F2I ports), rendering the IOD N unusable for other functions, including standard single-ended I/O. This requirement is clarified in Libero SoC v2025.2.
1648692	The "Questasim ScintillaTk" package path was not configured in the Libero v2025.1 release installation.	New installation of QuestaSim has been packaged into Libero 2025.2 which resolves the issue.
1571301	There were issues with PF_IO RX Delay RTL Simulation issue for RX delay taps greater than 125.	Support for narrow and wide mode delays in PF IODs has been provided.
1510223	The Expose fractional clock parallel data was only available with fractional aligned mode, and not in the fractional dynamic mode.	Support has been added for the Expose fractional clock parallel data in the fractional dynamic mode as well.
01628141 01647372	There were issues with the MSS LPDDR4 IBIS model generated using Libero SoC v2025.1 version. Without the "Model Selector" option, models were being exported for both input and output pins of BIDIR (Bidirectional) I/O.	Support has been added to export the model selector for BIDIR I/O's input side as well.

Table 6-1. Customer-reported Defects and Enhancement Requests with Case Numbers (continued)

Case Number	Summary	Resolution
1543687	The "CREATOR" field inside the STP file wrongly displayed FlashPro.	The "CREATOR" field inside the STP file has been updated to display Libero.
01622199 01625354 01652438 01645480 01666373	The Libero SoC Design Suite was ignoring proxy settings on both Windows 10 and 11 systems.	The curl flags have been added to enable HTTPS proxy support, resolving the issue.
1585675	Incorrect message was displayed in the programming log of the G4 devices.	The incorrect message has been removed and the issue resolved.
1616763	SmartDebug displayed PCIe_bridge registers incorrectly.	The issue was caused by duplication of the PCIe bridge registers, which resulted in incorrect addresses being displayed. This has now been resolved, and the duplication has been prevented.
1571939	The generated settings for PolarFire DLL in the PF_CCC configurator were incorrect in the "Phase Generation" mode.	The parameters have been updated in the configurator-generated netlist for the "Phase Generation" mode.
1572135	RX-delay-line RTL simulation showed unexpected variations in effective TAP delays.	The PF IOD simulation model now supports 256 tap delays, increment/decrement by 1 tap delay and each tap provides 25 ps delay.
1637894	The SDF writer incorrectly wrote zero delay for the RTG4 device family.	The SDF writer has been updated to bypass skipped pins and connect to the previous driving cells.
1589373	Post synthesis generated netlist for the Synplify tool was incorrect.	The Synplify tool was incorrectly returning an integer instead of a real value when performing division where the numerator was a real number and the denominator an integer, as defined in the "std.vhd" library. This issue has been fixed in this release.
1556938	SmartDebug was displaying incorrect write-leveling results.	The write-level tap delay value has been fixed by correctly reading the lower significant bits of the register.
01588834 01595754	The relationship between DQS position and delay tap width in MSS DDR differed from that in Fabric DDR.	This issue resulted in a drift towards the left margins in the MSS DDR I/O margin. It has been resolved.

The following table lists the customer-reported defects and enhancement requests resolved in Libero SoC v2025.2 that do not have case numbers. Resolution of previously reported “Known Issues and Limitations” are also noted in this table.

Table 6-2. Customer-reported Defects and Enhancement Requests (No Case Numbers)

Summary	Resolution
MSS_DDR DQS position was not center-aligned for DDR3 and LPDDR3 for passing the DDR training.	The relationship between DQS position and delay tap width in MSS DDR differed from that in Fabric DDR, which resulted in a drift toward the left margins in the MSS DDR I/O Margin. This issue has now been resolved.
Libero GUI crashed when the MegaVault location was changed to /integ/tools/megavault/MegaVault_rr2_lin/.	The crash was caused by invalid syntax in the MegaVault structure. A check has been added to detect syntax issues early and prevent crashes for users.
There was issue with clock halt using Live Probe negative edge.	PolarFire now supports setting negative edge trigger on a Live Probe signal to halt the clocks.
PF_IOD_OCTAL_DDR core version 2.0.109 was failing at synthesis.	The tool now automatically generates all possible exception constraints (false paths).

Table 6-2. Customer-reported Defects and Enhancement Requests (No Case Numbers) (continued)

Summary	Resolution
Synthesizing design with CoreAHBLite was failing.	This issue has been resolved and synthesis passes with "ACP ON" on the Windows machines.
SynplifyPro mapping took 5 hours on simple designs.	This long runtime issue has been resolved and synthesis finishes faster.
For a valid RTL, Synplify incorrectly reported a warning.	This incorrect warning is no longer reported in the Synplify report.
The MPF200T-FCG784E part number should be added to the Silver license.	The license for this part number has been changed to be supported with a Silver license.
Internal assertion failed while running Place & Route.	The issue was caused by recent updates to the timing-cost function and occurred in ECO flows or designs containing many fixed instances. The problem has been resolved, and all designs pass successfully.
Incorrect Operating System information was reported in the `libero_setup_info.txt` file for the newer versions of Windows, like Windows 10 and 11.	A fix has been added to correctly identify the operating system and populate it accordingly.

7. Known Issues and Limitations (Ask a Question)

For information about current known issues and limitations related to the Libero SoC Design Suite, visit Libero SoC Design Suite Release Notes - Known Issues and Limitations.

8. Additional References (Ask a Question)

8.1. Related Release Notes (Ask a Question)

In addition to this release notes, you may find the information in the following release notes helpful.

- PolarFire SoC MSS Configurator v2025.2 Release Notes
- Programming and Debug Tools v2025.2 Release Notes
- SmartHLS Release Notes

8.2. Documents Updated in This Release (Ask a Question)

The Libero documentation is updated frequently. To view the updated information, see Libero SoC Design Suite Help Documentation.

Important: To download a copy for offline use, visit Download Libero SoC Design Suite Help Documentation.

9. Revision History (Ask a Question)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
A	12/2025	Initial Revision

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