Release Notes
Libero SoC v2026.1

Introduction (Ask a Question)

The Libero® SoC Design Suite offers high productivity with its comprehensive, easy-to-learn, easy-to-adopt development tools for designing with Microchip FPGA and SoC device families. It provides you with an integrated hardware tool suite incorporating RTL entry through bitstream programming, a rich IP library, and complete reference designs and development kits. Libero SoC Design Suite includes SmartHLS™ compiler software for abstracted high-level synthesis development flow, which shortens design time, simplifies verification, and accelerates time to market for designs using our FPGAs.

Use Libero SoC v2026.1 for designing with the following Microchip devices:

- RT PolarFire®, RT PolarFire SoC, and RTG4™ Rad-Tolerant FPGAs
- PolarFire SoC and SmartFusion® 2 SoC FPGAs
- PolarFire and IGLOO® 2 FPGAs

To design with older Microchip FPGA family devices, use Libero SoC v11.10 or Libero IDE v9.3 and its subsequent service packs.

To access datasheets, silicon user guides, tutorials, and application notes, visit the Microchip website, navigate to the relevant product family page, and then click the **Documentation** tab. Development kits and boards are listed in the **Kits and Hardware** tab.

Important: Libero SoC v2026.1 does not support Classic Constraint flow. IGLOO2, SmartFusion2, and RTG4 projects using the "Classic" flow cannot be opened in this release. For more information, see Migrating an Existing Project Created with Classic Constraint Flow to Enhanced Constraint Flow.

You can find a comprehensive library of Libero SoC Design Suite Release Notes to explore previous and current release updates.

Download Libero® SoC v2026.1 Software (Ask a Question)

You can download the Libero SoC v2026.1 Design Suite and related software from the FPGA Software Downloads page.

Important: Administrative privileges are required for installing the Libero SoC v2026.1 Design Suite software on the Windows® operating system.

Verify Software Downloads Using MD5 and SHA256 Checksum (Ask a Question)

To verify software downloads using MD5 and SHA256 checksums, use the appropriate procedure for your operating system.

- For Windows operating systems, enter the following at the command prompt: `certutil -hashfile [FILENAME] [HASH]`

- For Linux® operating systems, enter the following command on terminal: `md5sum <path_to_installer>` or `sha256sum <path_to_installer>`

Floating License Daemon Support (Ask a Question)

Microchip now supports 64-bit floating licensing daemons with FlexLM v11.19 for Libero® SoC Design Suite (actlmgrd) that include Synopsys Synplify Pro®/Identify Pro® ME (snpslmd) and Siemens ModelSim/QuestaSim® ME (saltd,which replaces the previous mgcld).

Before opening Libero SoC v2026.1, perform the following procedure to upgrade your systems:

1. Upgrade existing daemons from v11.16 to v11.19. The v11.19 daemons available for downloading appear under the **Daemons Downloads** link on the following Microchip web page: https://www.microchip.com/libero.
2. Install the upgraded license available on your microchipDIRECT account: https://www.microchipdirect.com/fpga-software-products.

This bundle is backward-compatible with all previous Libero SoC releases. Starting with Libero SoC v2024.2, the latest 64-bit license daemons with FlexLM v11.19 are required for all floating license users.

System Requirements (Ask a Question)

This section provides information about supported operating systems, system memory requirements, and other recommendations.

Supported Operating Systems (Ask a Question)

Libero® SoC Design Suite supports the following 64-bit operating systems:

- Microsoft® Windows 11.0
- Red Hat® Enterprise Linux (RHEL) 8.10 and 9.6, AlmaLinux® 8.10 and 9.6
- Ubuntu® 22.04.3 LTS and 24.04.3 LTS

Important:

- Support for Windows 10 has been discontinued in Libero SoC starting with the 2025.1 release.
- Siemens ModelSim Pro does not directly support the Ubuntu platform. However, users can successfully install and run ModelSim Pro and QuestaSim Pro ME on Ubuntu by installing the necessary libraries. Libero provides the script `check_linux_req.sh` to install the required system packages for Ubuntu.
- Libero SoC Design Suite has been tested on x86 and x64 processor-based machines only.
- Libero SoC v2026.1 is the last release to support Siemens ModelSim ME Pro. Beginning with the Libero SoC v2027.1 release, QuestaSim ME Pro will be the only simulator embedded in the Libero SoC Design Suite.

System Memory Recommendations (Ask a Question)

A minimum of 32 GB of Random-Access Memory (RAM) is recommended for implementing designs on MPF500T, MPFS460T, and RT PolarFire® FPGA and SoC devices. For all other devices, a minimum of 16 GB of RAM is recommended.

Table of Contents

1. New in This Version (Ask a Question)

This section contains information about new features, devices, and enhancements introduced in the Libero® v2026.1 Design Suite.

1.1. Changes That Address Important Issues (Ask a Question)

1.1.1. RTG4™ (Ask a Question)

1.1.1.1. System Controller Suspend Mode (SCSM) (Ask a Question)

The Libero® SoC v2026.1 release changes the default setting to "ON" and moves the option to **Project Settings > Device Settings**. It helps align the default configuration with the recommended suspend-mode usage across RTG4™, RT PolarFire®, and RT PolarFire SoC. Pre-existing RTG4 designs that did not employ SCSM will be prompted to enable SCSM when opened in v2026.1, and the user must review the Programming Bitstream options to ensure it meets their required settings.

1.1.1.2. One-Time Programmable (OTP) (Ask a Question)

Libero® SoC v2026.1 introduces additional options for designs employing the OTP option, such as customizing which remaining JTAG actions are permitted with OTP, as well as enabling System Control Suspend Mode (SCSM) and OTP at the same time, with no further JTAG access possible.

You can refer to the Libero SoC Design Flow User Guide and the RTG4™ FPGA System Controller User Guide for more information

1.1.2. RT PolarFire® SoC (Ask a Question)

1.1.2.1. PFSOC_TAMPER (Ask a Question)

Libero® SoC v2026.1 disables the **Fabric Digest Check** option when **Fabric POR Digest Check** is selected for RT PolarFire® SoC devices that do not support it. The GUI now provides guidance for alternative digest-check methods such as external JTAG/SPI VERIFY_DIGEST, system controller Digest Check service followed by device reset, or IAP_VERIFY service.

1.2. New Device Support (Ask a Question)

RT PolarFire® timing data: Updated MIL timing data for the following supported devices from Preliminary to Production for STD and -1 speed grades:

- RTPF500ZT/ZTS/ZTL/ZTLS
- RTPFS160ZT/ZTS/ZTL/ZTLS
- RTPFS460ZT/ZTS/ZTL/ZTLS

1.3. Software Features and Enhancements (Ask a Question)

This section describes new software features and enhancements introduced in the Libero® SoC v2026.1 Design Suite.

1.3.1. Simulator Updates (Ask a Question)

This section describes simulator updates introduced in Libero® SoC v2026.1.

1.3.1.1. Version Upgrades (Ask a Question)

Libero® SoC v2026.1 updates simulator support to **QuestaSim ME Pro 2025.3** and **ModelSim ME Pro 2025.3**, with QuestaSim ME Pro as the default simulator and ModelSim ME Pro available as an optional simulator.

This release also supports Visualizer debug flows. Visualizer is the unified debug environment for QuestaSim and is available as an alternative to the classic simulation debug flow. The Visualizer debug flow uses the `-access`/`-debug` options instead of the legacy `+acc` flow.

The following example shows the basic syntax for running the Visualizer flow:

```
vsim -voptargs="-debug -designfile design.bin" -qwavedb=+signal+memory
```

For more information about the Visualizer, see the documentation available with the QuestaSim installation. You can also refer to the ModelSim_to_QuestaSim_Migration_User_Guide.

1.3.1.2. Simulation Compile Control (Ask a Question)

Simulation flows now allow users to pass custom arguments to `vlog` and `vcom` commands. This enhancement gives users more control over Verilog and VHDL compilation options during simulation.

1.3.2. Remote Programming Server Support for Libero® SoC and FlashPro Express (Ask a Question)

Libero SoC v2026.1 enables **Remote Programming Server** support for Libero SoC and FlashPro Express, allowing users to configure and use programming hardware connected to a remote machine. Existing workstation-mode behavior remains unchanged, while the new remote option provides greater flexibility for shared or centralized programming setups.

1.3.3. Standalone SmartDebug Remote Workflows (Ask a Question)

Libero® SoC v2026.1 enables remote programming and debug workflows in standalone SmartDebug. This support includes remote server connections, programmer management, chain construction and scanning, programming actions, debug features, and multi-client usage.

1.3.4. Netlist Viewer Displays CFG Macro Initialization Strings (Ask a Question)

Libero® SoC v2026.1 enhances the Netlist Viewer to display initialization strings for CFG macros. This update makes it easier for users to inspect configuration macro initialization details during design review and debug.

1.3.5. Tcl Export Flow (Ask a Question)

Libero® SoC v2026.1 improves hierarchical export of component descriptions to Tcl by addressing issues related to HDL folder handling. This update improves reliability when exporting component-description information for hierarchical design flows.

1.3.6. SmartDesign Tcl (Ask a Question)

Libero® SoC v2026.1 improves the `sd_create_pin_group` Tcl command to correctly handle cases where an existing pin-group member is moved to another group. This update improves pin-group management in SmartDesign Tcl flows.

1.3.7. Synplify Pro ME and Identify ME (Ask a Question)

The Libero® SoC v2026.1 release supports the upgraded version, **Y-2026.03M**, of Synplify Pro ME and Identify ME Debugger tools.

1.3.8. Platform OS Updates (Ask a Question)

Libero® SoC v2026.1 extends platform operating system support to **Red Hat Enterprise Linux (RHEL) 9**, **AlmaLinux 9**, and **Ubuntu 24.04**.

1.4. PolarFire®, PolarFire SoC, RT PolarFire, and RT PolarFire SoC (Ask a Question)

This section describes new features and enhancements for PolarFire, PolarFire SoC, RT PolarFire, and RT PolarFire SoC device families in Libero® SoC v2026.1.

1.4.1. Transceiver Simulation Model Enhancements (Ask a Question)

This section describes enhancements to the PolarFire® transceiver simulation model in Libero® SoC v2026.1.

1.4.1.1. PF_XCVR Simulation Model for Fast Lock-Time Simulation (Ask a Question)

Libero® SoC v2026.1 enhances the PolarFire® transceiver simulation model to support fast lock-time simulation behavior. This update helps reduce simulation time while preserving expected transceiver initialization behavior.

1.4.1.2. Independent TX and RX Lanes Support (Ask a Question)

Libero® SoC v2026.1 enables independent TX and RX lane operation in the transceiver simulation model. This enhancement provides greater flexibility for customers simulating transceiver configurations where transmit and receive lanes are used independently.

1.4.2. PF_IOD Post-Layout Simulation (Ask a Question)

Libero® SoC v2026.1 adds post-layout simulation support for statically delayed PolarFire® IOD resources. This support does not apply to dynamically trained PF_IOD interfaces. In this release, only post-layout gate-level functional simulation behavior is supported for the statically delayed PF_IOD resources. The PF_IOD external timing check arcs have been removed to prevent currently unsupported back-annotated timing simulation results through the IOD.

1.4.3. PF_IOD Initial Tap Value Simulation (Ask a Question)

Libero® SoC v2026.1 enables PF_IOD post-layout simulation with startup or initial tap values. This enhancement allows customers to more accurately simulate IOD delay behavior based on configured initial conditions.

1.4.4. PF_IOD_OCTAL_DDR Clock Frequency Display (Ask a Question)

Libero® SoC v2026.1 improves the PF_IOD_OCTAL_DDR configurator by displaying the rounded frequency for the CCC PLL Output 3 clock divider label. This update improves readability and helps users better understand the generated clock configuration.

1.4.5. PF_IOD_GENERIC_RX Data Rate and Fabric Clock Configuration Guidance (Ask a Question)

Libero® SoC v2026.1 enhances PF_IOD_GENERIC_RX configuration guidance for data rate versus fabric clock speed. This update helps customers configure receive interfaces with improved awareness of valid data-rate and fabric-clock relationships.

1.4.6. PF_XCVR Clocking Support (Ask a Question)

Libero® SoC v2026.1 updates the PF_XCVR configurator to support the **Global (shared)** clock option for applicable TX and RX clock configurations where both global and regional clock ports are exposed. This allows supported designs to use the quad's shared global clock output while retaining regional clock outputs for other lane clocks, subject to the device limitation of one global clock output to the fabric per quad.

1.4.7. PF_PCIE UIC Initialization (Ask a Question)

Libero® SoC v2026.1 updates PF_PCIE UIC initialization for PCIe configurations using **-6 dB de-emphasis**. This enhancement improves support for PCIe designs that require this de-emphasis setting.

1.4.8. PF_Crypto AHB Clock Frequency Guidance (Ask a Question)

Libero® SoC v2026.1 updates the PF_Crypto tooltip and parameter-description guidance to clarify the supported AHB clock frequency ranges for embedded DLL configurations. The embedded DLL must be enabled when the AHB clock frequency is greater than or equal to 125 MHz, and disabled when the AHB clock frequency is less than or equal to 70 MHz; AHB clock frequencies greater than 70 MHz and less than 125 MHz are not supported for this configuration.

1.4.9. PF_DDR Warning for Missing I/O Calibration on Memory Interface Banks (Ask a Question)

Libero® SoC v2026.1 now reports a warning when I/O Calibration is not enabled for banks using memory interfaces. This warning helps customers identify potential DDR configuration issues earlier in the design flow.

1.4.10. Periphery Pre-Placement Checks (Ask a Question)

Libero® SoC v2026.1 adds pre-placement checks for PolarFire® IOD resources. This enhancement helps identify IOD placement issues earlier in the design flow and improves implementation predictability for supported designs.

1.4.11. Routability Improvements (Ask a Question)

Libero® SoC v2026.1 improves routability for designs where global signals drive wide-mux structures. This enhancement helps improve routing robustness for applicable PolarFire designs.

1.4.12. Clock Source Validation (Ask a Question)

Libero® SoC v2026.1 adds a Design Rule Check to validate that the IP pin `CLK_FROM_RCOSC_160MHZ` is driven by the RC Oscillator. This check helps users identify invalid clock-source connections early in the design flow.

1.4.13. Silver License Expansion (Ask a Question)

Libero® SoC v2026.1 expands Silver license support for the following PolarFire® device/package combinations:

- MPF300TS-1FCG1152I
- MPF200TC:
  - FCG1152I
  - FCG1152E
  - FCVG484E

1.5. PolarFire® SoC, RT PolarFire SoC (Ask a Question)

This section describes new features and enhancements for PolarFire SoC and RT PolarFire SoC device families in Libero® SoC v2026.1.

1.5.1. MSS DDR Impedance Display in Ohms (Ask a Question)

Libero® SoC v2026.1 now displays the configured MSS DDR impedance value in ohms in the **MSS Impedance (Ohm)** column. This update improves visibility into the selected DDR impedance configuration.

1.5.2. eNVM Configuration (Ask a Question)

Libero® SoC v2026.1 enables users to add a plain-text data client in the eNVM configuration flow. This enhancement provides additional flexibility when configuring eNVM data clients.

1.5.3. PolarFire® SoC Standalone MSS Configurator (Ask a Question)

This section describes new features and enhancements for the PolarFire SoC Standalone MSS Configurator in Libero® SoC v2026.1.

1.5.3.1. PMP Configuration DRCs for Batch Mode (Ask a Question)

Libero® SoC v2026.1 now provides additional Design Rule Checks for PMP and MPU expert mode fields in batch mode to prevent MSS generation for invalid values.

1.5.3.2. MSS DDR Timing Support (Ask a Question)

Libero® SoC v2026.1 updates the MSS DDR configuration flow to account for the `tCCD_L` memory timing parameter. This enhancement improves timing parameter handling for supported MSS DDR configurations.

1.5.3.3. MSS Timing Shell Export with HDL Export (Ask a Question)

Libero® SoC v2026.1 enables export of MSS Timing Shell information when HDL export is enabled. This enhancement ensures timing-related MSS information is available with exported HDL collateral.

1.6. RTG4™ (Ask a Question)

This section describes new features and enhancements for RTG4 devices in Libero® SoC v2026.1.

1.6.1. PROBE_READ_DATA Pin (Ask a Question)

Libero® SoC v2026.1 enables the layout log to print the I/O settings for the PROBE_READ_DATA output pin when selected.

1.6.2. Compressed Bitstream Support for RTG4™ DAT File Generation (Ask a Question)

Libero® SoC v2026.1 enables compressed bitstream support during RTG4 DAT file generation. This enhancement helps reduce generated DAT file size for supported RTG4 programming flows.

2. Migrating Designs to Libero® SoC (Ask a Question)

This section lists core enhancements and upgrades in Libero SoC v2026.1 and provides the procedure to update a core version.

2.1. Core Enhancements and Upgrades (Ask a Question)

The following table lists core enhancements and upgrades in Libero® SoC v2026.1.

Core	2026.1 Version	Status	Comments
PF_CRYPTO	1.0.111	Production	Updated tooltip and parameter-description guidance for AHB clock frequency requirements. See the PF_Crypto AHB Clock Frequency Guidance section for more details.
PF_IOD_GENERIC_RX	2.1.117	Production	Enhanced PF_IOD_GENERIC_RX configuration guidance for data rate versus fabric clock speed. See the PF_IOD_GENERIC_RX Data Rate and Fabric Clock Configuration Guidance section for more details.
PF_RGMII_TO_GMII	1.3.112	Production	Repackaged to include the latest PF_IOD_GENERIC_RX version.
PFSOC_TAMPER	2.0.101	Production	Disabled unsupported Fabric Digest Check option for RT PolarFire® SoC devices. See the PFSOC_TAMPER section for more information.

2.2. Updating a Core Version (Ask a Question)

1. Download the latest version of the core into your vault.
2. Upgrade each configured core in your design to the latest version by right-clicking the core component in the design hierarchy and selecting **Update Component Version**. The component is regenerated automatically.

   Important: The Update Component Version option is now available on instances of core components in a SmartDesign canvas as well. In addition, the selected core version is downloaded automatically from the Update Component Version dialog itself if needed.

3. Review the SmartDesign components and user RTL files in which the core component has been instantiated. If the port-list is modified after updating, right-click the core component's instance in the SmartDesign and select **Update Instance**. Check for any pin/port disconnections and connect or tie them off as needed, then regenerate the SmartDesign component.
4. Build Design Hierarchy and Derive the Timing Constraints again from the Constraint Manager tool to use the latest generated core timing constraints.
5. Rerun the design flow.

3. Resolved Issues (Ask a Question)

The following table lists the customer-reported defects and enhancement requests resolved in Libero® SoC v2026.1 that have case numbers. Resolution of previously reported “Known Issues and Limitations” are also noted in this table.

Table 3-1. Customer-reported Defects and Enhancement Requests with Case Numbers

Case Number	Summary	Resolution
01548618	Support was requested for newer Ubuntu versions with Libero® SoC.	The following Ubuntu versions are now supported with Libero: • 22.04.3 LTS • 24.04.3 LTS See the Platform OS Updates section for more information.
01551651	CFG macro INIT strings were not visible in the Netlist Viewer.	The Netlist Viewer has been updated to display INIT strings for CFG macro instances. Users can now right-click a CFG macro and select "Get Init Params" to view the macro’s INIT string. See the Netlist Viewer Displays CFG Macro Initialization Strings section for more information.
01552158	Synthesis failed with error: “Couldn't find binding for variable p”.	This compile error has been resolved and synthesis now passes successfully.
01566000	An internal error occurred in `c_vhdl.exe` of the Synthesis tool.	The crash has been resolved. The synthesis tool now reports appropriate error messages.
01605468	Incorrect feedback mux removal messaging was reported during synthesis optimization.	The incorrect “CL282” message has been corrected to report the appropriate synthesis message.
01634664, 01631506	Error and warning codes had inconsistent descriptions in OEM_Message_Reference documentation.	The documentation has been updated to correct the descriptions for warning codes “CG238” and “CG100”.
01638904, 01637345	Help documentation for the `syn_redhardlevel` attribute limitation was missing.	Help documentation has been updated to include the `syn_redhardlevel` attribute limitation.
1590754.0	An m_generic issue was observed with the Synplify Pro version bundled with Libero SoC v2024.2.	The crash has been fixed, and the COREAXI4INTERCONNECT IP core has been updated to resolve the RTL errors. Synthesis now passes successfully.
01596808, 01604528	Support was requested for Ubuntu 24.04 including running the PolarFire® SoC MSS Configurator on the latest Ubuntu versions, as Ubuntu 20.04 was approaching end of support.	Ubuntu 24.04.3 LTS is now supported with Libero SoC and PF Studio, with required runtime dependencies installed using the provided `check_linux_req.sh` script. MSS generation has been verified in both GUI and batch mode for standalone MSS and MSS from Libero. See section Platform OS Updates section for more information.
01626076	Updates were requested for I/O standard and drive-strength handling on reserved pins for RTG4™ devices.	The layout log now prints the I/O settings for the reserved PROBE_READ_DATA output pin when selected. For more information, see the PROBE_READ_DATA Pin section.
01660477	The I/O Editor displayed drive impedance values in milliamps instead of ohms.	The configured MSS DDR impedance value is now displayed in ohms in the new MSS Impedance (Ohm) column, correctly distinguishing impedance (ohms) from output drive (mA). See the MSS DDR Impedance Display in Ohms section.
01768254	The Device Selection table did not show 24 transceiver lanes for RTPFS460ZT/ZTS/ZTL/ZTLS devices.	The Device Selection table under "Project Settings" has been corrected to show 24 transceiver lanes for all RTPFS460ZT/ZTS/ZTL/ZTLS devices in the CG1509 and FC1509 packages. This change updates the displayed lane count only and has no impact on any design flow.

Table 3-1. Customer-reported Defects and Enhancement Requests with Case Numbers (continued)

Case Number	Summary	Resolution
01650912	“Undo” behavior was inconsistent in Libero SoC.	The "Undo" and "Redo" behaviors have been corrected to operate consistently in the Libero SoC text editor.
01656398	PF_IOD_GENERIC_RX calculated I/O clock speed and fabric clock speed incorrectly when the data rate was entered as a whole number without a decimal point.	The PF_IOD_GENERIC_RX configurator has been updated to handle data-rate values consistently whether they are entered with or without a decimal point. For more information, see the PF_IOD_GENERIC_RX Data Rate and Fabric Clock Configuration Guidance section.
01674213	DDR4 memory training time reported in SmartDebug differed from the actual measured training time.	SmartDebug DDR4 memory training-time reporting has been corrected to use the user (fabric) clock as the reference instead of the memory clock, aligning the reported training time with the actual measured value.
01749194	An issue was observed with PolarFire SmartDebug Eye Monitor.	SmartDebug behavior for Signal Integrity (SI) settings in the Eye Monitor has been clarified. Because SI settings cannot be read back from the device, SmartDebug loads either the user-configured settings or the settings modified in the previous session, and a pop-up message now informs the user of this behavior when a modified lane is selected.
01687724	RTG4 programming options required updates in the tool UI and Tcl command flow	System Controller Suspend Mode is now available as a project setting. The Programming Bitstream Options UI and related Tcl command have been updated accordingly. For more information, see the System Controller Suspend Mode (SCSM) and One-Time Programmable (OTP) sections.
01695557	A bitstream generation message was requested for the RTG4 System Controller Suspend Mode enhancement.	Bitstream generation now displays a warning when System Controller Suspend Mode is disabled, helping users confirm the setting before generating programming files. For more information, see the System Controller Suspend Mode (SCSM) section.
01690337	MSS DDR Debug DQ/DQS optimization displayed incorrect stage results and parameters.	The MSS DDR Debug pass/fail determination has been corrected to use the appropriate training-status registers, so DQ/DQS optimization stage results and parameters are now reported correctly.
01700330	SmartDebug tool crashed on Ubuntu 22.04.	The SmartDebug crash on Ubuntu has been resolved. The tool now launches and operates correctly when used with the Embedded FlashPro programmer on Ubuntu
01690844	The Parameter Report displayed an empty instance name when multiple top modules existed.	The Parameter Report generation has been corrected so that an empty instance-name entry is no longer produced when multiple top modules are present in the project.
01695547	Libero Build Hierarchy could hang when a VHDL function type mismatch was present.	Libero now reports the VHDL error instead of hanging during Build Hierarchy when a VHDL function type mismatch (for example, mixing real and integer types) is present.
01708923	HDL core recognition was inconsistent in the Libero SoC design hierarchy.	HDL core recognition has been corrected. A parameterized module added via a Tcl script (using create_links) and converted to an HDL+ core is now consistently recognized as an HDL+ core in the Design Hierarchy and instantiated correctly in SmartDesign.

Table 3-1. Customer-reported Defects and Enhancement Requests with Case Numbers (continued)

Case Number	Summary	Resolution
01718510, 01734432	Support was requested for adding a plain-text data client in eNVM as well as data client in eNVM concurrent with Boot Mode-2 client in sNVM.	Plain-text data client support has been added in eNVM. For more information, See the eNVM Configuration section.
01736313	HDL+ incorrectly generated parameters when a SystemVerilog import statement was present with MiV_RV32.	HDL+ parameter extraction has been updated to import only parameters explicitly imported in the source file. Parameter extraction now supports wildcard imports and extracts only explicitly specified parameters for named imports.
01742180	Place-and-route failed for an RTPF TSN design involving global signals driving wide mux structures.	Routability has been improved for designs where global signals drive wide-mux structures, reducing routing conflicts and allowing the affected design to complete place-and-route. See the Routability Improvements section.
1646619	Enhancement was requested for the PF_Crypto core configurator.	The PF_Crypto tooltip and parameter-description guidance have been updated to clarify the supported AHB clock frequency ranges. The embedded DLL must be enabled for AHB clock frequency ≥ 125 MHz and disabled for ≤ 70 MHz. Frequencies between 70 MHz and 125 MHz are not supported. The fix is available in PF_CRYPTO 1.0.111. See the PF_Crypto AHB Clock Frequency Guidance section for more details.
811815	PF_IOD back-annotated simulation included external timing checks on IOG/LANECTRL for dynamic IOD configurations without external timing check arcs.	IOD/LANECTRL external check arcs are filtered out from the back-annotated SDF. This update is part of PF_IOD back-annotated functional simulation support.
1669714.0	QuestaSim 2024.3 in Libero SoC v2025.1 experienced a 120-second startup delay in air-gapped environments.	The QuestaSim startup behavior has been improved to avoid the observed delay in air-gapped environments.

Table 3-2. Customer-reported Defects and Enhancement Requests (No Case Numbers)

Summary	Resolution
The default value of the PFSoC MSS `BFM_SELECT` parameter required an update.	The default value of the PFSoC MSS `BFM_SELECT` parameter has been updated from `1` to `0`.
QuestaSim experienced a startup delay in air-gapped environments.	The QuestaSim startup behavior has been improved to avoid the observed delay in air-gapped environments.
IBIS output contained zero RLC values for selected RTPFS460ZTL/FC1509/MIL and MPF300XT configurations.	IBIS model generation has been corrected to generate valid RLC values for the affected device/package configurations.
MSS I/O IBIS generation reported an unknown model error for an LVCMOS25 configuration.	MSS I/O IBIS model generation has been corrected so the affected LVCMOS25 model is generated and referenced properly.
Some models were missing in PFSoC IBIS generation runs.	PFSoC IBIS generation has been updated to export the required models in generated IBIS files.
Additional guidance was needed because UL_DEBUG Lock does not block debug through the exposed MSS JTAG fabric interface.	An informational message has been added to clarify debug access behavior when UL_DEBUG Lock is used with the exposed MSS JTAG fabric interface.
Enhancements were requested for the SPI Configurator.	The SPI Configurator has been enhanced to improve supported configuration workflows.
System Controller Suspend Mode required additional changes and enhancements.	System Controller Suspend Mode handling has been updated with additional logs, warnings, and improved UI. For more information, see the System Controller Suspend Mode (SCSM) and One-Time Programmable (OTP) sections.
Probe settings in the Configure Programming Options dialog could not be changed after constraints probe settings were applied.	Probe settings handling has been corrected so programming option changes can be applied as expected.

Table 3-2. Customer-reported Defects and Enhancement Requests (No Case Numbers) (continued)

Summary	Resolution
Changes made to IOPADP_IN and IOPADN_IN in the previous release required correction.	The SDF was updated to move the IOPADN_IN arc delay to IOPADP_IN.
Physical Memory Protection configuration in PFSoC MSS was missing required DRC checks.	Additional DRC checks have been added to validate Physical Memory Protection configuration settings. For more information, see the PMP Configuration DRCs for Batch Mode section.
SmartDebug SI setting changes were not retained after applying user-configured values and importing a PDC file.	SmartDebug SI settings handling has been corrected so modified values are retained after applying settings and importing PDC files.
Libero® crashed when viewing or exporting the memory map.	Memory map view and export handling has been corrected to prevent the crash.
Block flow compile could fail for designs with long instance, net, or port names.	Libero SoC v2026.1 increases name-length handling in block flow, including support for port names up to 1024 characters, preventing compile crashes for affected RTG4™, PolarFire®, and PolarFire SoC designs.
During JTAG programming for PolarFire SoC/PFSoC devices, the configured I/O state for some pins could be applied incorrectly. For example, pin G17 could remain at logic 1 even when configured to logic 0.	The I/O State configuration file has been corrected to fix the BSR pin order for PFSoC devices, ensuring configured I/O states are applied correctly during programming.

4. Known Issues and Limitations (Ask a Question)

For information about current known issues and limitations related to the Libero® SoC Design Suite, visit Libero SoC Design Suite Release Notes - Known Issues and Limitations.

5. Additional References (Ask a Question)

This section provides additional reference materials related to Libero® SoC v2026.1.

5.1. Related Release Notes (Ask a Question)

In addition to this release notes, you may find the information in the following release notes helpful:

- PolarFire® SoC MSS Configurator v2026.1 Release Notes
- Programming and Debug Tools v2026.1 Release Notes
- SmartHLS™ 2026.1 Release Notes

5.2. Documents Updated in This Release (Ask a Question)

The Libero® documentation is updated regularly. To view the updated information, see Libero SoC Design Suite Help Documentation.

Important: To download a copy for offline use, click Download Libero SoC Design Suite Help Documentation.

6. Revision History (Ask a Question)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
B	07/2026	The following changes are made in this revision: • Applied readability improvements throughout the document. • Added the PF_IOD post-layout simulation update in the PolarFire, PolarFire SoC, RT PolarFire, and RT PolarFire SoC section. • Updated the important note in the Supported Operating Systems section.
A	07/2026	Initial Revision

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