PolarFire SoC MSS Configurator User Guide

Libero SoC v2026.1

Introduction (Ask a Question)

The PolarFire® SoC Microcontroller Subsystem (MSS) Configurator provides a graphical user interface that allows embedded software engineers to define the MSS start-up state quickly. It exports an XML file that is used by the embedded software flow that converts the XML into initialization constructs. Additionally, the tool outputs a CXZ file for inclusion into your Libero® design flow. The CXZ file contains information about metadata and port needed by the FPGA designer to complete the MSS and FPGA fabric connectivity.

MSS configurator is available as a stand-alone application and as part of the Libero SoC design tool suite. The information in this user guide applies to both.

Important: Older versions of this documentation uses the terms "Master" and "Slave." The equivalent Microchip terminology used in this document is "Initiator" and "Target" respectively.

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1. Installing the PolarFire SoC MSS Configurator (Ask a Question)

The PolarFire SoC MSS Configurator bundled with Libero is available at the following location in the Libero installation section:

- `Windows: <$Installation_Directory>\Microsemi\Libero_SoC_vX.X\Designer\bin64\pfsoc_mss.exe`
- `Linux: <$Installation_Directory>\Microsemi\Libero_SoC_vX.X\bin64\pfsoc_mss`

The PolarFire SoC MSS Configurator can also be installed as a stand-alone application.

For more information about how to install Libero, see Libero SoC v12.0 and later.

1.1. Input and Output Files (Ask a Question)

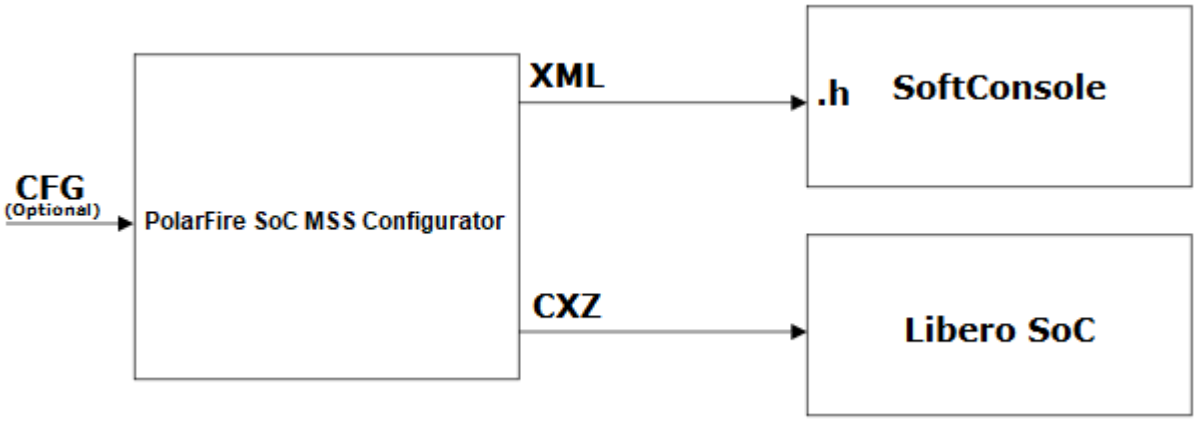
The following sections describe the PolarFire SoC MSS Configurator input and output files.

1.1.1. Output Files (Ask a Question)

The PolarFire SoC MSS Configurator generates the output file formats as shown in the following figure.

- **XML Configuration File**: Contains the MSS memory map, clock, DDR memory controller, and peripheral configuration. The XML file is used to generate hardware files required for building the firmware project.
- **CXZ File**: Encapsulates the hardware design of the MSS block and can be imported into Libero SoC project.

Figure 1-1. PolarFire SoC MSS Configurator Block Diagram



1.1.2. Input files (Ask a Question)

The PolarFire SoC MSS Configurator can be invoked without any input files. A configuration file `(.cfg)` from an earlier MSS configurator session can be optionally provided to the PolarFire SoC MSS Configurator.

Note: A `.cfg` file and a report file can also be generated from the PolarFire SoC MSS Configurator.

2. Running the PolarFire SoC MSS Configurator (Ask a Question)

You can run the PolarFire SoC MSS Configurator in Batch mode or Interactive mode. This chapter describes the following sections:

- Batch Mode
- Interactive Mode
- Using the PolarFire SoC MSS Configurator GUI

2.1. Batch Mode (Ask a Question)

The PolarFire SoC MSS Configurator application can be executed in the Batch mode for scripted execution as follows:

- Windows®:

```
<Libero SoC or Standalone MSS Configurator installation area>\bin64\pfsoc_mss.exe
-GENERATE -CONFIGURATION_FILE:<absolute or relative path for configuration file name
(.cfg)> -OUTPUT_DIR:<absolute or relative path for output directory> -EXPORT_HDL:<true/
false> -LOGFILE:<absolute or relative path for logfile file name>
```

  `-EXPORT_HDL` and `-LOGFILE` are optional arguments.

- Linux®:

```
<Libero SoC or Standalone MSS Configurator installation area>/bin64/pfsoc_mss.exe
-GENERATE -CONFIGURATION_FILE:<absolute or relative path for configuration file name
(.cfg)> -OUTPUT_DIR:<absolute or relative path for output directory> -EXPORT_HDL:<true/
false> -LOGFILE:<absolute or relative path for logfile file name>
```

  `-EXPORT_HDL` and `-LOGFILE` are optional arguments.

2.2. Interactive Mode (Ask a Question)

The Interactive (GUI) mode in the PolarFire SoC MSS Configurator provides the following high-level options.

Table 2-1. Configurator-Project Menu Options

Option	Description
New	Starts configuring a new MSS subsystem.
Open	Opens a configuration (`.cfg`) file.
Save/Save As	Saves the current configuration of the MSS subsystem to a configuration (`.cfg`) file.
Generate	Generates MSS configuration (`.xml`) and component (`.cxz`) files after configuring the MSS subsystem.
Close	Closes the current configuration (`.cfg`) file.

PolarFire SoC MSS Configurator can also be invoked in GUI mode for a specific configuration file as follows:

- Windows:

```
<Libero SoC or Standalone MSS Configurator installation area>\bin64\pfsoc_mss.exe
-CONFIGURATION_FILE:<absolute or relative path for configuration file name (.cfg)>
-OUTPUT_DIR:<absolute or relative path for output directory>
```

- Linux:

```
<Libero SoC or Standalone MSS Configurator installation area>/bin64/pfsoc_mss.exe
-CONFIGURATION_FILE:<absolute or relative path for configuration file name (.cfg)>
-OUTPUT_DIR:<absolute or relative path for output directory>
```

Important: `-OUTPUT_DIR` is an optional argument in GUI mode. If specified, the default output directory location in GUI will always point to the specified location.

2.3. Using the PolarFire SoC MSS Configurator GUI (Ask a Question)

The PolarFire SoC MSS Configurator GUI has the following tabs.

- Peripherals
- DDR Memory
- DDR Memory Partition
- Crypto
- L2 Cache
- MSS To/From Fabric Interface Controllers
- Clocks
- MSS I/O Attributes
- Physical Memory Protection
- Misc

2.3.1. Peripherals (Ask a Question)

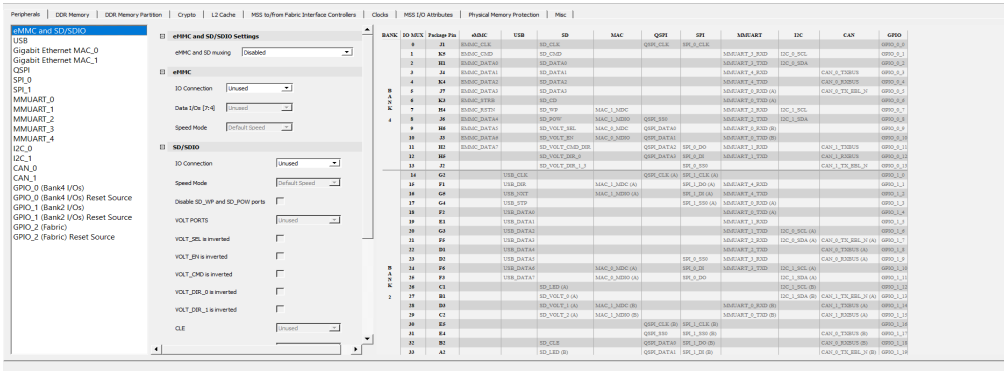
Select the following I/Os using the **Peripherals** tab:

- GPIOs from Bank 2 and Bank 4, which are dedicated to the MSS.
- Fabric I/Os, if the dedicated I/Os from Bank 2 and Bank 4 are not available.
- GPIOs from Bank 5 are dedicated to SGMII but can be routed to GMII or MII fabric I/Os. GPIO from Bank 5 are displayed only when Gigabit Ethernet MAC_0 or Gigabit Ethernet MAC_1 is selected.

Important: I/Os from the DDR bank are dedicated to the DDR Controller in the MSS.

For more information, see the PolarFire SoC MSS Technical Reference Manual. The following figure shows the **Peripherals** tab on the PolarFire SoC MSS Configurator.

Figure 2-1. Peripherals Tab



By default, all peripherals are marked as **Unused**. To include peripherals that are required in the design, select the peripheral from the left-hand side of the window and use the corresponding drop-down to assign MSS I/Os or fabric I/Os.

The I/Os associated with the following peripherals are dedicated and cannot be assigned to fabric I/Os:

- USB peripherals are dedicated in Bank 2.
- eMMC peripherals are dedicated in Bank 4.
- Ports SD_POW and SD_WP can be disabled when not in use and can be used for other interfaces.
- SD/SDIO peripherals are dedicated in Bank 4.

The GPIOs in Bank 2 and Bank 4 have the following options:

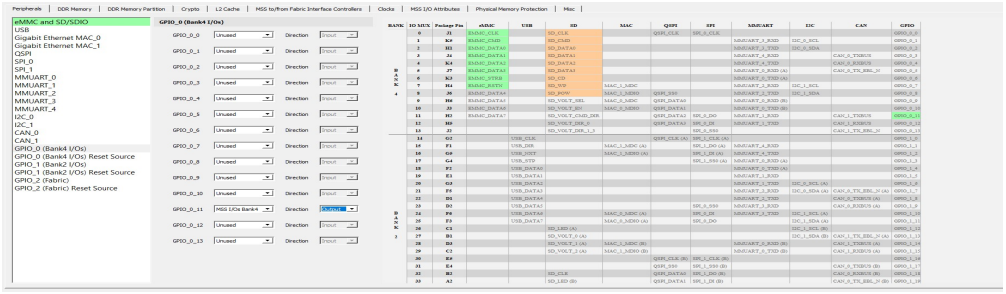
- Unused
- MSS I/Os Bank2/4
- Static High
- Static Low

Important:

- **Static High** and **Static Low** can only be set when **eMMC and SD muxing** is enabled.
- **GPIO_2 (Fabric)** does not support **Static High** and **Static Low** options.

According to the options selected, the affected GPIOs are highlighted in green, as shown in the following figure.

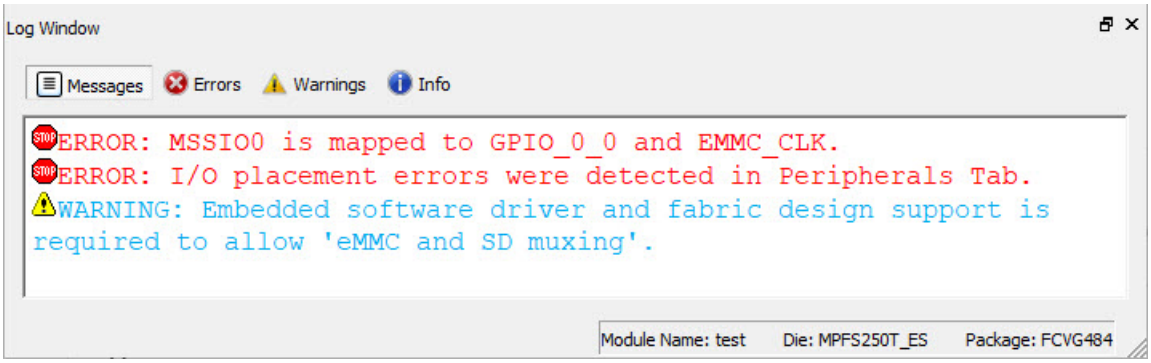
Figure 2-2. GPIO Options



Note: If the I/Os for a peripheral are selected in a bank, you cannot select the same I/Os for another peripheral from the same bank. If you try, the tool generates the following error message in the log window:

```
I/O placement errors were detected in Peripherals Tab.
```

Figure 2-3. I/O Placement Error Message in Log Window



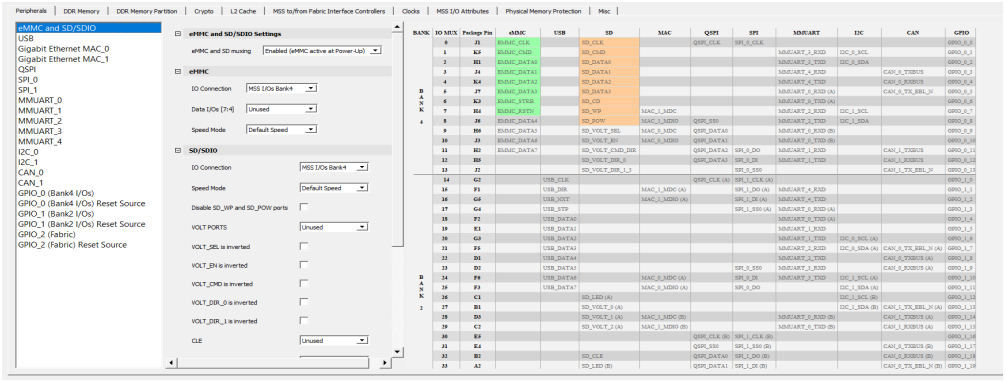
You can choose to enable either eMMC or SD at power-up using the eMMC and SD muxing option. The highlighted green-colored ports denote which I/O setting is active, whereas the orange-colored ports indicate which I/O setting is inactive.

The following warning message is generated in the log window, when the eMMC or SD setting is enabled.

```
Embedded software driver and fabric design support is required to allow 'eMMC and SD muxing'.
```

The eMMC and SD cannot be used simultaneously, as shown in the following figure.

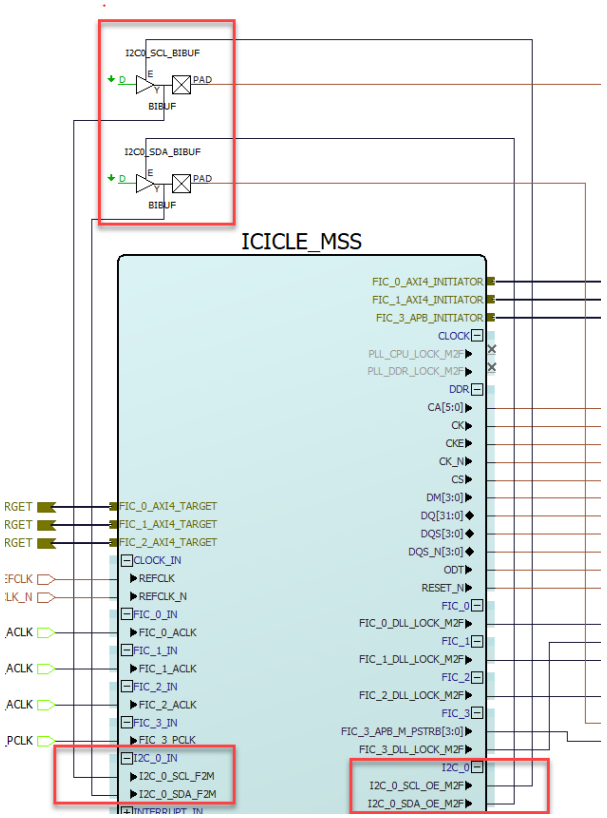
Figure 2-4. Overlapping I/O Warning



2.3.1.1. I2C Port Configuration for Fabric I/O (Ask a Question)

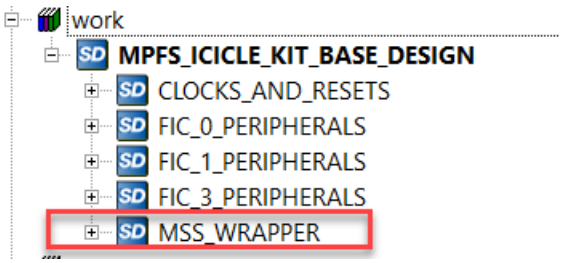
Fabric connections for the MSS I2C peripherals do not generate an output port, instead only an Output Enable (OE) port is available on the MSS component. You must instantiate an BIBUF with the D connected to 'GND' and the E and Y pins connected to OE and IN, respectively. The following figure shows these connections.

Figure 2-5. Fabric Connections



To see the BIBUF configuration required to use the I2C peripheral with fabric connections, see the PolarFire SoC Icicle Kit Reference Design from **MSS_WRAPPER subsystem** > **SmartDesign** .

Figure 2-6. MPFS Icicle Kit Base Design Hierarchy



2.3.2. DDR Memory (Ask a Question)

This section describes the options available in the **MSS Configurator** > **DDR Memory** tab for configuring MSS DDR Controller. For information about the architecture and functional blocks of MSS DDR Controller, see PolarFire SoC MSS Technical Reference Manual.

The following table lists the available options on the **DDR Memory** tab.

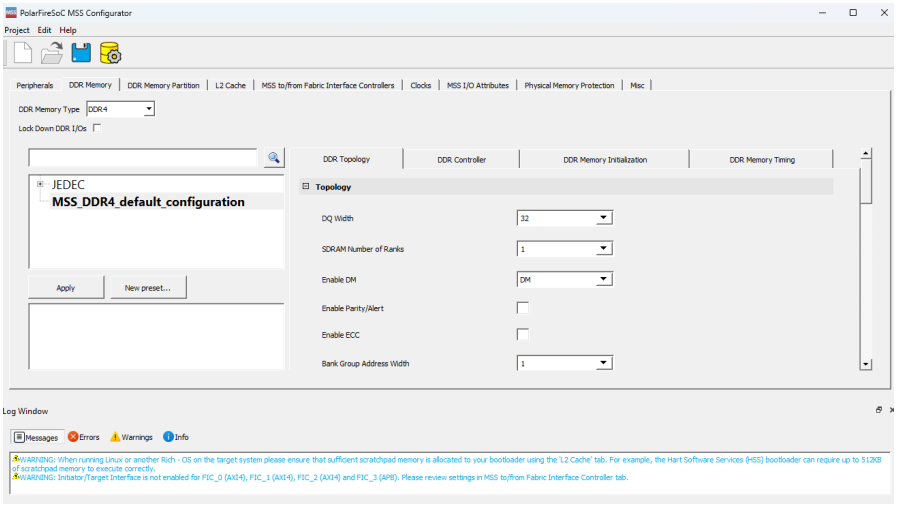
Table 2-2. DDR Memory Tab

Option	Description
DDR Memory Type	Allows selection of the required DDR type from the pull-down. The following memory types are available: • UNUSED • DDR3 • DDR3L • DDR4 • LPDDR3 • LPDDR4 Based on the **DDR Memory Type** selection, the DDR configuration options available on the **DDR Topology**, **DDR Controller**, **DDR Memory Initialization**, and **DDR Memory Timing** tabs vary. All DDR parameters must be configured according to the data sheet from the DDR vendor.
Lock Down DDR I/Os	Locks all DDR-related I/O pins after configuration and prevents them from being reassigned to fabric logic or reconfigured by software after boot.
JEDEC Presets	Pre-defined DDR configuration profiles provided in the MSS Configurator that automatically populate DDR parameters according to the JEDEC standard defaults for a selected memory type and speed grade. Changing the DDR memory type resets the available JEDEC presets.

DDR Topology

The **DDR Topology** tab controls the physical aspects of the memory, such as data and address widths, enabling of ECC and DM, and setting the clock frequency. The following image shows the **DDR Topology** tab when **DDR4** memory type is selected.

Figure 2-7. DDR Topology Tab



The following table lists the available options on the **DDR Topology** tab.

Table 2-3. DDR Topology

Option	Description
DQ Width	Specifies the total data bus width of the DDR interface between the MSS DDR controller and the external memory devices. Supported values for all memory types are 16 and 32 bits. The default selection is 32 bits.
SDRAM Number of Ranks	Specifies how many independent SDRAM ranks are connected to the MSS DDR controller. A rank is a group of memory devices (logical memory array) that operate in parallel and share the data (DQ) and address buses, but are selected using a separate Chip Select (CS#) signal. Single (1) and dual (2) rank options are available. By default, single rank is selected. This option is not available for LPDDR3 and LPDDR4 memory types, where only single rank is used.

Table 2-3. DDR Topology (continued)

Option	Description
Enable DM	Controls whether Data Mask (DM) signals are used on the DDR interface. DM pins allow the DDR controller to selectively mask (disable) individual byte lanes during write operations. Enabling DM is recommended when using the DDR3, DDR3L, and DDR4 memory types and for general-purpose systems and cached memory usages. By default, this option is enabled.
Enable Parity/ Alert	This option is available only for DDR4 memory type. When selected, this option enables Command and Address (CA) parity checking on the DDR interface and activates the ALERT_n signal used by the SDRAM device to report parity errors and certain fault conditions.
Enable ECC	Enables Error Correcting Code (ECC) protection on the MSS DDR memory interface. When enabled, the MSS DDR controller implements Single-Error Correction, Double-Error Detection (SECDED) on data stored in external DDR memory. ECC is implemented as 4 ECC bits per 32-bit data, resulting in the following DDR bus widths: • x16 data → x18 total • x32 data → x36 total When ECC is enabled, additional DQ_ECC pins are exposed which must be physically connected on the board. This option is available only for DDR, DDR3L, and DDR4 memory types. When ECC is enabled, DM must be disabled.
Bank Group Address Width	Defines the number of bank-group address bits used by the DDR controller when accessing external SDRAM. This setting is only applicable to DDR4 memories and must match the organization of the DDR4 device used on the board. Supported values are 1 bit (2 bank groups) and 2 bits (4 bank groups). By default, 1 is selected.
Number of Clock Outputs	Specifies how many differential DDR clock pairs (CK/CK#) the MSS DDR controller drives to the external SDRAM devices. This must match how the DDR clock is physically routed on the board and how many memory devices or ranks require a clock. This option is available for DDR3, DDR3L, and DDR4 memory types and only when dual rank is selected.
Memory Format	Describes the physical form factor and interconnection style of the DDR memory attached to the MSS DDR controller. The following memory formats are supported: • COMPONENT • UDIMM • RDIMM • LRDIMM • SODIMM For DDR3, DDR3L and DDR4, the COMPONENT, UDIMM, RDIMM, LRDIMM, and SODIMM memory formats are supported. For LPDDR3 and LPDDR4, only the COMPONENT memory format is supported.
Enable address mirroring on odd ranks	Enables the MSS DDR controller to internally swap certain address and bank bits when accessing odd-numbered ranks (Rank 1, Rank 3, and so on). This compensates for a physical wiring convention used on multi-rank DDR DIMMs, where the DRAM devices on odd ranks have some address pins intentionally crossed (mirrored). This option is available only for DDR3, DDR3L, and DDR4 memory types when two or more ranks are used and the memory format configured is other than COMPONENT.
Row Address Width	Defines the number of row address bits the MSS DDR controller uses when accessing the external DDR memory. This value must match the value specified in the DDR memory device datasheet. The supported values are 12–16 (both inclusive).
Column Address Width	Defines how many column address bits the MSS DDR controller uses to select a column within an open row and bank in the DDR memory. This value must match the value specified in the DDR memory device datasheet. The supported values are 9–12 (both inclusive).
Bank Address Width	Defines how many address bits are used to select a bank (or bank group) inside the DDR memory device. This value is not editable and is derived from the DDR memory device datasheet. The supported values are as follows: • 2 for DDR3, DDR3L, LPDDR3, and LPDDR4 memory types • 3 for DDR4

Table 2-3. DDR Topology (continued)

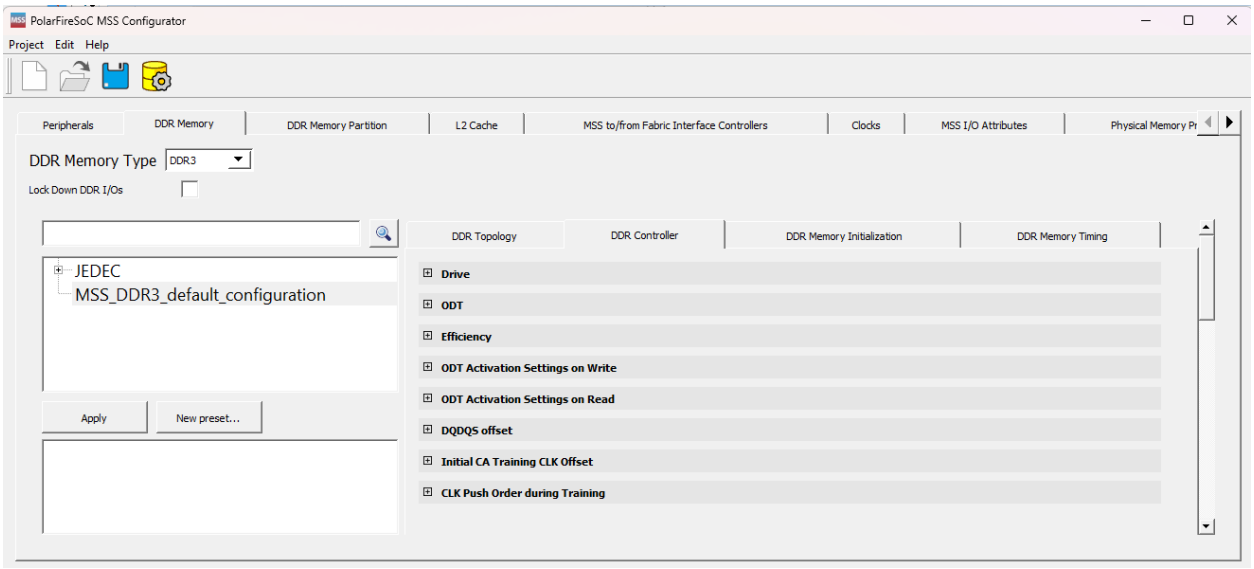
Option	Description
Memory Clock Frequency (MHz)	Specifies the external DDR clock rate (CK/CK#) driven by the MSS DDR controller to the memory device. This value affects every DDR timing calculations. This value can be determined by considering the DDR memory device datasheet and fabric timing or clocking constraints. Note that the clock frequency is different from data rate. The following table lists the supported ranges.

Memory Type	Supported Values	Default Value
DDR3	~300–800 MHz	666
DDR3L	~300–800 MHz	666
DDR4	~400–1200 MHz	800
LPDDR3	~400–800 MHz	666
LPDDR4	~800–1600 MHz	800

DDR Controller

The following image shows the **DDR Controller** tab.

Figure 2-8. DDR Controller



The following table lists the available options on the **DDR Controller** tab.

Table 2-4. DDR Controller

Option	Description
Drive	Drive settings control the output driver strength of the MSS DDR PHY pins. The values are presented in Ohms. The default and supported values vary for each memory type. The following settings are available: • DQ Drive: Specifies the write data strength. • DQS Drive: Specifies the write strobe strength. • ADD/CMD Drive: Specifies the address and command strength. • Clock Drive: Specifies the DDR clock strength.
ODT	On-Die Termination (ODT) for DQ and DQS signals. The values are presented in Ohms. The default and supported values vary for each memory type. The following settings are available: • DQ ODT: ODT for data signals. ODT is always enabled on the receiving side of the DQ bus. • DQS ODT: ODT for data strobe signals. Similar to DQ, termination is enabled on the receiving side.

Table 2-4. DDR Controller (continued)

Option	Description
Efficiency	Efficiency settings control the internal command scheduler of the DDR controller. They aim to reduce wasted cycles caused by unnecessary precharges, repeated row activations, and poor bank utilization. The following settings are available: • Enable Activate/Precharge Look-Ahead: When enabled, the DDR controller looks ahead at pending memory requests and decides whether to keep a row open or precharge early to prepare for the next access. By default, this option is disabled. • Address Ordering: Controls how system addresses are mapped to DDR field. The following options are available: – Chip-Bank-Row-Col – Chip-Row-Bank-Col (default)
ODT Activation Settings on Write/Read	These settings define which ODT pin(s) are asserted during write/read operations, per rank. In PolarFire SoC DDR, up to two ODT (ODT0 and ODT1) pins are supported. Each rank can be wired to ODT0, ODT1, or both. These options tell the controller which ranks enable ODT and when (note that ODT must be enabled on the receiving side to absorb reflections). These options are available only for DDR3, DDR3L, DDR4, and LPDDR3 memory types.
DQDQS Offset	DQDQS start training window offset: This option controls where the DDR controller begins searching for the valid timing window between DQ (data) and DQS (data strobe) during DQ–DQS training (read and/or write leveling). Values between 1–10 are supported. By default, this value is set to 1.
Reference Voltage	Reference Voltage (Vref) is the threshold voltage used by DDR receivers to decide whether a signal is a logic 0 or 1.These settings are available only for DDR4 and LPDDR4 memory types. The following settings are available: • Vref CA (as % of bank VDDI): Reference voltage used by the DRAM to sample the Command/Address (CA) signals, expressed as a percentage of the DDR I/O bank supply voltage (VDDI). • Vref data (as % of bank VDDI): Reference voltage used by the DRAM to sample the data signals, expressed as a percentage of the DDR I/O bank supply voltage (VDDI).
Initial CA Training CLK Offset	This setting defines the initial phase offset applied to the DDR clock when the controller starts CA (Command/Address) training. The following settings are available: • Advanced CA training: Select this option to enable the CA training offset. • Number of offsets: Specifies the required number of offsets. Up to 4 offsets can be enabled. • Offset 0–Offset 3: Specifies the clock-phase offset value in degrees.
CLK Push Order during Training	Specifies the order in which clock phase shifts are applied (pushed) during DDR training, mainly affecting CA clock training.

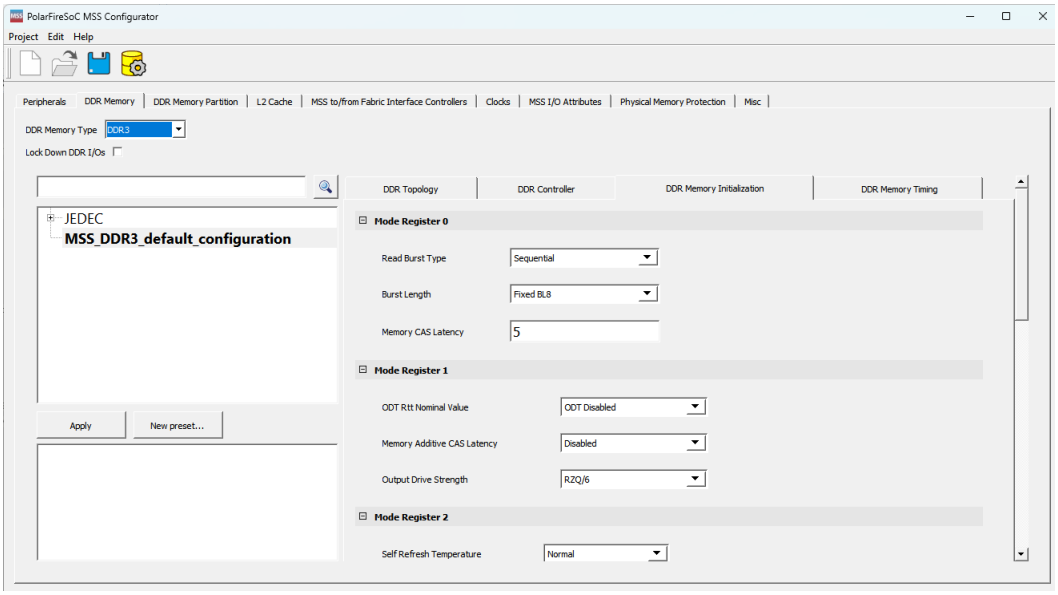
DDR Memory Initialization

The **DDR Memory Initialization** tab defines how the external DDR device itself is programmed during power-up. Its main purpose is to configure the DDR mode registers so that the memory operates correctly and matches both the JEDEC specification and the specific DDR device used on the board.

In the PolarFire SoC architecture, these settings are executed by the E51 monitor core during boot as part of the automatic DDR bring-up sequence.

The following figure shows the memory initialization configuration.

Figure 2-9. DDR Memory Initialization



The following table describes the options available in the **DDR Memory Initialization** tab for DDR3 and DDR3L.

Table 2-5. DDR Memory Initialization for DDR3 and DDR3L

Category	Option	Description
Mode Register 0	Read Burst Type	Specifies how column addresses advance during a read burst. The following values are supported: • Sequential (default): Data is returned from consecutive column addresses. For example, Col 0 → 1 → 2 → 3 and so on. • Interleaved: Column addresses toggle in a predefined pattern around the starting address. Historically used to reduce bank conflicts in older systems.
	Burst Length	Defines how many data words are transferred per memory command. A data word is the width of the DDR interface (x16, x32, x64, and so on). The following values are supported: • Fixed BL8 (default): 8 transfers. For example, for a x16 DRR, this means 16 bits × 8 transfers = 128 bits (16 bytes) per burst. • On-the-fly BC4 or BL8: The memory device can dynamically select the burst length per command, instead of being fixed at initialization.
	Memory CAS Latency	Specifies the number of clock cycles between issuing a READ command and when the first data appears on the DQ pins. For example, if CAS latency is 5, data appears 5 memory clock cycles after READ. This value must match the DDR memory device datasheet.

Table 2-5. DDR Memory Initialization for DDR3 and DDR3L (continued)

Category	Option	Description
Mode Register 1	ODT Rtt Nominal Value	Sets the internal termination resistance inside the DDR memory device which helps in reducing the signal reflections on the DQ/DQs lines. The values are defined relative to RZQ, an external precision resistor (~ 240 Ω) connected to the DRAM. The following values are supported: • ODT Disabled (default): No ODT • RZQ/2: ~ 120Ω • RZQ/4: ~ 60Ω • RZQ/6: ~ 40Ω • RZQ/12 for non-write: ~ 20Ω • RZQ/8 for non-write: ~ 30Ω
	Memory Additive CAS Latency	Adds extra latency between an ACTIVATE command and a READ/WRITE. The following values are supported: • Disabled (default) • CL-1: Adds a CAS latency of 1 clock cycle • CL-2: Adds a CAS latency of 2 clock cycles
	Output Drive Strength	Controls the output driver impedance of the DDR memory device. The following values are supported: • RZQ/6 (default): ~ 34Ω • RZQ/7: ~ 40Ω
Mode Register 2	Self Refresh Temperature	Selects the temperature range assumed by the DRAM during self-refresh. The following values are supported: • Normal (default): Standard commercial temperature range. Suitable for most systems. • Extended: High-temperature operation (industrial/automotive). Suitable for systems that may exceed normal operating temperatures.
	Memory Write CAS Latency	Specifies the number of clock cycles between a WRITE command and when write data is captured by the DRAM. Values between 5 and 12 are supported.
	Partial Array Self Refresh	Specifies how much of the DRAM array is refreshed during self-refresh mode and helps reduce self-refresh power consumption. Unrefreshed regions lose data. The following values are supported: • Full (default) • Half • Quarter • 1/8 • Half (reversed) • Quarter (reversed) • 1/8 (reversed)
	Dynamic ODT (Rtt_WR)	Controls the ODT used only during WRITE operations. Enabling this option temporarily overrides Rtt_Nom (MR1) during write bursts. The following values are supported: • Dynamic ODT Off (default) • RZQ/4 (~60Ω) • RZQ/2 (~120Ω)

The following table describes the options available in the **DDR Memory Initialization** tab for DDR4.

Table 2-6. DDR Memory Initialization for DDR4

Category	Option	Description
Mode Register 0	Read Burst Type	Specifies how column addresses advance during a read burst. The following values are supported: • Sequential (default): Data is returned from consecutive column addresses. For example, Col 0 → 1 → 2 → 3 and so on. • Interleaved: Column addresses toggle in a predefined pattern around the starting address. Historically used to reduce bank conflicts in older systems.
	Burst Length	Defines how many data words are transferred per memory command. A data word is the width of the DDR interface (x16, x32, x64, and so on). The following values are supported: • Fixed BL8 (default): 8 transfers. For example, for a x16 DRR, this means 16 bits × 8 transfers = 128 bits (16 bytes) per burst. • On-the-fly BC4 or BL8: The memory device can dynamically select the burst length per command, instead of being fixed at initialization.
	Memory CAS Latency	Specifies the number of clock cycles between issuing a READ command and when the first data appears on the DQ pins. For example, if CAS latency is 5, data appears 5 memory clock cycles after READ. This value must match the DDR memory device datasheet.
Mode Register 1	ODT Rtt Nominal Value	Sets the internal termination resistance inside the DDR memory device which helps in reducing the signal reflections on the DQ/DQs lines. The values are defined relative to RZQ, an external precision resistor (~ 240Ω) connected to the DRAM. The following values are supported: • ODT Disabled: No ODT • RZQ/2: ~ 120Ω • RZQ/4 (default): ~ 60Ω • RZQ/6: ~ 40Ω • RZQ/12 for non-write: ~ 20Ω • RZQ/8 for non-write: ~ 30Ω
	Memory Additive CAS Latency	Adds extra latency between an ACTIVATE command and a READ/WRITE. The following values are supported: • Disabled (default) • CL-1: Adds a CAS latency of 1 clock cycle • CL-2: Adds a CAS latency of 2 clock cycles
	Output Drive Strength	Controls the output driver impedance of the DDR memory device. The following values are supported: • RZQ/7 (default): ~ 34Ω • RZQ/5: ~ 48Ω

Table 2-6. DDR Memory Initialization for DDR4 (continued)

Category	Option	Description
Mode Register 2	Low Power Auto Self Refresh	Enables minimizing power consumption while preserving data when the system is idle or in a low-power state. The following values are supported: • Automatic (default) • Manual–Normal • Manual–Reduced • Manual–Extended
	Memory Write CAS Latency	Specifies the number of clock cycles between the WRITE command and the moment when valid write data must be presented on the DQ bus. Values between 9–20 are supported.
	Dynamic ODT (Rtt_WR)	Controls the On-die termination used only during WRITE operations. Enabling this option temporarily overrides Rtt_Nom (MR1) during write bursts. The following values are supported: • Dynamic ODT Off (default) • RZQ/2 (~120 Ω) • RZQ/1 (~240 Ω) • High-Z • RZQ/3 (~80 Ω)
Mode Register 3	Fine Granularity Refresh Mode	Enables the memory to change how often refresh operations occur, trading refresh frequency against refresh latency and bandwidth impact. The following values are supported: • Normal (1x): Standard JEDEC refresh • Fixed 2x (default) • Fixed 4x • On-the-fly 1x/2x • On-the-fly 2x/4x

Table 2-6. DDR Memory Initialization for DDR4 (continued)

Category	Option	Description
Mode Register 4	Temperature Refresh Range	Defines the temperature operating range assumed by the DDR4 device for determining its required refresh rate. This setting tells the memory whether it should use normal or extended temperature refresh timing, as defined by the JEDEC specification. The following values are supported: • Normal (default) • Extended
	Temperature Refresh Mode	Controls whether the device actively monitors its internal temperature and automatically adjusts the refresh rate based on that temperature. This feature enables temperature-controlled refresh, as defined by the JEDEC specification. The following values are supported: • Disabled (default) • Enabled
	Internal VRef Monitor	Specifies whether the device monitors its internally generated reference voltage (Vref) used by the input receivers for data (DQ), data strobes (DQS), and command/address signals. When the Internal Vref Monitor is enabled, the device continuously checks that its internal Vref generator remains within JEDEC-specified limits. If the internal Vref drifts outside the allowed range due to voltage, temperature, or noise issues, the device can internally flag this condition (device-specific behavior). The following values are supported: • Disabled (default) • Enabled
	Self Refresh Abort Mode	Controls how the DDR4 device exits Self-Refresh mode when normal operation must resume. Specifically, it determines whether the memory allows an early termination (abort) of an ongoing self-refresh cycle. The following values are supported: • Disabled (default) • Enabled
	READ Preamble	Configures the length of the DQS preamble that precedes valid read data when the device drives data back to the controller. This setting affects read timing margin, training robustness, and read latency. The following values are supported: • 1 CK (default): One clock-cycle DQS preamble • 2 CK: Two clock-cycle DQS preamble
	Write Preamble	Configures the length of the DQS preamble that the memory controller drives before write data is transferred to the device. It affects write timing margin, write leveling robustness, and write latency. The following value is currently supported: • 1 CK (default): One clock-cycle DQS preamble

Table 2-6. DDR Memory Initialization for DDR4 (continued)

Category	Option	Description
Mode Register 5	CA Parity Latency Mode	Specifies the number of clock cycles the device waits before executing the command, allowing time for parity validation. The following values are supported: • Disabled (default) • 4 clocks • 5 clocks • 6 clocks • 8 clocks
	ODT Input Buffer for Power-down	Controls whether the ODT input buffer remains enabled or is disabled when the device enters Power-down mode. This setting affects power consumption, signal integrity, and bus stability during low-power states. The following values are supported: • Disabled (default) • Enabled
	Parked ODT Value (Rtt_Park)	Defines the ODT resistance that the device applies when it is not actively participating in a read or write operation–that is, when the rank is idle (parked). This setting is mainly used in multi-rank DDR4 systems to maintain good signal integrity on the data bus. The following values are supported: • Disabled (default) • RZQ/4 • RZQ/2 • RZQ/6 • RZQ/1 • RZQ/5 • RZQ/3 • RZQ/7
Mode Register 6	Vref Calibration Enable	Controls whether the device participates in VrefDQ calibration (Vref training) during memory initialization. This feature allows the controller to optimize the data input reference voltage (VrefDQ) to improve read and write reliability. The following values are supported: • Enabled (default) • Disabled
	Vref Calibration Range	Defines the allowed voltage search window that the device uses during VrefDQ calibration (Vref training). It limits the range of reference voltages the controller can sweep while determining the optimal DQ reference voltage (VrefDQ). The following values are supported: • Range 1 (60%–92.5%) • Range 2 (45%–77.5%)
	Vref Calibration Value	Specifies the exact reference voltage (VrefDQ) that the device uses for DQ/DQS input sampling when Vref calibration is disabled, or it defines the initial/final programmed value when calibration is enabled. This value affects read and write data reliability, because it sets the voltage threshold used to interpret logic levels on the data bus.

The following table provides the **DDR Memory Initialization** options for LPDDR3.

Table 2-7. DDR Memory Initialization for LPDDR3

Category	Option	Description
Mode Register 2	Data Latency (#RL, #WL)	Defines how many clock cycles elapse between a memory command and when valid data is transferred on the DQ bus. • #RL (Read Latency) = CAS Latency + Additive Latency • #WL (Write Latency) = CAS Write Latency + Additive Latency
Mode Register 3	Output Drive Strength	Configures the output driver impedance for data (DQ), data strobe (DQS), and, in some cases, command/address signals. This setting affects signal integrity, edge rate, EMI, and power consumption on the interface.
Mode Register 11	DQ ODT	Defines whether and how termination is applied on the DQ/DQS lines when the memory is actively driving or receiving data. The following values are supported: • Disabled (default) • RZQ/4 • RZQ/2 • RZQ/1
	Power Down ODT	Controls whether ODT remains active or inactive when the device enters Power-down mode. This option affects standby power consumption and data bus stability while the memory is in a low-power state.

The following table provides the DDR Memory Initialization options for LPDDR4.

Table 2-8. DDR Memory Initialization for LPDDR4

Category	Option	Description
Mode Register 1	RD Pre-amble Type	Defines the DQS behavior immediately before read data starts. This setting affects how early the controller can detect and align to DQS. The following values are supported: • Static (default): DQS is held at a constant logic level (0 or 1) before toggling. • Toggle: DQS toggles for 1 UI before read data.
	RD Post-amble Length	Determines how long DQS continues toggling after the last read data beat. The following values are supported: • 0.5*tCK (default): DQS toggles for half a clock cycle after last data. • 1.5 *tCK: DQS toggles for one and half a clock cycles after last data.
Mode Register 2	Read Latency (#RL, #nRTP)	Specifies the number of memory clock cycles between issuing a READ command and when the first valid read data appears on the DQ bus. It is represented as a combination of #RL (Read Latency) and #nRTP (Read-to-Precharge Time).
	Write Latency	Specifies the number of clock cycles between issuing a WRITE command and when the DRAM expects valid write data. #WL (Write Latency) = CAS Write Latency + Additive Latency

Table 2-8. DDR Memory Initialization for LPDDR4 (continued)

Category	Option	Description
Mode Register 3	Pull-up Calibration Point	Selects the reference point used to calibrate the pull-up (PMOS) output driver impedance of the device. The following values are supported: • Mid-point (default) • End-point
	WR Post-amble Length	Controls the length of the write post-amble, that is, how long DQS remains active after the last write data beat. The following values are supported: • 0.5 tCK (default) • 1.5 tCK
	Pull-down Drive Strength	Selects the pull-down (NMOS) output driver impedance for DQ/DQS signals. The following values are supported: • RZQ/1 • RZQ/2 (default) • RZQ/3 • RZQ/4
Mode Register 4	Self Refresh Abort Mode	Controls how the DDR4 device exits Self-Refresh mode when normal operation must resume. Specifically, it determines whether the memory allows an early termination (abort) of an ongoing self-refresh cycle. The following values are supported: • Disabled (default) • Enabled
Mode Register 11	DQ ODT	Selects the ODT resistance inside the LPDDR4 DRAM for data signals during read/write operations. The following values are supported: • Disable • 40Ω • 48Ω • 60Ω (default) • 80Ω • 120Ω • 240Ω
	CA ODT	Selects the ODT resistance inside the LPDDR4 DRAM for command/address signals. The following values are supported: • Disable • 40Ω • 48Ω • 60Ω (default) • 80Ω • 120Ω • 240Ω

Table 2-8. DDR Memory Initialization for LPDDR4 (continued)

Category	Option	Description
Mode Register 14	Vref Calibration Enable	Controls whether the device participates in VrefDQ calibration (Vref training) during memory initialization. This feature allows the controller to optimize the data input reference voltage (VrefDQ) to improve read and write reliability. The following values are supported: • Enabled (default) • Disabled
	Vref Calibration Range	Defines the allowed voltage search window that the device uses during VrefDQ calibration (Vref training). It limits the range of reference voltages the controller can sweep while determining the optimal DQ reference voltage (VrefDQ). The following values are supported: • Range 1 (60%–92.5%) • Range 2 (45%–77.5%)
	Vref Calibration Value	Specifies the exact reference voltage (VrefDQ) that the device uses for DQ/DQS input sampling when Vref calibration is disabled, or it defines the initial/final programmed value when calibration is enabled. This value affects read and write data reliability, because it sets the voltage threshold used to interpret logic levels on the data bus.
Mode Register 22	SoC ODT	Enables or disables the SoC ODT mode in the device. When enabled, the DRAM applies ODT during SoC-driven transactions. The following values are supported: • Disable • Enable (default)
	ODTE-CK	Enables Clock (CK) signal to assert SoC ODT when toggling. This option is selected by default.
	ODTE-CS	Enables Chip Select (CS) to assert SoC ODT. This option is selected by default.
	ODTE-CA	Enables Command/Address (CA) signals to assert SoC ODT. This option is selected by default.

DDR Memory Timing

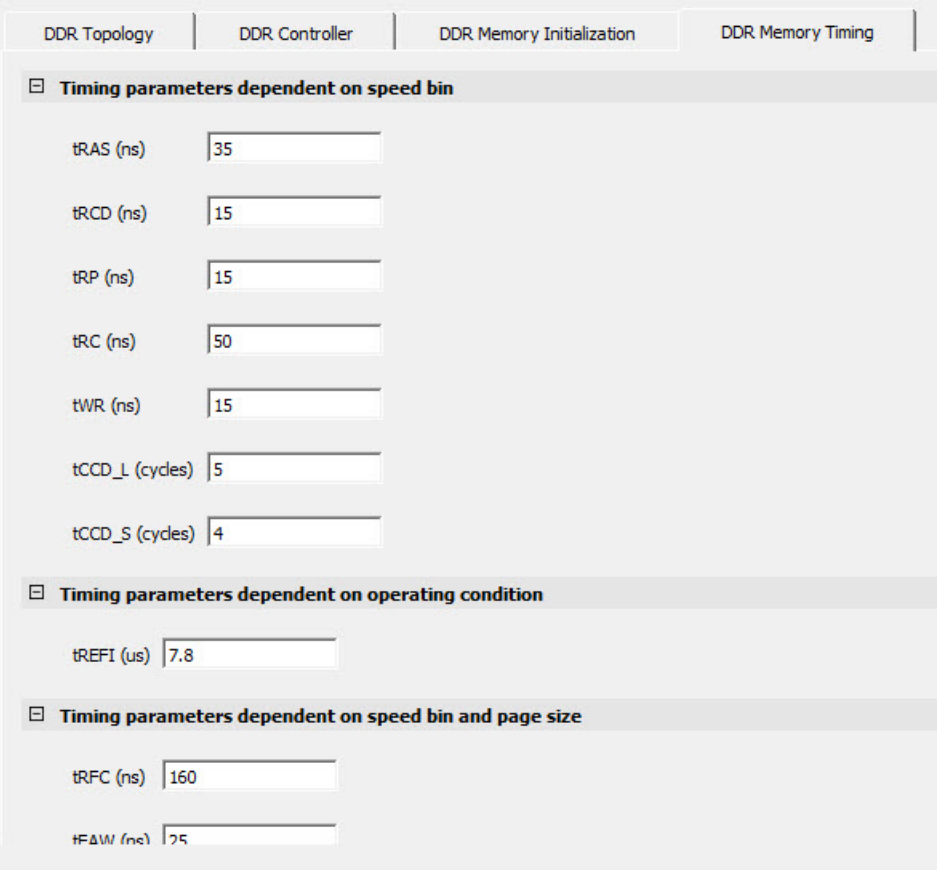
The **DDR Memory Timing** tab controls the timing parameters, which are translated to the appropriate configuration values for the DDR subsystem IP.

Notes:

- All parameters are editable numeric fields.
- All parameters support the JEDEC ranges.
- The default values are auto-computed when:
  - Memory type is selected
  - Frequency is changed
  - Defaults are restored

The following image shows the **DDR Memory Timing** tab.

Figure 2-10. DDR Memory Timing Tab



The following table describes the options available on the **DDR Memory Timing** tab that are applicable to DDR3 and DDR3L memory types.

Table 2-9. Timing Parameters for DDR3 and DDR3L

Category	Parameter	Description
Timing parameters dependent on speed bin	tRAS (ns)	Row Active Time Minimum time a row must remain open after an ACTIVATE command.
	tRCD (ns)	RAS to CAS Delay Delay from ACTIVATE (row open) to READ or WRITE command.
	tRP (ns)	Row Precharge Time Minimum time required to close (precharge) a row before opening another.
	tRC (ns)	Row cycle time Minimum time between ACTIVATE commands to the same bank. tRC = tRAS + tRP
	tWR (ns)	Write Recovery Time Minimum time from WRITE command to PRECHARGE.
	tFAW (ns)	Four ACTIVATE window Time window limiting how many ACTIVATE commands can occur.

Table 2-9. Timing Parameters for DDR3 and DDR3L (continued)

Category	Parameter	Description
Timing parameters dependent on speed bin and clock frequency	tWTR (cycles)	WRITE to READ delay Delay from WRITE command to a subsequent READ command.
	tRRD (ns)	Row to Row Delay Minimum time between ACTIVATE commands to different banks.
	tRTP (ns)	READ to PRECHARGE delay Minimum time from READ command to PRECHARGE.
Timing parameters dependent on operating condition	tREFI (ns)	Refresh interval Average time between refresh commands.
Timing parameters dependent on speed bin and page size	tRFC (ns)	Refresh cycle time Time required to complete a refresh operation.
Other timing parameters	tZQinit (cycles)	ZQ Initialization Time Time required for initial ZQ calibration after reset.
	ZQ Calibration Type	Selects the type of ZQ calibration performed. • Long—full calibration • Short—periodic fine calibration
	tZQCS (cycles)	ZQ Calibration Short Duration of a short (incremental) ZQ calibration.
	tZQoper (cycles)	ZQ Operation Time Minimum time between ZQ calibration commands.
	Enable User ZQ Calibration Controls	Allows manual control of ZQ timing parameters. When enabled, the user can override auto-calculated ZQ values.
	Automatic ZQ Calibration Period (us)	Interval at which automatic ZQ short calibration is performed.

The following table lists and describes the timing parameters available for DDR4.

Table 2-10. Timing Parameters for DDR4

Category	Parameter	Description
Timing parameters dependent on speed bin	tRAS (ns)	Row Active Time Minimum time a row must remain open after an ACTIVATE command.
	tRCD (ns)	RAS to CAS Delay Delay from ACTIVATE (row open) to READ or WRITE command.
	tRP (ns)	Row Precharge Time Minimum time required to close (precharge) a row before opening another.
	tRC (ns)	Row cycle time Minimum time between ACTIVATE commands to the same bank. tRC = tRAS + tRP
	tWR (ns)	Write Recovery Time Minimum time from WRITE command to PRECHARGE.
	tCCD_L (cycles)	Long Column-to-Column Delay Minimum delay between two column commands (READ or WRITE) issued to banks in different bank groups.
	tCCD_S (cycles)	Short Column-to-Column Delay Minimum delay between two column commands (READ or WRITE) issued to banks within the same bank group.
Timing parameters dependent on operating condition	tREFI (us)	Refresh interval Average time between refresh commands.

Table 2-10. Timing Parameters for DDR4 (continued)

Category	Parameter	Description
Timing parameters dependent on speed bin and page size	tRFC (ns)	Refresh cycle time Time required to complete a refresh operation.
	tFAW (ns)	Four Activate Window Rolling time window during which no more than four ACTIVATE (ACT) commands are allowed.
Timing parameters dependent on speed bin and clock frequency	tWTR_L (cycles)	Long Write-to-Read Delay Minimum delay between a WRITE command and a subsequent READ command issued to a bank in a different bank group.
	tWTR_S (cycles)	Short Write-to-Read Delay Minimum delay between a WRITE command and a subsequent READ command issued to a bank in the same bank group.
	tRRD_L (cycles)	Long Row-to-Row Delay Minimum delay between two ACTIVATE (ACT) commands issued to banks in different bank groups.
	tRRD_S (cycles)	Short Row-to-Row Delay Minimum delay between two ACTIVATE (ACT) commands issued to different banks within the same bank group.
	tRTP (ns)	READ to PRECHARGE delay Minimum time from READ command to PRECHARGE.
Other timing parameters	tZQinit (cycles)	ZQ Initialization Time Time required for initial ZQ calibration after reset.
	ZQ Calibration Type	Selects the type of ZQ calibration performed. • Long—full calibration • Short—periodic fine calibration
	tZQCS (cycles)	ZQ Calibration Short Duration of a short (incremental) ZQ calibration.
	tZQoper (cycles)	ZQ Operation Time Minimum time between ZQ calibration commands.
	Enable User ZQ Calibration Controls	Allows manual control of ZQ timing parameters. When enabled, the user can override auto-calculated ZQ values.
	Automatic ZQ Calibration Period (us)	Interval at which automatic ZQ short calibration is performed.

The following table lists and describes the timing parameters for LPDDR3

Table 2-11. Timing Parameters for LPDDR3

Category	Parameter	Description
Timing parameters dependent on speed bin	tRAS (ns)	Row Active Time Minimum time a row must remain open after an ACTIVATE command.
	tRCD (ns)	RAS to CAS Delay Delay from ACTIVATE (row open) to READ or WRITE command.
	tRP (ns)	Row Precharge Time Minimum time required to close (precharge) a row before opening another.
	tRC (ns)	Row cycle time Minimum time between ACTIVATE commands to the same bank. tRC = tRAS + tRP
	tWR (ns)	Write Recovery Time Minimum time from WRITE command to PRECHARGE.
	tFAW (ns)	Four ACTIVATE window Time window limiting how many ACTIVATE commands can occur.
	tMMR (cycles)	Mode Register to Mode Register Delay Minimum delay between two consecutive Mode Register commands.
	tMRW (cycles)	Mode Register Write Time Minimum time required to complete a Mode Register Write (MRW) command.
Timing parameters dependent on speed bin and clock frequency	tWTR (cycles)	WRITE to READ delay Delay from WRITE command to a subsequent READ command.
	tRRD (ns)	Row to Row Delay Minimum time between ACTIVATE commands to different banks.
	tRTP (ns)	READ to PRECHARGE delay Minimum time from READ command to PRECHARGE.
Timing Parameters dependent on operating condition	tREFI (ns)	Refresh interval Average time between refresh commands.
Timing parameters dependent on speed bin and page size	tRFC (ns)	Refresh cycle time Time required to complete a refresh operation.
Other timing parameters	tZQinit (us)	ZQ Initialization Time Time required for initial ZQ calibration after reset.
	ZQ Calibration Type	Selects the type of ZQ calibration performed. • Long—full calibration • Short—periodic fine calibration
	tZQCS (ns)	ZQ Calibration Short Time Time required to complete a short ZQ calibration (ZQCS command).
	tZQCL (ns)	ZQ Calibration Long Time Time required to complete a long ZQ calibration (ZQCL command).
	tZQRESET (ns)	ZQ Reset Time Minimum time the device must wait after a ZQRESET event before any ZQ calibration command (ZQCL or ZQCS) can be issued.
	Enable User ZQ Calibration Controls	Allows manual control of ZQ timing parameters. When enabled, the user can override auto-calculated ZQ values.
	Automatic ZQ Calibration Period (us)	Interval at which automatic ZQ short calibration is performed.

The following parameters are supported for LPDDR4.

Table 2-12. Timing Parameters for LPDDR4

Category	Parameter	Description
Timing parameters dependent on speed bin	tRAS (ns)	Row Active Time Minimum time a row must remain open after an ACTIVATE command.
	tRCD (ns)	RAS to CAS Delay Delay from ACTIVATE (row open) to READ or WRITE command.
	tRP (ns)	Row Precharge Time Minimum time required to close (precharge) a row before opening another.
	tRC (ns)	Row cycle time Minimum time between ACTIVATE commands to the same bank. tRC = tRAS + tRP
	tWR (ns)	Write Recovery Time Minimum time from WRITE command to PRECHARGE.
	tMMR (cycles)	Mode Register to Mode Register Delay Minimum delay between two consecutive Mode Register commands.
	tMRW (cycles)	Mode Register Write Time Minimum time required to complete a Mode Register Write (MRW) command.
Timing parameters dependent on speed bin and clock frequency	tWTR (cycles)	WRITE to READ delay Delay from WRITE command to a subsequent READ command.
	tRRD (ns)	Row to Row Delay Minimum time between ACTIVATE commands to different banks.
	tRTP (ns)	READ to PRECHARGE delay Minimum time from READ command to PRECHARGE.
Timing Parameters dependent on operating condition	tREFI (ns)	Refresh interval Average time between refresh commands.
Timing parameters dependent on speed bin and page size	tRFC (ns)	Refresh cycle time Time required to complete a refresh operation.
	tFAW (ns)	Four ACTIVATE window Time window limiting how many ACTIVATE commands can occur.
Other timing parameters	ZQ Calibration Time (us)	Defines how long the DDR controller waits for the ZQ calibration (ZQCL or ZQCS) to complete before resuming normal memory traffic.
	ZQ Calibration Latch Time (ns)	Minimum time required for the DRAM to latch (capture and apply) the results of a ZQ calibration operation after the calibration measurement itself has completed.
	tZQRESET (ns)	ZQ Reset Time Minimum time the device must wait after a ZQRESET event before any ZQ calibration command (ZQCL or ZQCS) can be issued.
	Enable User ZQ Calibration Controls	Allows manual control of ZQ timing parameters. When enabled, the user can override auto-calculated ZQ values.
	Automatic ZQ Calibration Period (us)	Interval at which automatic ZQ short calibration is performed.

Advanced

Available only for the LPDDR3 and LPDDR4 memory types, the **Advanced** tab controls the self refresh mode parameters (idle time to self refresh and clock disable in self refresh).

Figure 2-11. Advanced Tab

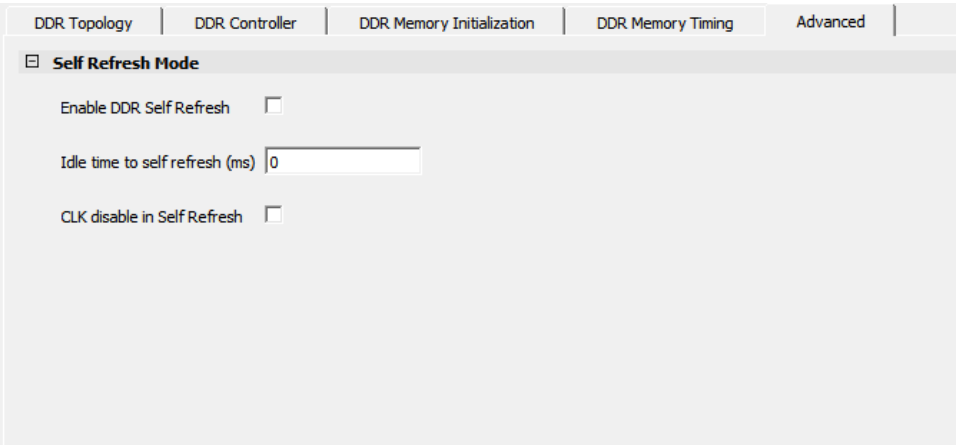


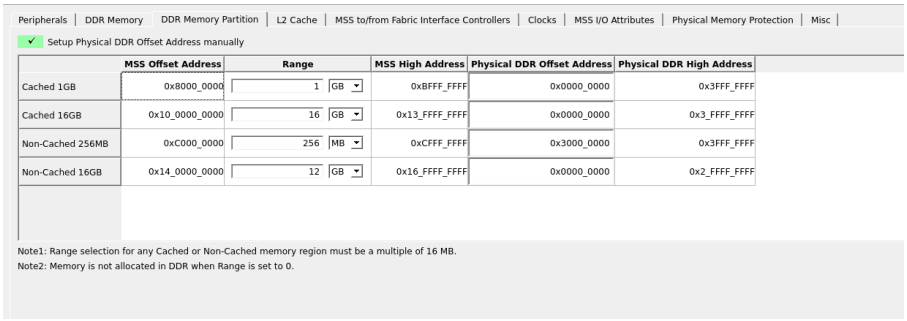
Table 2-13. Advanced options

Category	Option	Description
Self Refresh Mode	Enable DDR Self Refresh	Allows the DDR controller to place the external DRAM into Self-Refresh mode, where the memory refreshes itself internally without requiring periodic refresh commands from the controller. This option is disabled by default.
	Idle time to self refresh (ms)	Minimum continuous idle duration after which the DDR controller will automatically place the DRAM into Self-Refresh mode.
	CLK disable in Self Refresh	Controls whether the external DDR clock (CK) is stopped (disabled) while the DRAM is in Self-Refresh mode. This option is disabled by default.

2.3.3. DDR Memory Partition (Ask a Question)

The DDR Memory Partition tab allows the DDR memory to be allocated to cached and non-cached regions depending on the amount of DDR memory physically connected.

Figure 2-12. DDR Memory Partition Tab



In the DDR Memory Partition:

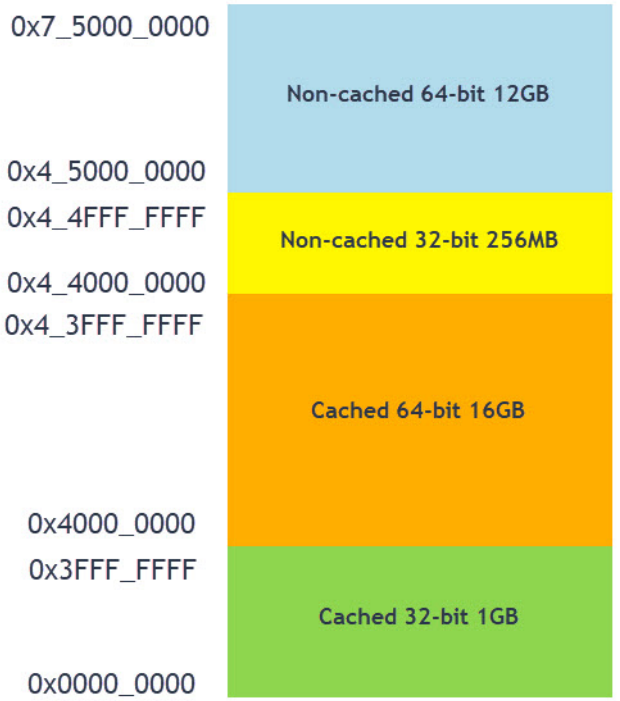
- The Offset Address (Base Address) for both cached and non-cached regions is fixed.
- High Address is the End Address based on the size.
- Users are expected to enter the Range. Based on the Range selection, High Address and Physical DDR Offset is updated.
  - When Range is set to zero, memory is not allocated in DDR.
  - When Range is set to a nonzero value, it must be a multiple of 16 MB.
- Physical DDR Offset is allocation of DDR memory (connected to the FPGA system) based on the nonzero Range value.

Important: When **Setup Physical DDR Address manually** option is enabled, the default Physical DDR Offset Address is set as 0x0000_0000 for all the regions and it is up to the user to change this address (when the size of the allocated memory region is greater than 0 bytes). When the size of allocated memory region is zero bytes, the offset and high address are reported as **N/A** and remains as a read-only field.

- Range is allocated sequentially starting with 0x0000_0000 in the following order:
  - Cached 32-bit
  - Cached 64-bit
  - Non-Cached 32-bit
  - Non-Cached 64-bit

  The following figure shows the graphical representation of how the Physical DDR Offset allocation is done based on the preceding ranges:

Figure 2-13. Physical DDR Offset — Graphical Representation



2.3.4. Crypto (Ask a Question)

The following table lists the crypto ownership modes.

Table 2-14. Crypto Ownership Modes

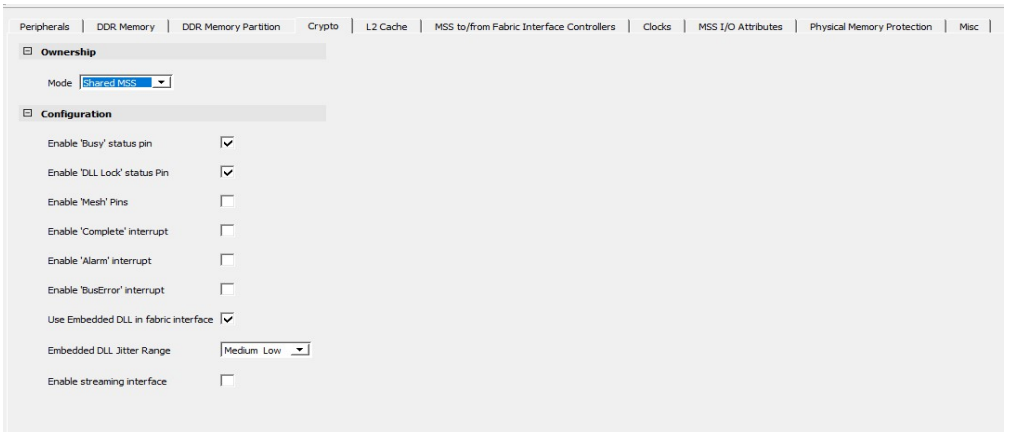
Owner	Description
MSS	The MSS owns the crypto.
Fabric	The Fabric owns the crypto and ports are exposed to the fabric.

Table 2-14. Crypto Ownership Modes (continued)

Owner	Description
Shared MSS	This is shared between the MSS and the Fabric. The MSS is the first owner. There are regular ports and other ports for handshaking to switch the ownership.
Shared Fabric	This is shared between the MSS and the Fabric. The Fabric is the first owner. There are regular ports and other ports for handshaking and to switch ownership.

Note: Streaming Interface is not available for Fabric mode.

Figure 2-14. Crypto Tab



In the crypto modes:

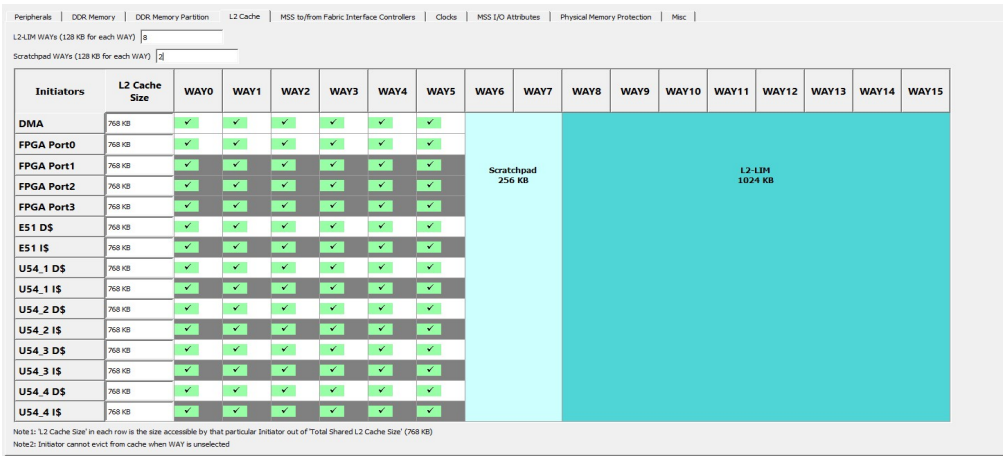
- The status pins and interrupt pins are available as configuration options in all the ownership modes except the MSS ownership mode.
- There are three options that expose the DLL lock, Busy, and Mesh ports. The Busy and DLL Lock are ON by default, while the Mesh input pin connects to 0 when not used.
- The **Use embedded DLL in fabric interface** is always provided in all modes and is enabled by default when the **Enable streaming interface** option is selected.

2.3.5. L2 Cache (Ask a Question)

Level2 memory subsystem has three operating modes – Cache, Loosely-Integrated-Memory (LIM), and Scratchpad. These modes can be configured in MSS configurator using the options in the L2 Cache tab based on user needs. The goal is to make the configuration options easier to use and understand for the users.

You can allocate L2 memory for the processor or peripheral using the **L2 Cache** tab, as shown in the following figure.

Figure 2-15. L2 Cache



In the L2 Cache tab:

- There are 16 WAYs. WAY0 is always allocated for Cache.
- In the GUI, the default L2-LIM size will be set at 15 (WAY1 – WAY15). This means that 1 WAY (128 Kbytes) is configured as L2 cache and 1920 Kbytes is configured as LIM. User can increase or decrease the L2-LIM size to configure the LIM as Cache memory for various processors and peripherals.
- In the GUI, all the WAYs are enabled for Cache by default. The user can disable the selection to allocate it for Scratchpad.
- Cache size shows the amount of memory available and is shared among all processors and peripherals.

Important:

- All AXI4 front way ports must be identical.
- The core D and I Ways have to be identical and hence ways for port 1, 2, 3, and ways for core I are disabled for selection.

2.3.6. MSS To/From Fabric Interface Controllers (Ask a Question)

Using the **MSS to/from Fabric Interface Controllers** tab, any combination of **FIC_0**, **FIC_1**, **FIC_2**, and **FIC_3** can be enabled and configured to support initiator and target interfaces. For more information, see the PolarFire SoC MSS Technical Reference Manual.

FIC_0, **FIC_1**, and **FIC_2** support AXI4 interfaces, while **FIC_3** supports APB.

For **FIC_0** and **FIC_1** interfaces, both initiator and target interfaces can be enabled at the same time. **FIC_2** interface can support only target interface, and **FIC_3** interface can only support initiator interface (MSS is initiator).

FIC_0 and **FIC_1** have both initiator and target interfaces to and from the FPGA fabric, while **FIC_2** and **FIC_3** support target or initiator interfaces, respectively.

The **Jitter Range** for the Embedded DLLs can be selected in the **Fabric Interface Controller** tab. The **Embedded DLL Jitter Range** drop-down has the following options:

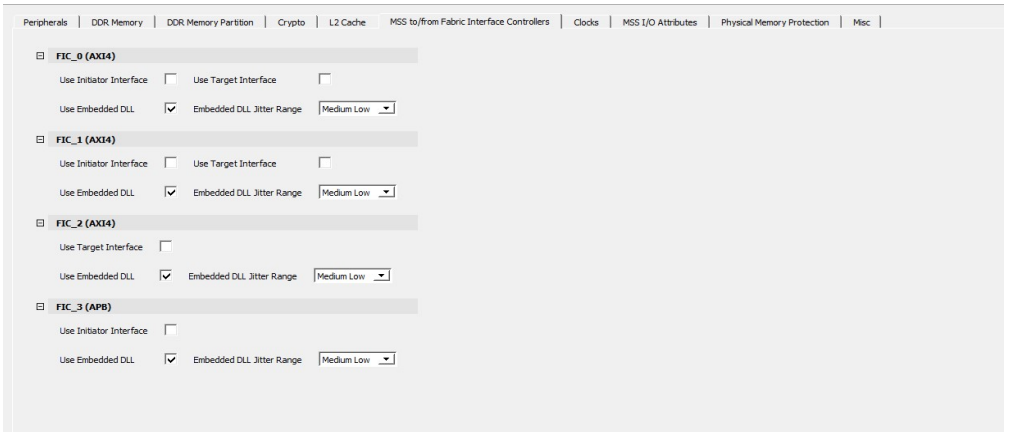
- Low
- Medium Low
- Medium High

- High

Important: The default selection is Medium Low.

The following figure shows all FIC options available and enabled. By default, the DLLs of all the FICs are enabled.

Figure 2-16. MSS to/from Fabric Interface Controllers Tab

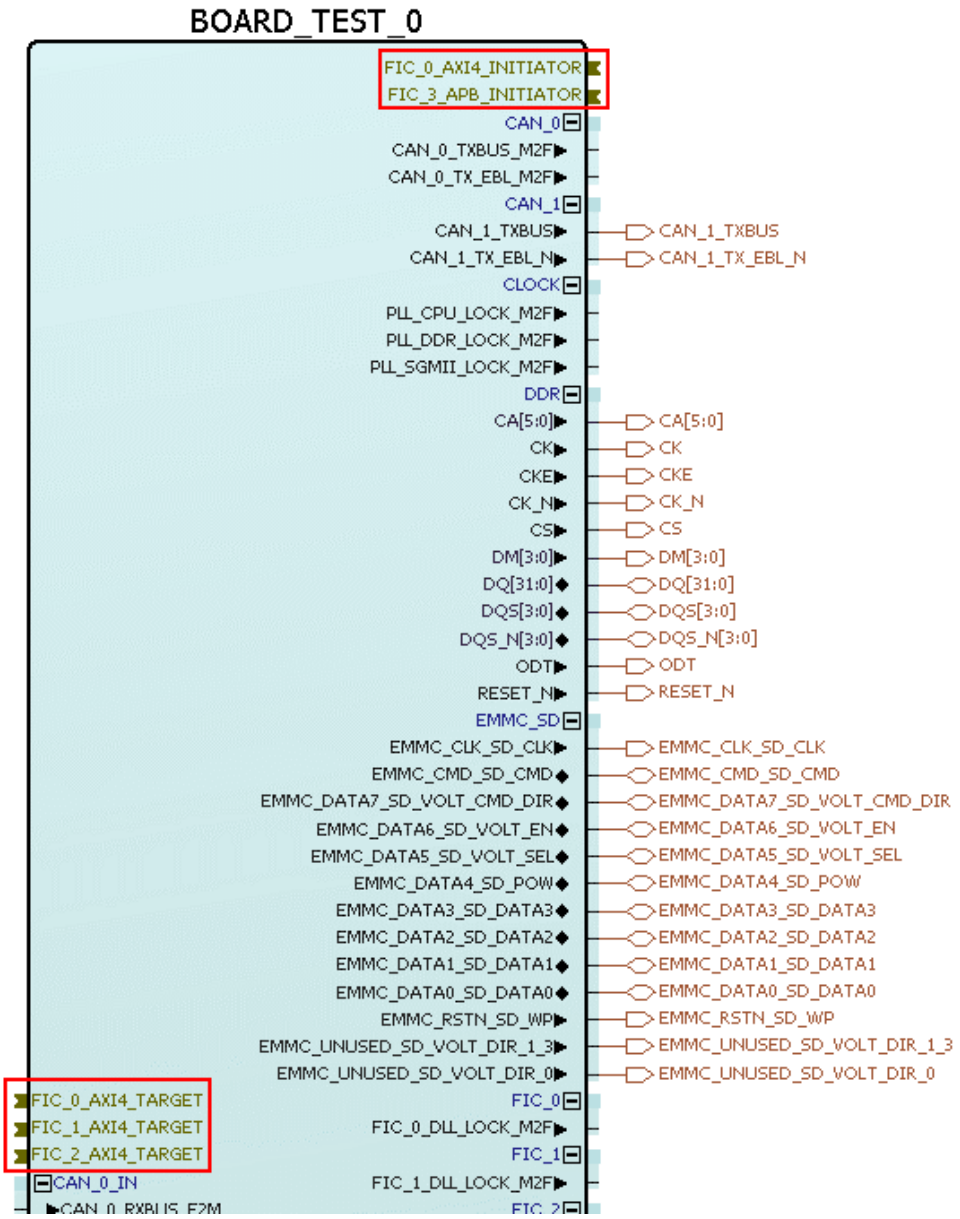


Important: The FIC interface can operate up to 250 MHz. The FIC clock is independent of the MSS clock. If the frequency of the FIC block is greater than or equal to 125 MHz, the embedded DLL must be enabled to remove the clock insertion delay. If the frequency of the FIC block is less than 125 MHz, the embedded DLL must be bypassed.

When an initiator interface is enabled for a FIC, that initiator interface must be connected to a target in the fabric. When a target interface is enabled for an FIC, that target interface must be connected to an initiator in the fabric.

There is a clock domain crossing logic in the FIC block to address the asynchronous MSS and Fabric clocks and therefore, user logic is not required to implement clock domain crossing synchronization for this interface.

Figure 2-17. FIC Interfaces Enabled



Note: The MSS SmartDesign component is visible only after importing the MSS CXZ file.

2.3.7. Clocks (Ask a Question)

Use the **Clocks** tab to configure the MSS PLL clock frequency and clock sources. For more information, see the PolarFire Family Clocking Resources User Guide.

There are three PLLs inside MSS, which generate the necessary clocks:

- MSS PLL
- DDR PLL
- SGMII PLL

Each PLL generates four output clocks from one input reference clock.

The actual output that PLL Solver generates is shown in the GUI next to the **Actual:** label. If the requirement is met, the color of the label is blue. If it is not met (from you), it is red.

In MSS PLL, you must specify the four output clock requirements.

- Output 0 (CPU Clock)
- Output 1 (Crypto Clock)
- Output 2 (eMMC Clock)
- Output 3 (CAN Clock)

The following conditions pose restrictions on the PLL solver. Solver attempts to solve the fixed requirements first and then the ones without restriction.

1. When eMMC is enabled, the output clock requirement is fixed at 200 MHz.
2. When the CAN peripheral is enabled, the output clock requirement must be a multiple of 8 (maximum 80 MHz).
3. Crypto can be at most 200 MHz for STD speed grade and 213 MHz for -1 speed grade.
4. CPU has the maximum frequency of 625 MHz for STD speed grade and 667 MHz for -1 speed grade.
   Note: When the actual frequency found by the PLL solver exceeds the maximum required clock frequency for MSS PLL and Crypto, MSS generation fails with the following error message.

```
ERROR: Invalid solution found for Output0 of MSS PLL. 800 MHz is greater than the
supported value of 667 MHz.
```

In DDR PLL, enter the required output clock frequency in the DDR tab in Line Edit "Memory clock frequency." All four output clocks are generated by the PLL that has the same frequency.

In SGMII PLL, the output frequency requirement is fixed at 625 MHz for all four outputs. You do not have to enter this. Additionally, the output clocks are phase-shifted by 90° (output clock 0 has a 0° phase shift, output clock 1 has a 90° phase shift, and so on).

The following table lists the option provided in the MSS **Clocks** selection tab.

Table 2-15. MSS Clock Selection Tab

Option	Description
eMMC/SD/SDIO clock source	eMMC/SD/SDIO can be clocked either through MSS PLL or Fabric I/O.
CAN clock source	CAN can be clocked either through MSS PLL or Fabric I/O.
MSS PLL reference clock source	MSS can be clocked from dedicated I/O from Bank 5 (REFCLK) or North West PLL output.
MSS PLL required clock frequency	• For STD speed, you can set the frequency value of up to 625 MHz. • For -1 speed, you can set the frequency value of up to 667 MHz. All MSS clock frequencies are derived from this setting.
MSS CPU cores clock frequency divider	The MSS CPU clock frequency is based on the MSS PLL clock frequency and is set using the divider values /1, /2, /4, or /8. The frequency must be greater than or equal to the MSS AXI clock, and can have a maximum value of 667 MHz for -1 speed, and 625 MHz for STD speed.
MSS AXI clock frequency divider	The MSS AXI clock frequency is based on the MSS CPU clock frequency and is set using the divider values of /1, /2, /4, or /8. The frequency must be greater than or equal to MSS AHB/APB clock, and can have a maximum value of 333.50 MHz for -1 speed, and 312.50 MHz for STD speed.
MSS AHB/APB clock frequency divider	The MSS AHB/APB clock frequency is based on the MSS CPU clock frequency and is set using the divider values /2, /4, or /8. The maximum supported frequency is 166.75 MHz for -1 speed, and 156.25 MHz for STD speed.

Table 2-15. MSS Clock Selection Tab (continued)

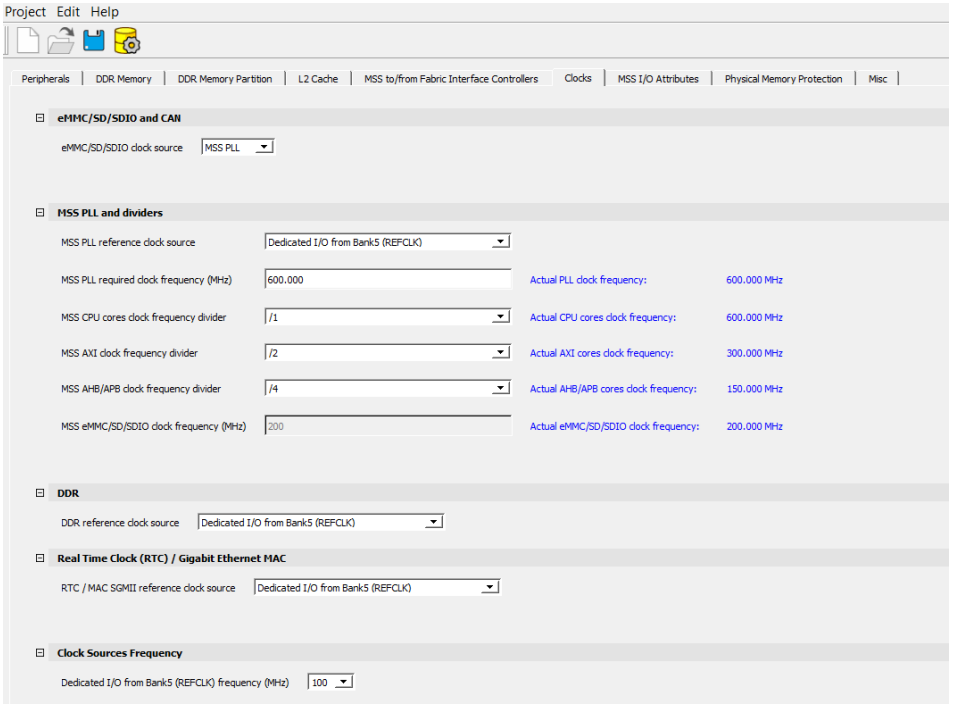
Option	Description
DDR reference clock source	You can select the North West (NW) PLL ports or I/Os from Bank 5.
RTC/MAC SGMII reference clock input source	You can select the NW PLL ports or I/Os from Bank 5.
Dedicated I/O from Bank5 (REFCLK) frequency	This is a dedicated I/O from Bank 5 to the MSS PLL. It can either be 100 MHz or 125 MHz.
NW PLL (REF_0_PLL_NW) frequency (MHz)/NW PLL (REF_1_PLL_NW) frequency (MHz)	This option is available when any peripheral is clocked from NW PLL output. It can be any value between 50 MHz and 125 MHz.
Crypto clock frequency from MSS (MHz)	You can set the reference clock frequency for Crypto between 1 MHz and 200 MHz for STD speed grade, and between 1 MHz and 213 MHz for -1 speed grade.
MSS CAN clock frequency (MHz)	The MSS CPU clock frequency is based on the MSS PLL clock frequency. The supported frequencies in MHz are 8, 16, 24, 32, 40, 48, 56, 64, 72, and 80.

Note: The **DDR Reference Clock Input Source** option appears only when the DDR memory type is selected from the **DDR Memory** tab.

The following figure shows the **Clocks** tab in the PolarFire SoC MSS Configurator. In this example, the following configurations are used:

- Dedicated I/Os from Bank 5 (REFCLK) are selected as the reference clock input source for the MSS. The MSS PLL clock frequency is set to 600 MHz.
- Dedicated I/Os from Bank 5 (REFCLK) are used to source the reference clock input frequency for the DDR subsystem.
- The DDR clock source and MSS clock source are set to 125 MHz.

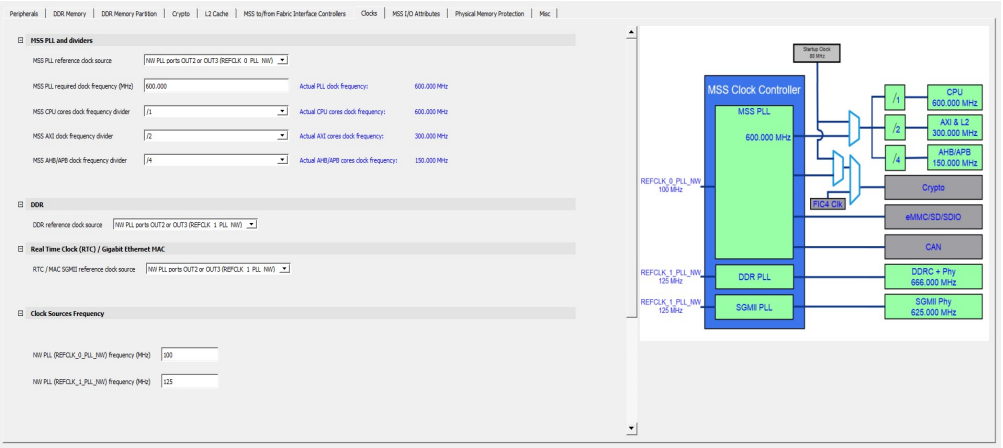
Figure 2-18. Clocks Tab



The following figure shows the **Clocks** tab with PLL in the PolarFire SoC MSS Configurator. In this example, the following configuration is used:

- NW PLL ports OUT2 or OUT3 (REFCLK_0_PLL_NW) are selected as the reference clock input source for the MSS. The MSS PLL clock frequency is set to 600.000 MHz.
- NW PLL ports OUT2 or OUT3 (REFCLK_1_PLL_NW) are used to source the reference clock input frequency for the DDR subsystem and Real Time Clock/Gigabit Ethernet MAC.
- The DDR Clock Source and MSS Clock Source are set to 100 MHz.

Figure 2-19. Clocks Tab with PLL



For more information about configuring the MSS DDR subsystem, see DDR Memory.

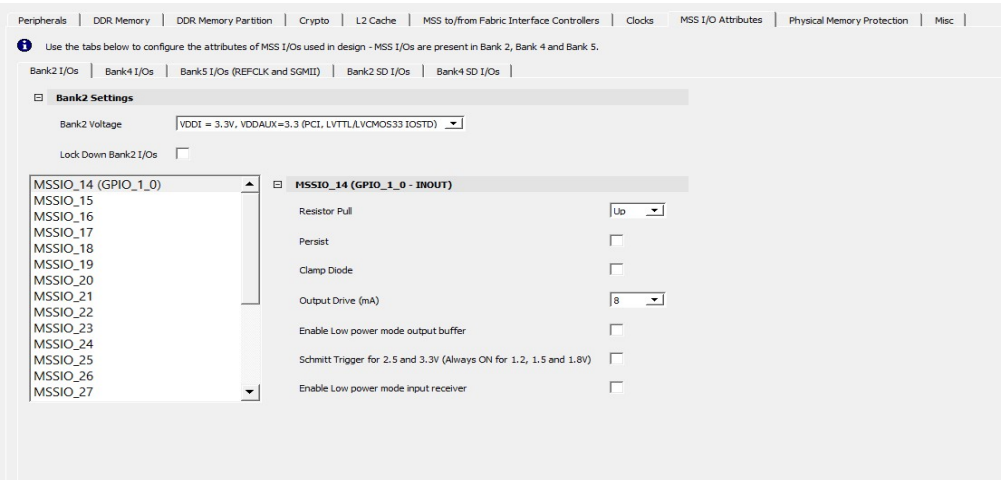
2.3.8. MSS I/O Attributes (Ask a Question)

MSS I/Os are present in Bank2, Bank4, and Bank5. The following sections describe the supported attributes for each bank.

2.3.8.1. Bank2 I/Os (Ask a Question)

The MSS I/Os are available across Bank2. The **Bank2 I/Os** tab allows you to select the electrical characteristics of the MSS I/Os. Each MSS I/O along with the settings must be enabled one-by-one.

Figure 2-20. Bank2 I/Os Tab



Note: Enable the Lock Down Bank2 I/Os option to lock all the Bank2 MSSIOs.

The following table lists the I/O standards and the output drive.

Important: This is applicable to Bank2 and Bank4 MSSIOs only.

Table 2-16. I/O Standard and Output Drive

Protocol	Speed Mode	LVCMOS Standard	Output Current Drive	Supported Out Drive Values
USB 2.0	High	3.3V	8 mA–20 mA	8, 12, 16, and 20 mA
		2.5V	6 mA–16 mA	6, 8, 12, and 16 mA
		1.8V	6 mA–12 mA	6, 8, 10, and 12 mA
eMMC	Default speed	3.3V	3.3V => 2–20 mA	2, 4, 8, 12, 16, and 20 mA
		1.8V	1.8V => 2–10 mA	2, 4, 6, 8, and 10 mA
		1.2V	1.2V => 2–8 mA	2, 4, 6, and 8 mA
	High speed	3.3V	3.3V => 4–20 mA	4, 8, 12, 16, and 20 mA
		1.8V	1.8V => 4–10 mA	4, 6, 8, and 10 mA
		1.2V	1.2V => 4–8 mA	4, 6, and 8 mA
	High speed DDR	3.3V	3.3V => 2–20 mA	2, 4, 8, 12, 16, and 20 mA
		1.8V	1.8V => 2–10 mA	2, 4, 6, 8, and 10 mA
		1.2V	1.2V => 2–8 mA	2, 4, 6, and 8 mA
	HS200	1.8V	1.8V => 6–10 mA	6, 8, and 10 mA
		1.2V	1.2V => 4–8 mA	4, 6, and 8 mA
	HS400	1.8V	1.8V => 4–10 mA	4, 6, 8, and 10 mA
		1.2V	1.2V => 4–8 mA	4, 6, and 8 mA
	HS400-ES	1.8V	1.8V => 4–10 mA	4, 6, 8, and 10 mA
		1.2V	1.2V => 4–8 mA	4, 6, and 8 mA
SDIO	Low Speed	3.3V	2 mA–20 mA	2, 4, 8, 12, 16, and 20 mA
	Full Speed	3.3V	2 mA–20 mA	2, 4, 8, 12, 16, and 20 mA
SD	Default speed	3.3V	2 mA–20 mA	2, 4, 8, 12, 16, and 20 mA
	High speed	3.3V	4 mA–20 mA	4, 8, 12, 16, and 20 mA
	SDR12	1.8V	2 mA–10 mA	2, 4, 6, 8, and 10 mA
	SDR25	1.8V	4 mA–10 mA	4, 6, 8, and 10 mA
	SDR50	1.8V	4 mA–10 mA	4, 6, 8, and 10 mA
	DDR50	1.8V	4 mA–10 mA	4, 6, 8, and 10 mA
	SDR104	1.8V	6 mA–10 mA	6, 8, and 10 mA
CAN		3.3V	3.3V==>2 mA–20 mA	2, 4, 8, 12, 16, and 20 mA
		2.5V	2.5V ==> 2–16mA	2, 4, 6, 8, 12, and 16 mA
		1.8V	1.8V ==> 2–12mA	2, 4, 6, 8, 10, and 12 mA
		1.5V	1.5V ==> 2–8mA	2, 4, 6, and 8 mA
		1.2V	1.2V ==> 2–8mA	2, 4, 6, and 8 mA
QSPI		3.3V	3.3V => 8–20 mA	8, 12, 16, and 20 mA
		2.5V	2.5V => 8–16 mA	8, 12, and 16 mA
		1.8V	1.8V => 8–12 mA	8, 10, and 12 mA
		1.5V	1.5V => 8–10 mA	8 mA
		1.2V	1.2V => 6–8 mA	6 and 8 mA

Table 2-16. I/O Standard and Output Drive (continued)

Protocol	Speed Mode	LVCMOS Standard	Output Current Drive	Supported Out Drive Values
SPI	Initiator	3.3V	3.3V => 8–20 mA	8, 12, 16, and 20 mA
		2.5V	2.5V => 8–16 mA	8, 12, and 16 mA
		1.8V	1.8V => 8–12 mA	8, 10, and 12 mA
		1.5V	1.5V => 8–10 mA	8 mA
		1.2V	1.2V => 6–8 mA	6 and 8 mA
	Target	3.3V	3.3V => 8–20 mA	8, 12, 16, and 20 mA
		2.5V	2.5V => 8–16 mA	8, 12, and 16 mA
		1.8V	1.8V => 8–12 mA	8, 10, and 12 mA
		1.5V	1.5V => 8–10 mA	8 mA
		1.2V	1.2V => 6–8 mA	6 and 8 mA
MMUART	—	3.3V	3.3V => 2–20 mA	2, 4, 8, 12, 16, and 20 mA
		2.5V	2.5V => 4–16 mA	4, 6, 8, 12, and 16 mA
		1.8V	1.8V => 4–12 mA	4, 6, 8, 10, and 12 mA
I2C	Standard	3.3V	3.3V => 2–20 mA	2, 4, 8, 12, 16, and 20 mA
		2.5V	2.5V ==> 2–16mA	2, 4, 6, 8, 12, and 16 mA
		1.8V	1.8V => 2–10 mA	2, 4, 6, 8, and 10 mA
	Fast	3.3V	3.3V => 2–20 mA	2, 4, 12, 16, and 20 mA
		2.5V	2.5V ==> 2–16mA	2, 4, 6, 8, 12, and 16 mA
		1.8V	1.8V => 2–10 mA	2, 4, 6, 8, and 10 mA
Ethernet MAC(MDIO)	PHY Management Interface	3.3V	3.3V => 8–20 mA	8, 12, 16, and 20 mA
		2.5V	2.5V => 8–16 mA	8, 12, and 16 mA
		1.8V	1.8V => 8–12 mA	8, 10 and 12 mA
		1.5V	1.5V => 8–10 mA	8 mA
		1.2V	1.2V => 6–8 mA	6 and 8 mA
GPIO	—	3.3V	3.3V => 2–20 mA	2, 4, 8, 12, 16, and 20 mA
		2.5V	2.5V => 2–16 mA	2, 4, 6, 8, 12, and 16 mA
		1.8V	1.8V => 2–12 mA	2, 4, 6, 8, 10, and 12 mA
		1.5V	1.5V => 2–8 mA	2, 4, 6, and 8 mA
		1.2V	1.2V => 2–8 mA	2, 4, 6, and 8 mA

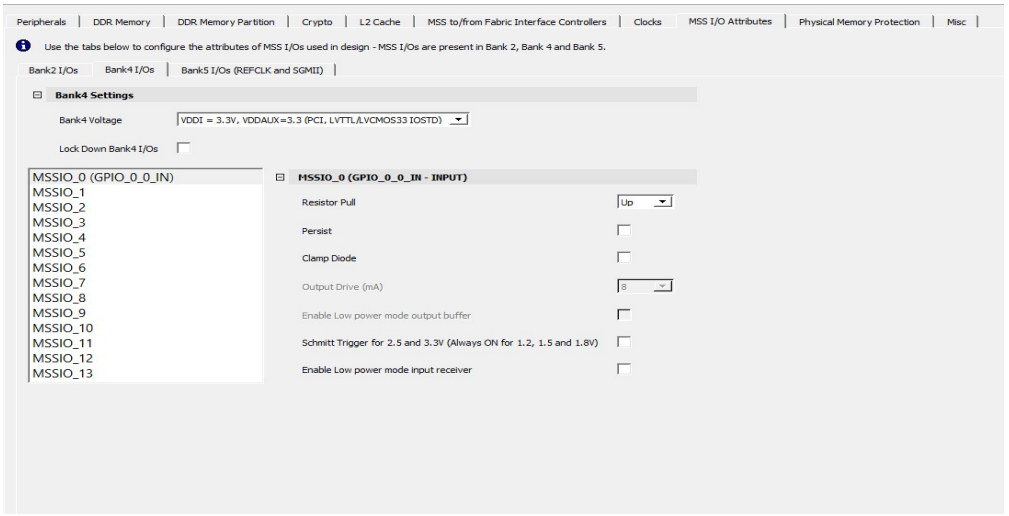
When a peripheral supports multiple speed modes, the following must be followed:

- I/O standard check must be specific for the peripheral and the speed mode is selected.
- Support for out drive values depends on the peripheral type, the speed mode, and the I/O standard.

2.3.8.2. Bank4 I/Os (Ask a Question)

The MSS I/Os are available across Bank 4. The **Bank4 I/Os** tab allows you to select the electrical characteristics of the MSS I/Os. Each MSS I/O along with the settings must be enabled one by one.

Figure 2-21. Bank4 I/Os Tab

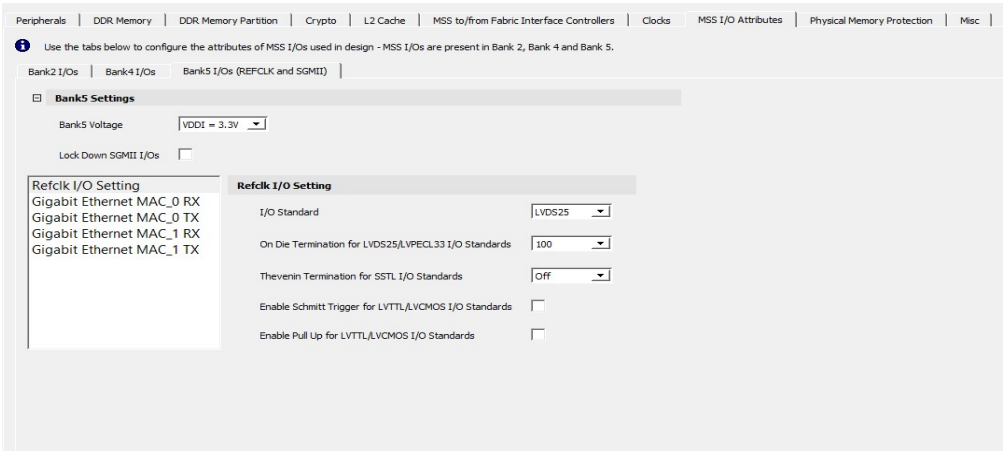


Important: Enable the Lock Down Bank4 I/Os option to lock all the Bank4 MSSIOs.

2.3.8.3. Bank5 I/Os (REFCLK and SGMII) (Ask a Question)

Using the Bank5 I/Os (REFCLK and SGMII) tab, you can select the electrical characteristics of the Bank5 I/Os, as shown in the following figure. The tool generates a warning in the log window for unsupported selections.

Figure 2-22. Bank5 I/Os (REFCLK and SGMII) Tab with RefClk I/O Setting Option Selected



Important: Enable the Lock Down SGMII I/Os option to lock all the SGMII I/Os.

PolarFire SoC supports two full-duplex SGMII channels (Channel0 and Channel1). Each channel has one RX and one TX. There are two input and two output I/Os that must be configured for SGMII, and all I/Os are differential.

The following are the **I/O Standard** options for the **Refclk I/O Setting**:

- LVTTL

- LVCMOS33
- LVCMOS25
- LVCMOS18
- SSTL25
- SSTL18
- LVDS25
- LVPECL33

SGMII Inputs

MAC_0 (Channel0) RX and MAC_1 (Channel1) RX are inputs and have the following options:

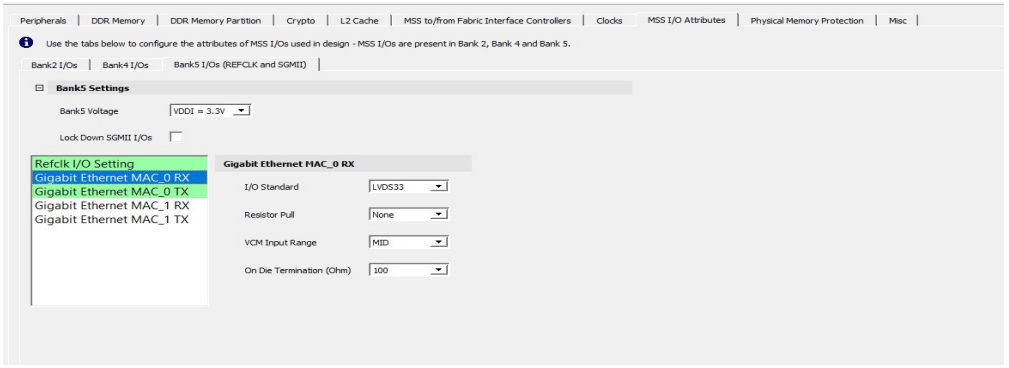
- I/O Standard

> **Important:** The IOSTD must match the bank voltage in the **Refclk I/O Setting** section. For example, if the bank 5 voltage VDDI is 3.3 V, you cannot set SGMII I/Os to any IOSTD, which is 2.5 V such as LVDS25, RSDS25, MINILVDS25, SUBLVDS25, PPDS25, and LCMDS25.

- Resistor Pull
- VCM Range
- On Die Termination (Ω)

The following figure shows the SGMII RX.

Figure 2-23. Bank5 I/Os (REFCLK and SGMII) Tab with Gigabit Ethernet MAC_0 RX Option Selected



SGMII RX Register Settings

The following table lists the Channel 0/Channel 1 RX register settings.

Table 2-17. Channel 0/1 RX Register Settings

GUI Labels/Parameter Name	Options
I/O Standard	LVDS33, LVDS25, RSDS33, RSDS25, MINILVDS33, MINILVDS25, SUBLVDS33, SUBLVDS25, PPDS33, PPDS25, LCMDS33, LCMDS25
Resistor Pull	None, Up, Down
VCM Input Range	MID, LOW
On Die Termination (Ohm)	OFF, 100

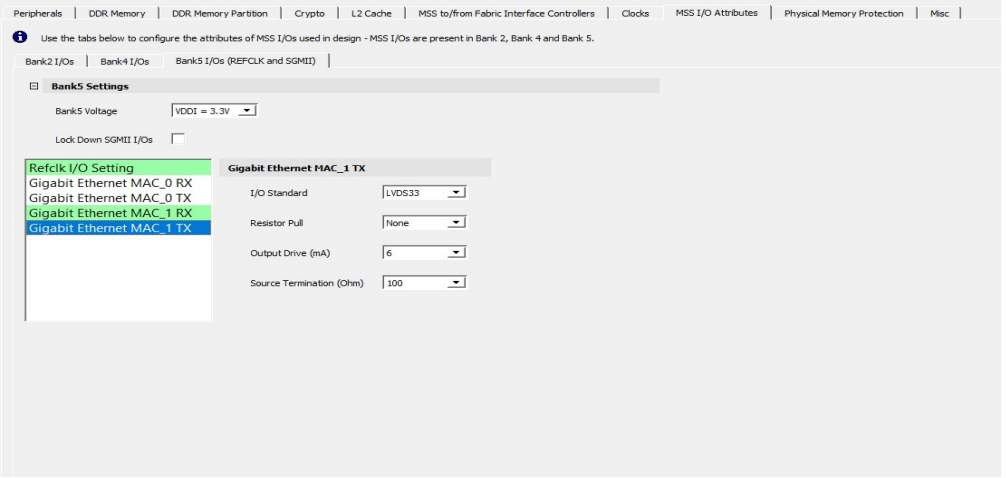
SGMII Outputs

MAC_0 (Channel0) TX and MAC_1 (Channel1) TX are outputs and have the following options:

- I/O Standard
- Resistor Pull
- Output Drive
- Source Termination (Ohm)

The following figure shows the SGMII TX.

Figure 2-24. Bank5 I/Os(REFCLK and SGMII) Tab with Gigabit Ethernet MAC_1 TX Option Selected



SGMII TX Register Settings

The following table lists the Channel 0/Channel 1 TX register settings.

Table 2-18. Channel 0 /1 TX Register Settings

GUI Labels/Parameter Name	Options
I/O Standard	LVDS33, LVDS25, RSDS33, RSDS25, MINILVDS33, MINILVDS25, SUBLVDS33, SUBLVDS25, PPDS33, PPDS25, LCMDS33, LCMDS25
Resistor Pull	None, Up, Down
Output Drive (mA)	1.5, 2, 3, 3.5, 4, 6
Source Termination (Ohm)	OFF, 100

SGMII Output I/O Standard Settings

Based on the selected I/O standards, you must enforce the following DRC checks:

Table 2-19. SGMII Output DRC Check

I/O_TYPE	Direction	Legal Output DRIVE Settings (mA)
LVDS33	Output	6, 4, 3.5, 3
LVDS25	Output	6, 4, 3.5, 3
RSDS33	Output	4, 3, 2, 1.5
RSDS25	Output	4, 3, 2, 1.5
MINILVDS33	Output	6, 4, 3.5, 3
MINILVDS25	Output	6, 4, 3.5, 3
SUBLVDS33	Output	3, 2, 1.5, 1
SUBLVDS25	Output	3, 2, 1.5, 1

Table 2-19. SGMII Output DRC Check (continued)

I/O_TYPE	Direction	Legal Output DRIVE Settings (mA)
PPDS33	Output	4, 3, 2, 1.5
PPDS25	Output	4, 3, 2, 1.5
LCMDS33	Output	6, 4, 3.5, 3
LCMDS25	Output	6, 4, 3.5, 3

I/O Standard and Supported Output Drive

Voltage selection for Bank 5 must match the I/O Standard selected for TX and RX in both channels.

Example 2-1.

Bank5 Voltage selection -> VDDI = 3.3V -> LVDS33 is legal but not LVDS25

Table 2-20. Legal Values/Settings for I/O_TYPE/Output Drive Combination

I/O_TYPE	Legal Output DRIVE Settings (mA)
LVDS33	6, 4, 3.5, 3
LVDS25	6, 4, 3.5, 3
RSDS33	4, 3, 2, 1.5
RSDS25	4, 3, 2, 1.5
MINILVDS33	6, 4, 3.5, 3
MINILVDS25	6, 4, 3.5, 3
SUBLVDS33	3, 2, 1.5, 1
SUBLVDS25	3, 2, 1.5, 1
PPDS33	4, 3, 2, 1.5
PPDS25	4, 3, 2, 1.5
LCMDS33	6, 4, 3.5, 3
LCMDS25	6, 4, 3.5, 3

2.3.8.4. Bank2 and Bank4 I/Os Related to SD and eMMC Muxing (Ask a Question)

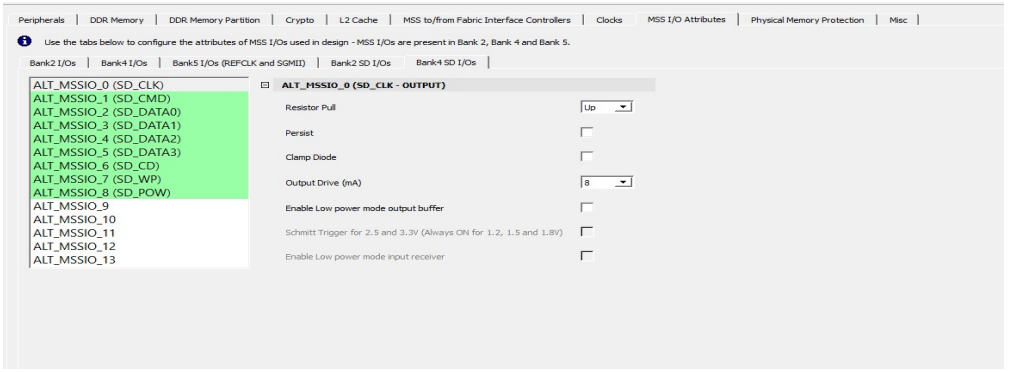
The eMMC and SD peripherals use the same MSS I/Os, so both peripherals cannot be active at the same time. However, the PolarFire SoC MSS Configurator allows you to configure the electrical characteristics of the MSS I/Os related to both peripherals when **eMMC and SD muxing** is enabled in the **Peripherals** tab, where one of the peripherals (eMMC or SD) is active at power-up and the other peripheral is not active at power-up. The MSS I/Os related to a peripheral that is active at power-up is listed in **Bank2 I/Os** tab and **Bank4 I/Os** tab. MSS I/Os related to a peripheral that is not active at power-up is shown as follows:

In the highlighted tabs, you might be able to select the electrical characteristics of eMMC or SD MSS I/Os only (electrical characteristics of MSS I/Os related to any other peripherals are grayed-out).

- If **eMMC and SD muxing** is selected as **Enabled (eMMC active at Power-Up)** in **Peripherals** tab, the highlighted tabs will be shown to the user.

Important: The eMMC MSS I/Os are listed under Bank2/Bank4 I/Os tabs, and SD MSS I/Os are listed in the highlighted tabs.

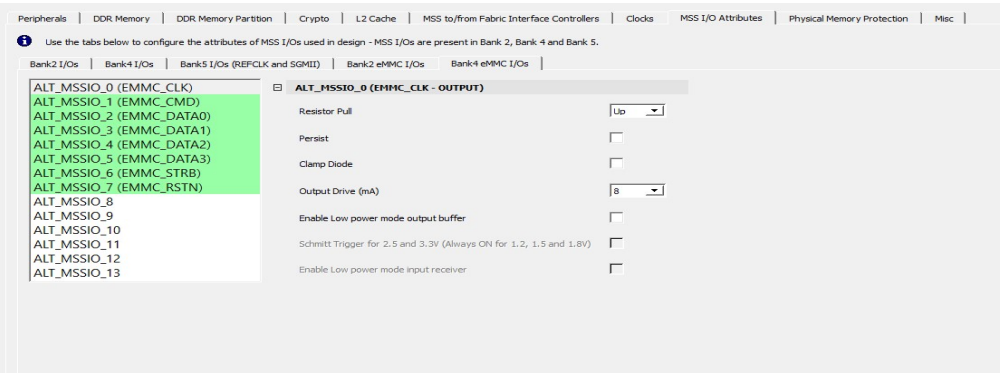
Figure 2-25. Bank2 and Bank4 SD I/Os Tabs



- If **eMMC and SD muxing** is selected as **Enabled (SD active at Power-Up)** in **Peripherals** tab, the highlighted tabs will be shown to the user.

Important: The SD MSS I/Os are listed under Bank2/Bank4 I/Os tabs, and eMMC MSS I/Os are listed in the highlighted tabs.

Figure 2-26. Bank2 and Bank4 eMMC I/Os Tabs



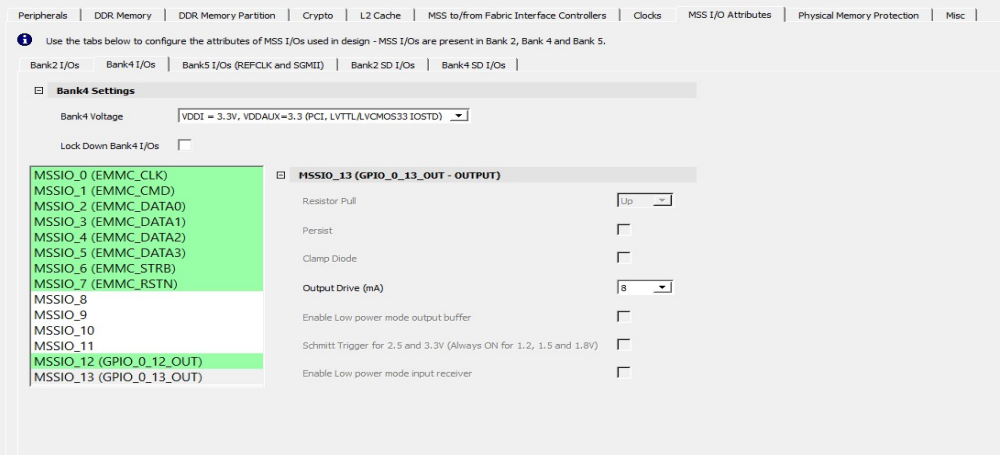
Important: When **eMMC and SD muxing** is enabled, the user must ensure that the required embedded software driver and fabric design support is available to dynamically switch between eMMC and SD peripherals.

When **eMMC and SD muxing** is enabled, MSSIO PADs can be configured as Pull-Up or Pull-Down by selecting GPIOs as **Static High** or **Static Low**. When **Static High** or **Static Low** is selected for a GPIO in Bank 4 or Bank 2, all the I/O attributes of the corresponding MSSIO are greyed out except **Output Drive**. **Resistor Pull** is set to **Up** when **Static High** is selected and to **Down** when **Static Low** is selected by default for the corresponding MSSIOs in **Bank2 I/Os** and **Bank4 I/Os** tab and vice versa in the **Bank2 eMMC(SD) I/Os** and **Bank4 eMMC(SD) I/Os** tab.

For example: when **Static High** is selected for `GPIO_0_13` in the **Peripherals** tab, the **MSSIO I/O Attributes** tab will be setup as follows:

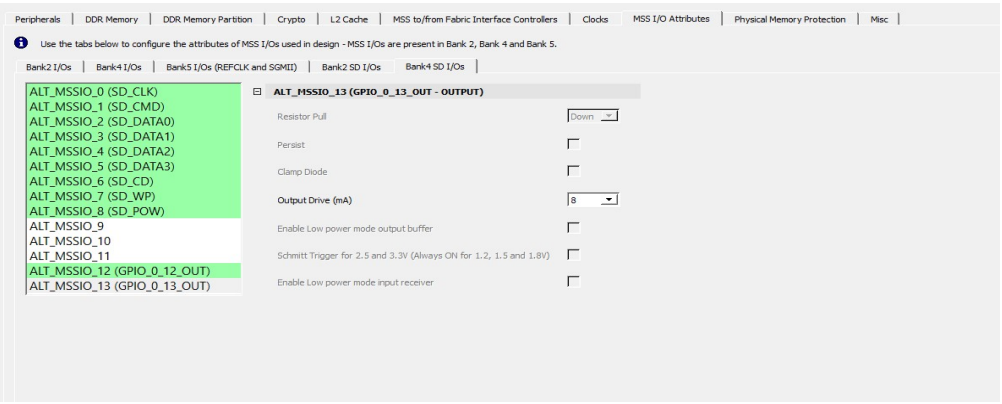
- Bank4 I/Os settings are shown in the following figure.

Figure 2-27. Bank4 I/O Settings



- Alternate Bank4 I/Os settings are shown in the following figure.

Figure 2-28. Alternate Bank4 I/Os Settings



2.3.9. Physical Memory Protection (Ask a Question)

The Physical Memory Protection (PMP) prevents a process (running on a RISC-V Processor) or an initiator (FPGA Fabric) from accessing memory that has not been allocated to it. RISC-V system has PMP unit, which provides control registers for each processor to allow physical memory access privileges (read, write, execute) to be specified for each physical memory region.

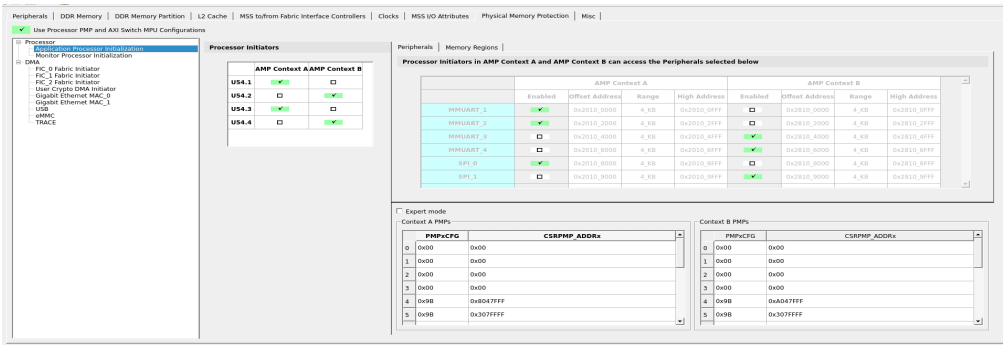
For more information on how PMP works on RISC-V® processors, refer the RISC-V PMP - With PFSoC Examples page.

Similarly, the AXI Switch has Memory Protection Unit (MPU) block which provides register control to setup memory access regions for FPGA initiators.

Application Processor Initialization

The following figure shows the Application Processor Initialization tab.

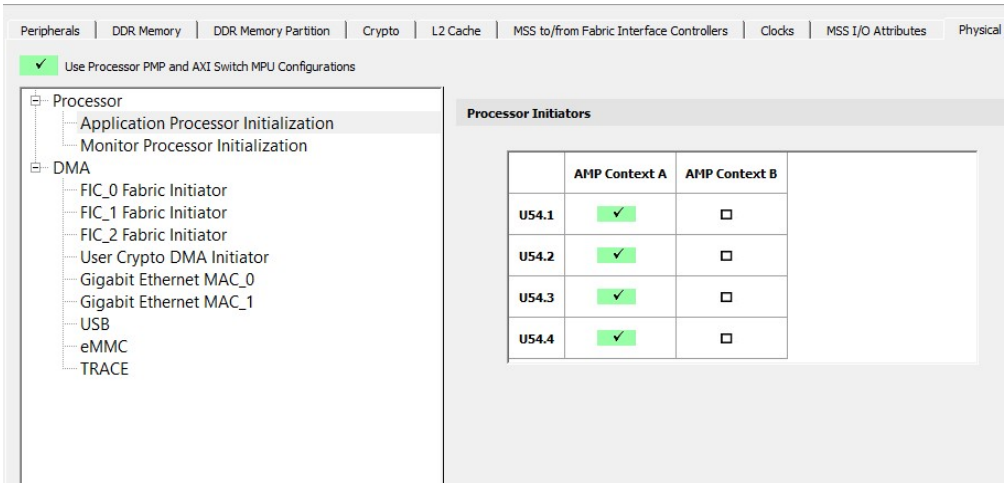
Figure 2-29. Application Processor Initialization Tab



Processor Initiators

Four CPU initiators can be enabled in one of the two Asymmetric Multi Processing (AMP) contexts. CPU initiators can access both CPU and Peripherals. However, they cannot be enabled in both Context A & Context B.

Figure 2-30. Processor Initiators



Processor Initiators in Context A and Context B can access the following selected Peripherals

The AMP Context A is assigned to AHB0 bus interface and AMP Context B is assigned to AHB1 bus interface. Peripherals can be enabled in either Context A or in Context B. The range and base address for the peripherals are populated in Graphical User Interface and are not editable. The base address will be different for peripherals that are on dual AHB bus interfaces for Context A and Context B.

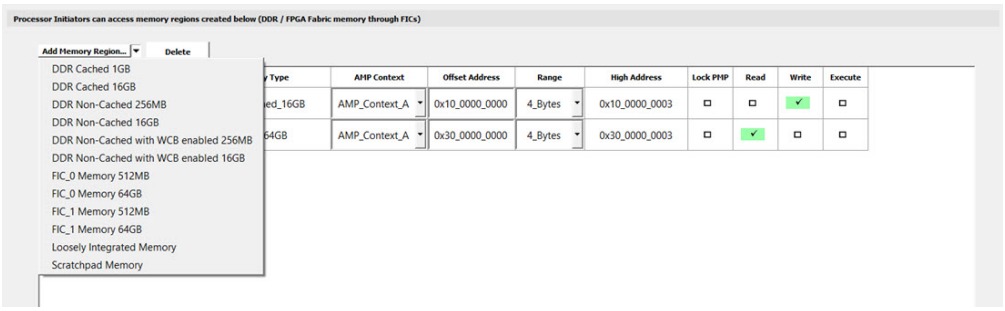
Figure 2-31. Processor Initiators in Context A and Context B Accessing the Peripherals

	AMP Context A				AMP Context B		
	Enabled	Offset Address	Range	High Address	Enabled	Offset Address	Range
MMUART_1	✓	0x2010_0000	4_KB	0x2010_0FFF	☐	0x2810_0000	4_KB
MMUART_2	✓	0x2010_2000	4_KB	0x2010_2FFF	☐	0x2810_2000	4_KB
MMUART_3	☐	0x2010_4000	4_KB	0x2010_4FFF	✓	0x2810_4000	4_KB
MMUART_4	☐	0x2010_6000	4_KB	0x2010_6FFF	✓	0x2810_6000	4_KB
SPI_0	✓	0x2010_8000	4_KB	0x2010_8FFF	☐	0x2810_8000	4_KB
SPI_1	☐	0x2010_9000	4_KB	0x2010_9FFF	✓	0x2810_9000	4_KB
I2C_0	✓	0x2010_A000	4_KB	0x2010_AFFF	☐	0x2810_A000	4_KB
I2C_1	☐	0x2010_B000	4_KB	0x2010_BFFF	✓	0x2810_B000	4_KB
CAN_0	✓	0x2010_C000	4_KB	0x2010_CFFF	☐	0x2810_C000	4_KB
CAN_1	☐	0x2010_D000	4_KB	0x2010_DFFF	✓	0x2810_D000	4_KB
Gigabit Ethernet MAC_0	✓	0x2011_0000	8_KB	0x2011_1FFF	☐	0x2811_0000	8_KB

Processor Initiators can access memory regions created as follows (DDR/FPGA Fabric memory through FICs)

DDR memory appears at several address ranges depending on whether it is cached, non-cached, or access through a Write Combine Buffer (WCB). WCB improves performance (by combining multiple writes to the same address into a single write) for sequential accesses. Each AMP context needs to specify how much DDR memory of each type it needs. Some DDR memories may be shared between AMP Context to pass data. User can create protection for memory region accessed by processors by clicking on the **Add Memory Region...** button. User can delete any memory region by selecting the memory region and clicking **Delete** button. The following figure shows the memory regions available to Processor Initiators.

Figure 2-32. Memory Regions Available to Processor Initiators



The following table lists different types of memory regions that user can create.

Table 2-21. Available Memory Region

Memory Type	Memory Size	Address Size	Address Range
DDR Cached	512 MB	32-bit	0x80000000 - 0xBFFFFFFF
	16 GB	64-bit	0x10_00000000 - 0x13_FFFFFFFF
DDR Non-Cached	256 MB	32-bit	0xC0000000 - 0xCFFFFFFF
	16 GB	64-bit	0x14_00000000 - 0x17_FFFFFFFF
DDR Non-Cached with WCB enabled	256 MB	32-bit	0xC0000000 - 0xCFFFFFFF
	16 GB	64-bit	0x14_00000000 - 0x17_FFFFFFFF
FIC_0 Memory	512 MB	32-bit	0x60000000 - 0x7FFFFFFF
	64 GB	64-bit	0x20_00000000 - 0x2F_FFFFFFFF
FIC_1 Memory	512 MB	32-bit	0xE0000000 - 0xFFFFFFFF
	64 GB	64-bit	0x30_00000000 - 0x3F_FFFFFFFF
Loosely Integrated Memory	—	—	Start Address is 0x0800_0000
Scratch	—	—	Start Address is 0x0A00_0000

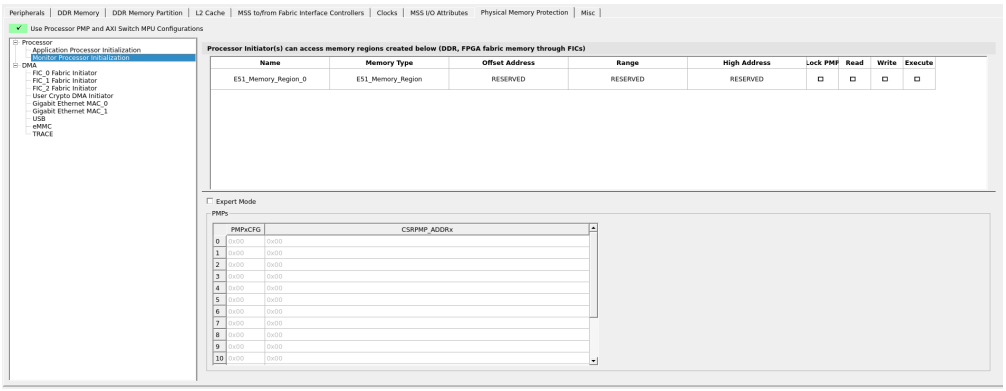
When the values are modified for **Peripherals** and **Memory Regions**, the same gets updated dynamically in the PMPxCFG and CSRPMP_ADDx pairs in both the Context A and Context B tables.

Monitor Processor Initialization

The Monitor Processor Initialization view has a Monitor Processor Initialization tab with a default region, E51_Memory_Region_0. It can only be modified in the Expert Mode.

The following figure shows the Monitor Processor Initialization tab.

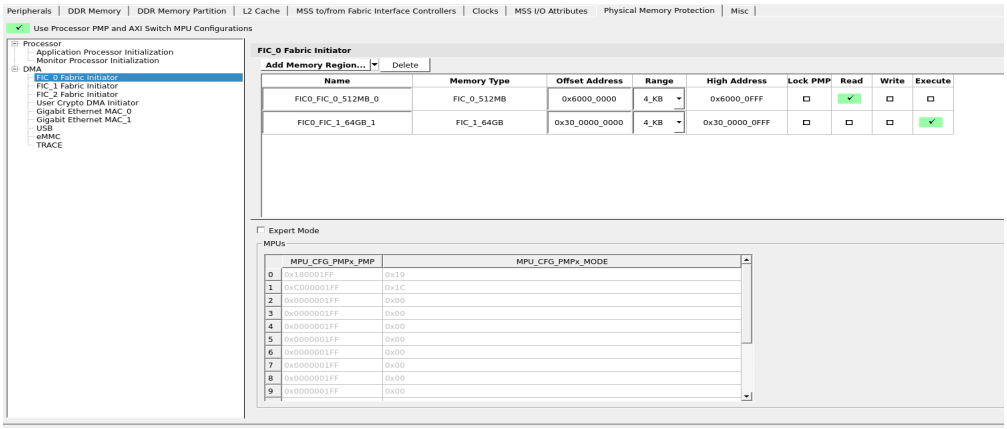
Figure 2-33. Monitor Processor Initialization Tab



Direct Memory Access

Direct Memory Access (DMA) provides FPGA (Non-CPU) Initiators read/write/execute access to the Memory subsystem and Fabric Memory. Users can create protection for memory regions accessed by FPGA Initiators by clicking any one of the FPGA Initiators and clicking the **Add Memory Region...** button. User can delete any memory region by selecting the memory region and clicking **Delete** button.

Figure 2-34. DMA Tab



The following table lists the different types of memory regions that user can create.

Memory Type	Memory Size	Address Size	Address Range
DDR Non-Cached	256 MB	32-bit	0xC0000000 - 0xCFFFFFFF
	16 GB	64-bit	0x14_00000000 - 0x17_FFFFFFFF
FIC_0 Memory	512 MB	32-bit	0x60000000 - 0x7FFFFFFF
	64 GB	64-bit	0x20_00000000 - 0x2F_FFFFFFFF
FIC_1 Memory	512 MB	32-bit	0xE0000000 - 0xFFFFFFFF
	64 GB	64-bit	0x30_00000000 - 0x3F_FFFFFFFF
FIC_3 Memory	512 MB	32-bit	0x40000000 - 0x5FFFFFFF
User Crypto Memory	128 KB	32-bit	0x22000000 - 0x2201FFFF

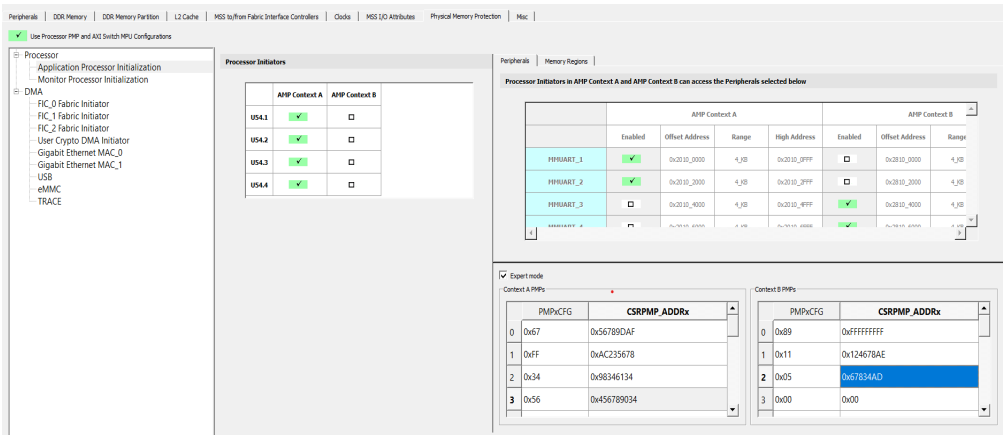
Expert Mode

Expert Mode is a specialized feature in the configurator intended for advanced users who require direct control over PMP and MPU configurations. It allows manual modification of these settings, overriding the automatic updates and calculations normally performed by the application. However, the Peripherals and Memory Regions tables do not update dynamically in this mode, nor can they be edited.

Expert Mode is applicable for the **Application Processor Initialization, Monitor Processor Initialization** and **DMA** tabs.

The following figure shows the **Expert Mode** in use in the **Application Processor Initialization** tab.

Figure 2-35. Expert Mode



When the **Expert Mode** is disabled, all changes made are discarded and the values from the latest entries in the Initiator tables are displayed.

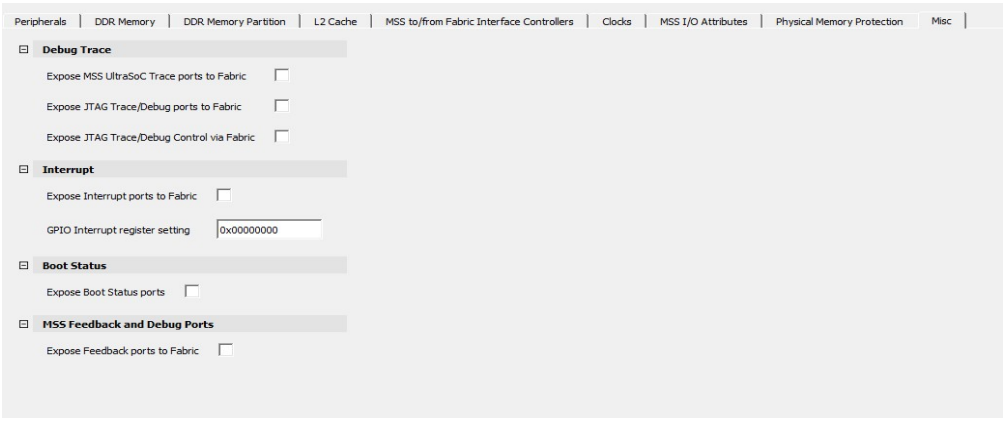
Note: In the Normal mode, when the **Expert Mode** option is unchecked, the PMP and MPU configation tables are read only. Any changes made in the Peripherals and Memory Regions tables are automatically calculated and reflected in the PMP and MPU tables.

2.3.10. Misc (Ask a Question)

Use the **Misc** tab to enable the following options:

- Trace functionality
- JTAG (Debug) functionality
- Interrupts to/from MSS
- Configuring GPIO Interrupt Register
- Exposing Boot Status ports
- Exposing feedback ports to fabric

Figure 2-36. Misc Tab



By default, these options are marked as **Unused**. When any of the options are enabled, the corresponding ports are exposed on the MSS block (see the following figure).

The **Debug Trace** options enable hardware trace support in the Microprocessor Subsystem (MSS). When you enable trace functionality option in the **Misc** tab, you are instructing the tool to expose the MSS trace-related I/O pins/ports in the generated MSS component. These ports can then be

routed to FPGA fabric I/Os or dedicated pins so that external debug/trace tools or internal logic could use them.

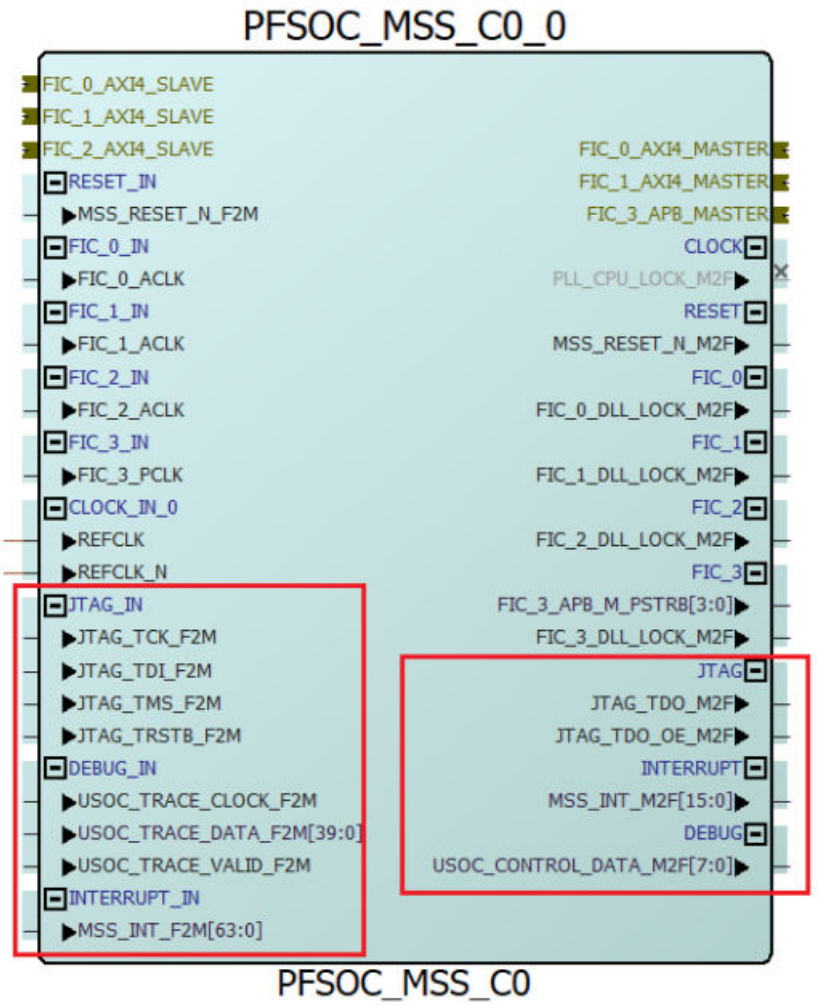
The following options are available under **Debug Trace** option:

- **Expose MSS UltraSoC Trace Ports to Fabric** enables the internal debug/trace infrastructure to present non-JTAG debug interfaces toward the fabric.
- **Expose JTAG Trace/Debug Ports to Fabric** enables the MSS internal debug and trace endpoints to be routable toward the FPGA fabric via a non-JTAG interface.
- **Expose JTAG Trace/Debug Control via Fabric** determines whether the FPGA fabric can control the MSS debug and trace logic. When you enable it, the FPGA fabric is allowed to act as a debug controller for the MSS, using internal control buses instead of an external JTAG probe.

The **Interrupt** options control whether interrupt lines between the FPGA fabric and the MSS are exposed as ports in the generated MSS component. The following options are available under **Interrupt** option:

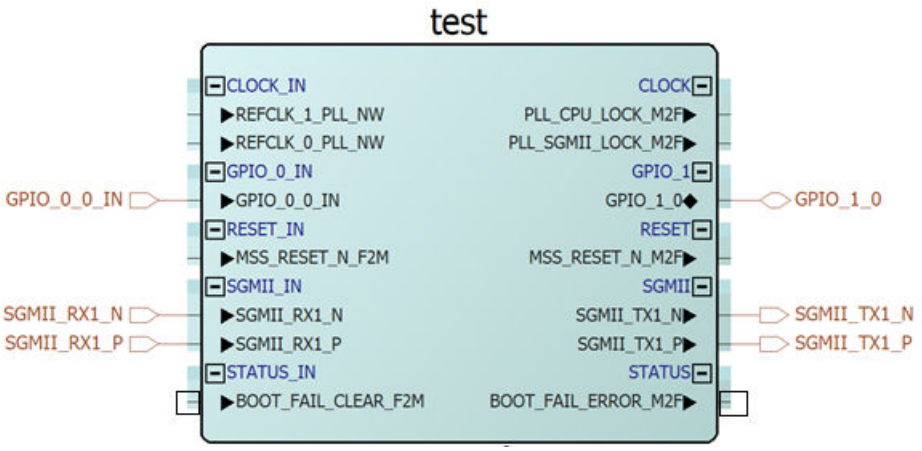
- **Expose Interrupt ports to Fabric** makes UltraSoC trace outputs from the MSS available to the FPGA fabric via FIC, so the fabric can receive the trace data. It does not generate trace or provide a sink—just exposes the ports.
- **GPIO Interrupt register setting** instantiates the interrupt logic for GPIO pins inside the MSS. This option connects the GPIO interrupt outputs to the MSS interrupt controller and allows each GPIO pin to be configured for edge/level sensitivity via registers.

Figure 2-37. PFSOC_MSS_C0_0 when Debug Trace Options and Interrupt Options Enabled



Boot Status: When **Expose Boot Status ports** option is selected, the ports `BOOT_FAIL_CLEAR_F2M` and `BOOT_FAIL_ERROR_M2F` are exposed as shown in the following figure. Both the signals typically represent binary states through voltage levels and are generally synchronous with the MSS clock.

Figure 2-38. PFSOC_MSS_C0_0 when Boot Status Option Enabled

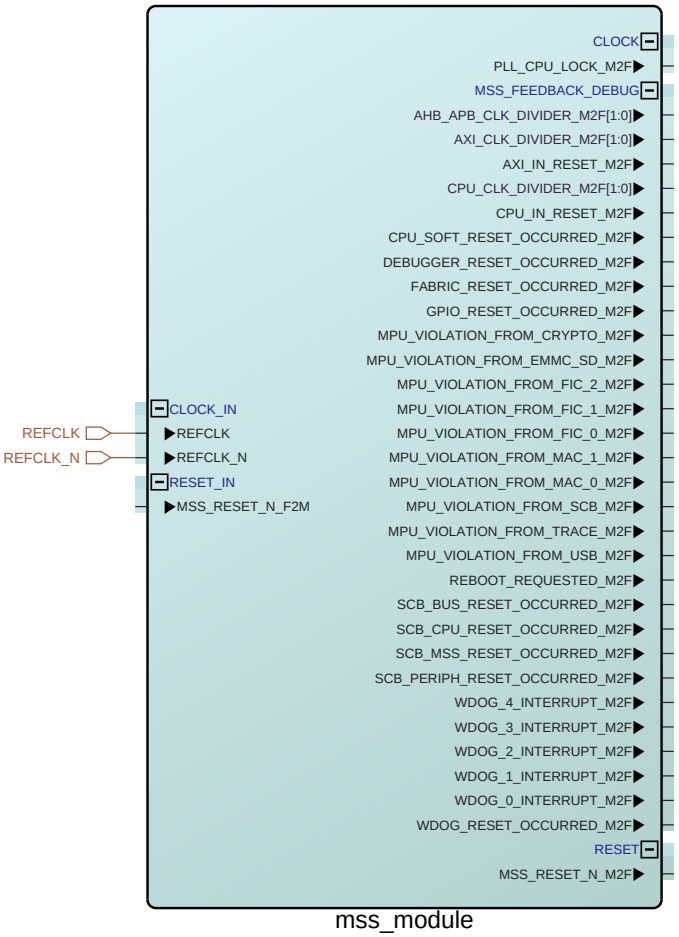


BOOT_FAIL_ERROR_M2F is a signal from the MSS to the FPGA fabric that indicates a boot failure has occurred. When the MSS detects the failure, it sets this signal high and informs the fabric to take action or log the issue.

BOOT_FAIL_CLEAR_F2M is a signal from the FPGA fabric to inform the MSS that the boot failure has been addressed. When the FPGA fabric handles the issue, it sets the signal high telling the MSS to clear the boot failure status.

MSS Feedback and Debug Ports: This option is only available for production devices. If selected, a group of MSS_FEEDBACK_DEBUG ports are exposed as shown in the following figure.

Figure 2-39. MSS Module With MSS_FEEDBACK_DEBUG Ports Exposed



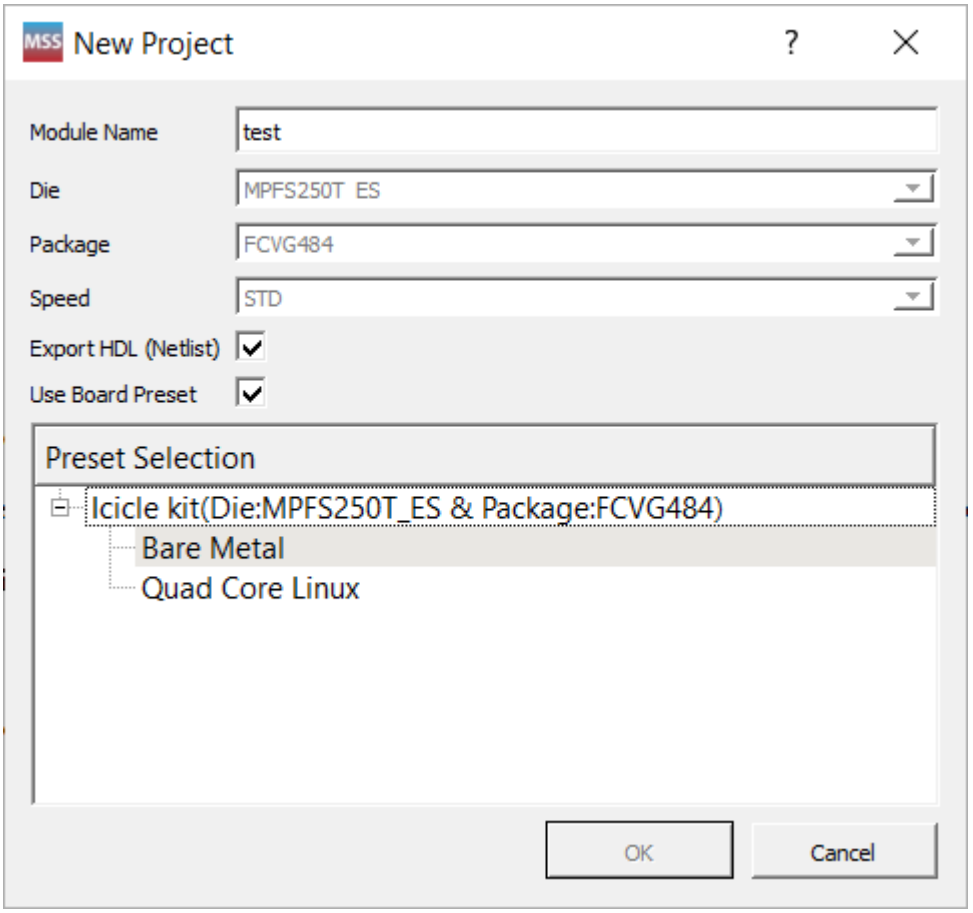
Important: In a Libero project, when System Controller Suspend Mode is enabled (**Project** > **Project Settings** > **Device settings**), the PFSOC_SCSM macro must be instantiated in the user design and the REBOOT_REQUESTED_M2F pin of MSS must be connected to the SC_WAKE pin of PFSOC_SCSM macro to wake up the system controller temporarily so it can reboot the MSS during normal operation.

3. Creating a Project and Configuring MSS (Ask a Question)

To create a project and configure MSS:

1. Launch the PolarFire SoC MSS Configurator (`pfsoc_mss`) using one of the following ways:
   - Libero SoC installation directory
   - Standalone MSS installation area
   - Windows Start menu
2. Create a new project using **Project > New**. The New Project dialog is displayed.

Figure 3-1. MSS — Module Name Dialog Box



3. Enter a module name (for example, `PFSOC_MSS_C0`), and then select the appropriate die, package, and speed. The module name you enter appears in the following places:
   - File names of the PolarFire SoC MSS Configurator generated outputs at the specified output/ generation directory
   - MSS component file (`<module_name>.cxz`)
   - MSS XML configuration file (`<module_name>_mss_cfg.xml`)
   - MSS configuration file corresponding to the current MSS configuration that is generated (`<module_name>.cfg`)
   - MSS configuration report file (`<module_name>_Report.html`)
   - Component/module name of the MSS component (`cxz`) that can be imported to a Libero SoC project

4. The **Export HDL (Netlist)** option controls whether the HDL output is generated for the MSS. When enabled, the HDL representation of the MSS, that includes timing shell information, is generated and placed in the project's output/generation directory along with other generated artifacts. This option is cleared by default.
   In Batch mode, this option can be used as follows:

   ```
   -EXPORT_HDL true | false
   ```

5. The **Use Board Preset** option enables you start a new MSS project using a predefined configuration (.cfg preset) that matches a specific evaluation board or known hardware platform. Currently, the following Icicle Kit presets are available for selection.
   - Bare Metal
   - Quad Core Linux

   Presets for Icicle Kit

   When you create a New Project, you can import one of the available presets for Icicle kit. These presets are staged in data folder and are in 'CFG' format. All the parameter/values from the CFG file are loaded, except for the following four parameters:
   - Module Name
   - Die
   - Package
   - Speed

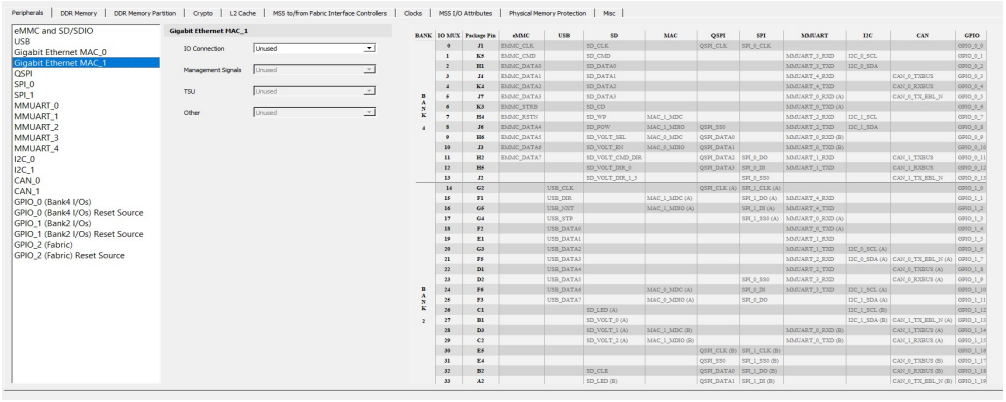
   User-selected values are used for Module Name, Die, Package, and Speed parameters in the GUI. This is done to facilitate changing Module Name/Die/Package/Speed (from the Icicle kit preset) to meet users need.

   The default speed grade is STD including for the Icicle Kits. If you open a previous release `.cfg`, which does not have speed grade (PolarFire SoC MSS Configurator v2021.2 or earlier) in v2021.3, it has STD as the default speed grade.

   The list of presets are shown using a tree widget. By default, the 'Default Configuration' preset is selected in GUI and user must explicitly select one of the presets for Icicle kit to load them. Once a preset is selected, users cannot edit them using **Edit Settings** option as the preset tree widget is unavailable in the **Edit Settings** dialog box.

   The following figure shows the MSS configurator tabs.

Figure 3-2. MSS Configurator Tabs



6. Configure **Clocks**, **Fabric Interface Controllers**, **I/O Configuration**, **DDR Memory**, and **Misc settings**.
7. Click the **Save** option to save the MSS configuration to a `.cfg` file.
8. From the **Save MSS Configuration** dialog box:

- Browse to a directory and create a folder. For example, create `C:\Microsemi\PFSOC_MSS_Configuration`.
- Enter a file name (for example, `PFSOC_MSS_C0)` and click **Save**.
  Note: The file name you enter is for the stand-alone MSS project only and is not used as the component name.

The MSS Configuration is created and saved to the file specified and the Log window shows the following message: `INFO: Successfully saved MSS configuration in C:/Microsemi/PFSOC_MSS_Configuration/PFSOC_MSS_C0.cfg file`.

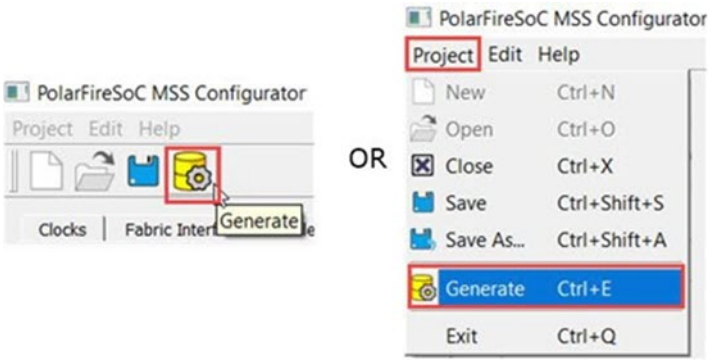
4. Generating, Importing, and Exporting the MSS Component (Ask a Question)

The following sections describe the steps for generating, importing, and exporting the MSS component.

4.1. Generating the MSS Component and Report (Ask a Question)

To generate the MSS component, use the **Generate** option (see the following figure).

Figure 4-1. Generate Option



The configuration file (`module_name.xml`) required for the firmware project and the configuration report file (`module_name.html`) are also generated at this time.

The Log window shows the following messages indicating the generated files:

```
INFO: Successfully generated MSS configuration report to 'C:/Microsemi/
PFSOC_MSS_Configuration\PFSOC_MSS_C0_Report.html'
```

```
INFO: Successfully generated MSS component file to 'C:/Microsemi/PFSOC_MSS_Configuration/
PFSOC_MSS_C0.cxz'
```

The report file (`module_name.html`) consists of following sections:

- Design Information – This section consists of design parameters like device family name, die, package, configurator version, and the date the report was generated.
- FPGA Fabric – This section mentions whether FPGA Fabric programming is required or not.
- Fabric Interface Controllers – Consists information about status of the interface controllers.
- Peripherals – Contains information about which peripherals are being used or unused.
- DDR Memory – Shows the memory type.
- List of Ports – Depicts information about all the ports with direction.
- I/O REFCLK Port Settings – Shows all the information about Reference clock ports.
- MSSIO Port Settings – Shows all the information about MSSIO ports.
- DDRIO Port Settings – Shows all the information about DDRIO ports.
- SGMII I/O Port Settings – Shows all the information about SGMII ports.

Figure 4-2. Configuration Report for PolarFire SoC MSS Configurator

Design Information

Design Parameter Name	Design Parameter Value
Family	PolarFireSoC
Die	MPFS250T_ES
Package	FCVG484
Version	2021.3
Date	Wed Nov 10 11:06:25 2021

FPGA Fabric

FPGA Fabric Programming	Required

MSS to/from Fabric Interface Controllers

Interface Controller Name	Enabled
FIC_0 AXI4 Initiator Interface	true
FIC_0 AXI4 Target Interface	true
FIC_1 AXI4 Initiator Interface	false
FIC_1 AXI4 Target Interface	true
FIC_2 AXI4 Target Interface	true
FIC_3 APB Initiator Interface	true

Peripherals

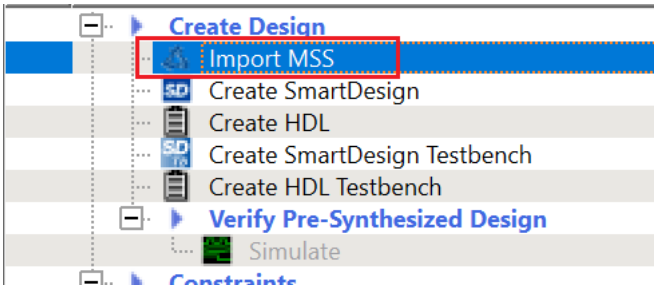
Peripheral Name	Enabled
eMMC	MSSIO_B4
USB	MSSIO_B2
SD/SDIO	MSSIO_B4
Gigabit Ethernet MAC_0	SGMII_IO_B5
Gigabit Ethernet MAC_1	SGMII_IO_B5
QSPI	MSSIO_B2
SPI_0	FABRIC
SPI_1	UNUSED
MMUART_0	FABRIC
MMUART_1	FABRIC
MMUART_2	FABRIC
MMUART_3	FABRIC
MMUART_4	FABRIC
I2C_0	FABRIC
I2C_1	MSSIO_B2_B
CAN_0	FABRIC
CAN_1	MSSIO_B2_B
GPIO_0_0	UNUSED
GPIO_0_1	UNUSED
GPIO_0_2	UNUSED
GPIO_0_3	UNUSED
GPIO_0_4	UNUSED
GPIO_0_5	UNUSED

4.2. Importing the MSS CXZ File to Libero SoC (Ask a Question)

To import the `PFSOC_MSS_C0.cxz` file:

1. Use the **Import MSS** option shown in the following figure.

Figure 4-3. Import MSS to Libero



2. From Design Hierarchy, drag the MSS component to SmartDesign canvas.
3. Build the hierarchy.

Note: Any changes required in the MSS configuration must be performed in the PolarFire SoC MSS Configurator, and the updated `MSS CXZ` file must be re-imported and used in Libero SmartDesign.

4.3. Importing the MSS XML File to SoftConsole (Ask a Question)

Copy the XML file from:

```
<$Directory>:/Microsemi/PFSOC_MSS_Configuration/PFSOC_MSS_C0_mss_cfg.xml
```

to:

```
<$Installation
Directory>:\Microchip\<$SoftConsole_Workspace>\Project_Name\src\platform\config\xml
```

Note: This step can also be performed using the **Import** option from SoftConsole.

4.4. Exporting the FPGA Design Hardware Platform Information (Ask a Question)

When using PolarFire SoC, the overall application runs an embedded software application on the RISC-V cores that may use the FPGA fabric to expand the number of I/O peripherals, accelerate software functions using FPGA logic, or control FPGA fabric functions. In these cases, the processor communicates with the FPGA fabric via the MSS Fabric Interface Controllers (FIC) and interrupt ports. The embedded software application must contain the following information to establish this communication properly:

- Fabric blocks like LSRAM, DMA Controller, and PCIe® are connected to the AXI interconnect IP on the Fabric side. MSS communicates with these fabric blocks via Fabric Interface Controllers, which connects to the AXI Interconnect IP. The memory addresses of these fabric blocks are specified in the AXI Interconnect IP Configurator. These memory addresses must be specified in the software application.
- In the Libero SoC design, the user must drive the required MSS interrupt ports and other interrupts can be grounded. The corresponding Interrupt Request (IRQ) handler routines must be invoked in the software application for interrupt handling.

Libero SoC tool does not export the FPGA fabric peripheral memory map, interrupt mapping, or peripheral clock frequencies. Therefore, add this information manually in your embedded software projects. For example, if fabric blocks such as LSRAM and DMA Controller are used in the design and interfaced with the MSS through a FIC, then the memory addresses of these fabric blocks must be specified in the user application code for accessing them from MSS.

5. Simulating an FPGA Design Interacting with MSS (Ask a Question)

The MSS simulation model has been designed to verify that the connectivity to the MSS has been properly established with the FPGA fabric logic.

The MSS simulation model can be used to verify:

- The Fabric—MSS connectivity using the Fabric Interface Controllers (FICs).
- The Fabric—MSS interrupt (M2F and F2M) interface.

For information about how to set up and run the simulation for the PolarFire SoC MSS, see MSS Simulation User Guide for PolarFire SoC.

6. Programming the Application Bitstream (Ask a Question)

To program the application bit stream:

1. Use Libero SoC or FlashProExpress to program the FPGA fabric array, sNVM, eNVM and any security settings.
2. Use Libero SoC to program any eNVM client.

Note: SoftConsole must be used to program the Boot mode.

Alternatively, you can also perform the following steps:

1. Use SoftConsole to program the eNVM with the First Stage Boot image.
   a. Select the project you want programmed to eNVM in SoftConsole's **Project Explorer** pane.
   b. Click the **PolarFire SoC Boot Mode 1** external tool.

Programming progress messages appear in the Console.

For more information, see PolarFire SoC Software Development and Tool Flow User Guide.

7. Sample Project (Ask a Question)

For PolarFire SoC Icicle Kit reference design and supporting files, see PolarFire SoC Icicle Kit Reference Design GitHub repository.

8. References (Ask a Question)

See the following reference documents for further details:

- Configuration of the MSS clocks.
  - For detailed information about the MSS clocking features, see PolarFire Family Clocking Resources User Guide.
- Configuration of the MSS interfaces to the FPGA fabric.
  - For detailed information about the MSS Fabric Interface Controller (FIC) features, see PolarFire SoC MSS Technical Reference Manual.
- Selection and assignment of the MSS peripherals to the MSS dedicated I/Os and/or the FPGA fabric dedicated peripheral interfaces.
  - For detailed information about the MSS Peripherals features, see PolarFire SoC MSS Technical Reference Manual.
- Configuration of the MSS Bank voltages and I/O standards and attributes.
  - For detailed information about the MSS Banks and I/Os features, see PolarFire Family I/O User Guide.
- Configuration of the MSS DDR memories (DDR3/L, DDR4, LPDDR3, and LPDDR4).
  - For detailed information about the MSS DDR4, DDR3, LPDDR3, and LPDDR4 features, see PolarFire Family Memory Controller User Guide.
- Configuration of the MSS debug features.
  - For detailed information about the MSS debug features, see PolarFire SoC MSS Technical Reference Manual.

9. Revision History (Ask a Question)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
U	06/2026	The following changes are made in this revision: • Reordered the chapters to match the MSS Configurator GUI. • Added detailed descriptions for all the options available in the DDR Memory tab. • Added information about the **Export HDL** option in the Creating a Project and Configuring MSS section.
T	02/2026	The following change is made in this revision: • In the section Misc, added descriptions for **Debug Trace** and **Interrupt** options in the **Misc** tab.
S	02/2026	The following change is made in this revision: • Added the I/O Standard options in the Bank5 I/Os (REFCLK and SGMII) section.
R	12/2025	The following change is made in this revision: • Updated the hyperlink in the Simulating an FPGA Design Interacting with MSS section.
Q	12/2025	The following changes were made in this revision: • Updated the tab names in the Using the PolarFire SoC MSS Configurator GUI section. • Updated the Table 2-16. – Updated LVCMOS Standard, Output Current Drive, Supported Out Drive Values for CAN. – Updated LVCMOS Standard, Output Current Drive, Supported Out Drive Values for I2C. • Updated the section title and added Expert Mode in the Physical Memory Protection section. • Updated images as per the GUI layout change in the tool in the Running the PolarFire SoC MSS Configurator section. • Updated the Figure 3-2 in the Creating a Project and Configuring MSS section. • Updated the Application Processor Initialization and Direct Memory Access section titles.
P	05/2025	The following change is made in this revision. • Added definitions for `Boot_fail_error_M2F` and `Boot_Fail_Clear_F2M` signals in the Misc section.
N	08/2024	This document is released with Libero SoC Design Suite v2024.2 without changes from v2024.1.
M	02/2024	This document is released with Libero SoC Design Suite v2024.1 without changes from v2023.2.
L	08/2023	The following change is made in this revision. • Added new section I2C Port Configuration for Fabric I/O.
K	04/2023	The following change is made in this revision. • Updated section Clocks.

Revision History (continued)

Revision	Date	Description
J	12/2022	The following list of changes are made in this revision. • Updated section MSS To/From Fabric Interface Controllers. • Updated section Peripherals. • Updated section Bank2 I/Os. • Updated section Bank4 I/Os. • Updated section Bank5 I/Os (REFCLK and SGMII). • Updated section Bank2 and Bank4 I/Os Related to SD and eMMC Muxing. • Updated section DDR Memory. • Updated section Misc. • Updated section L2 Cache. • Updated section Physical Memory Protection. • Updated section Creating a Project and Configuring MSS.
H	08/2022	The following list of changes are made in this revision. • Updated the Batch Mode section. • Updated the Interactive Mode section. • Updated the Bank2 I/Os section. • Updated the Generating the MSS Component and Report section.
G	04/2022	The following list of changes are made in this revision. • Updated Clocks with support for -1 speed grade devices. • Added information related to Feedback ports in Misc.
F	12/2021	The following list of changes are made in this revision. • Updated Creating a Project and Configuring MSS. • Removed note from Batch Mode. • Added information related to Locked Down I/Os in Misc.
E	08/2021	The following list of changes are made in this revision. • References: Updated the MSS Fabric Interface Controller features reference.
D	08/2021	The following list of changes are made in this revision. • Clocks: Updated the Clocks Tab with addition of eMMC/SD/SDIO and CAN clock sources. • MSS To/From Fabric Interface Controllers: Fabric Interface Controller tab was renamed to 'MSS to/from Fabric Interface Controllers'. • Peripherals: Added information about eMMC or SD/SDIO setting. • MSS I/O Attributes: MSS REFCLK I/O, Bank4 and Bank2 I/Os and SGMII I/Os were moved to MSS I/O Attributes. • Misc: Updated the section with Feedback Ports option.
C	04/2021	The following list of changes are made in this revision. • Peripherals: Added note related to the availability of SD pins. • Crypto: Updated the section with Streaming Interface Option details. • Memory Partition and Protection: Added this section.

Revision History (continued)

Revision	Date	Description
B	12/2020	Revision B is released in December 2020. Following is a list of changes made in this revision: • Updated the Using the PolarFire SoC MSS Configurator GUI section. • Updated the Creating a Project and Configuring MSS section. • Updated the Generating the MSS Component and Report section. • Updated the Clocks section. • Added a note in the SGMII section.
A	9/2020	Initial Revision

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