

**UG0590**  
**RTG4 FPGA**  
**Clock Conditioning Circuit with PLL**  
**Configuration User Guide**



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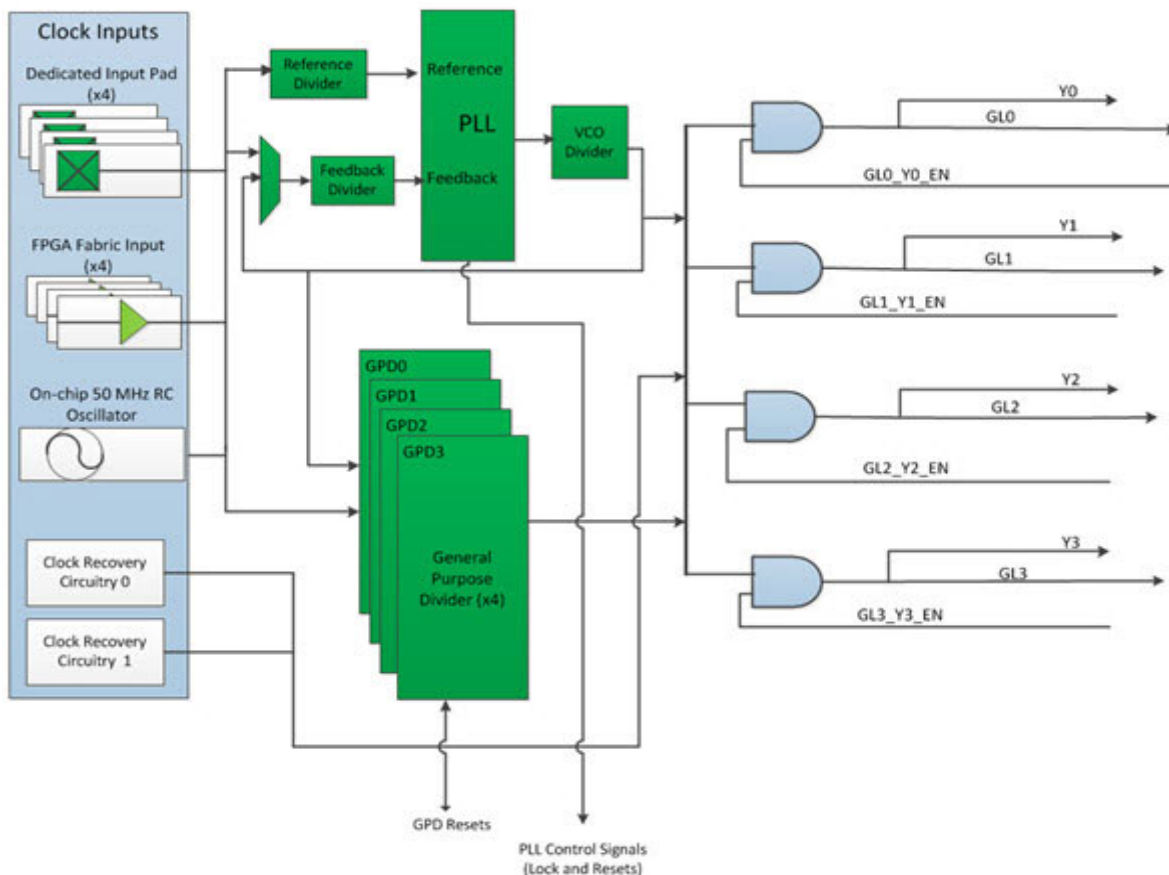
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# Introduction

The Fabric Clock Conditioning Circuit (CCC) Configurator enables you to configure the CCC/PLL blocks available on RTG4 devices (Figure 1)..



**Figure 1 • Clock Paths Overview**

The Fabric CCC can condition up to eleven input clocks to generate up to four clocks. Each of the four output clocks can directly drive the global network and/or the local routing network.

Each of the four output clocks can be driven by:

- One of eight PLL output phases
- One of four General Purpose Divider (GPD) outputs
- One of eleven input clocks:
  - Dedicated Input Pad 0
  - Dedicated Input Pad 1
  - Dedicated Input Pad 2
  - Dedicated Input Pad 3
  - FPGA Fabric Input 0
  - FPGA Fabric Input 1
  - FPGA Fabric Input 2

- FPGA Fabric Input 3
- 50 MHz On-chip Oscillator
- Clock Recovery Circuitry 0
- Clock Recovery Circuitry 1

The reference clock of the PLL can be driven by one of nine input clocks:

- Four Dedicated Input Pads
- Four FPGA Fabric Inputs
- 50 MHz On-chip Oscillator

Each of the four GPDs can be driven by either one of nine input clocks (Dedicated Input Pad 0 through 3, Dedicated Fabric Input 0 through 3 and the 50 MHz Oscillator) or one of eight PLL output phases. The configuration of the CCC can be broken down into the following three major blocks:

- Output Clocks GLx/Yx configuration
  - Clock source selection
  - Clocks frequency and phase configurations
- PLL configuration
  - PLL clock generation configuration including external feedback support
- General Purpose Divider (GPD) configuration

# 1 – Configuration Options

## Basic Configuration

Microsemi recommends the following flow to configure the clock generated by the CCC for basic use cases:

1. Select the number of desired output clocks (up to four).
2. For each selected output clock, set the required output frequency.
3. Configure the CCC/PLL reference clock source and frequency. For Oscillator input, a 50 MHz Oscillator is available.

In basic configuration, the PLL is always used to generate the output frequency. The feedback of the PLL is internal to the CCC.

Click the **Basic** tab of the CCC Configurator for the basic configuration of the CCC (Figure 1-1).

Actual output frequencies achieved by the CCC Configurator are shown in the Actual column.

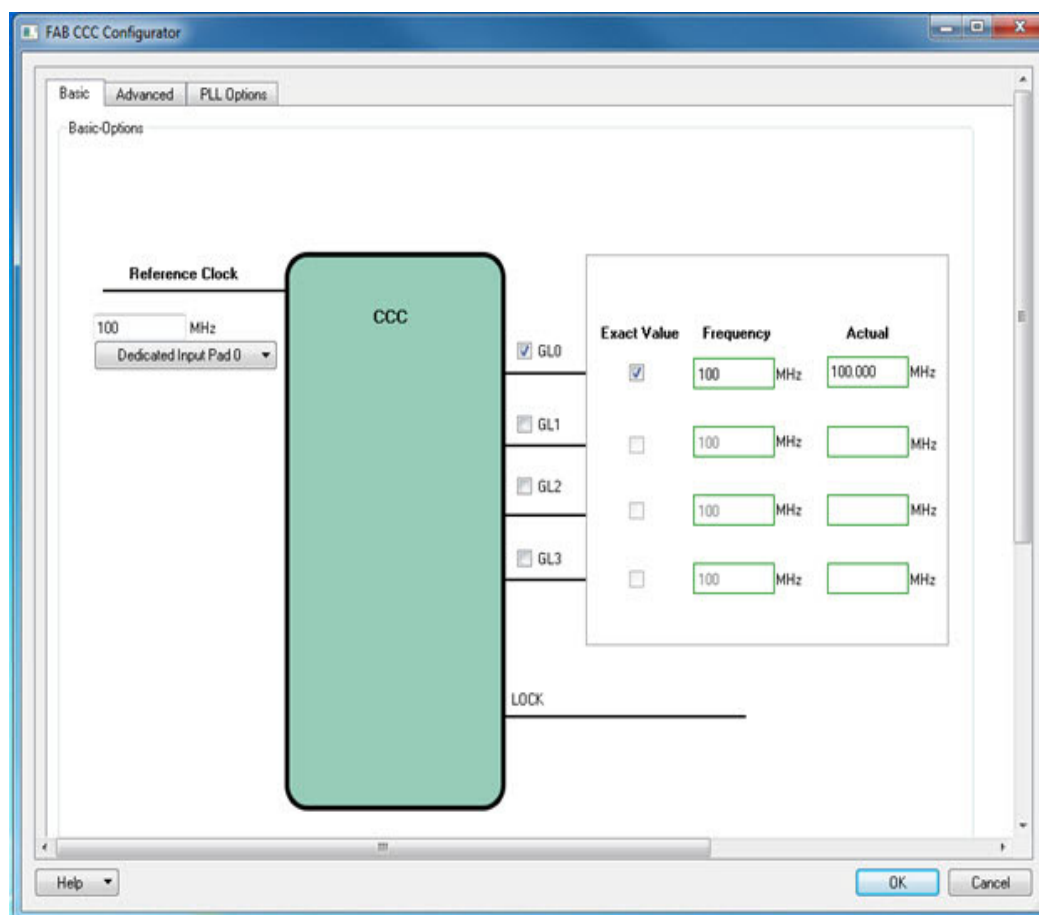


Figure 1-1 • Basic CCC Configuration Tab

## Basic Tab

### Output Clocks Selection

You must select at least one of the output clocks (Figure 1-2). The GL0, GL1, GL2 and GL3 output clocks drive a global network in the FPGA fabric.

	Frequency	Actual
<input checked="" type="checkbox"/> GL0	50.000 MHz	50.000 MHz
<input checked="" type="checkbox"/> GL1	100.000 MHz	100.000 MHz
<input checked="" type="checkbox"/> GL2	200.000 MHz	200.000 MHz
<input type="checkbox"/> GL3	100.000 MHz	MHz

Figure 1-2 • Output Clocks Selection

## Output Clock Frequency

You must specify the required output clock frequency (Figure 1-3). Those frequencies are used by the CCC Configurator to compute the configuration of the CCC dividers and PLL to meet the requirements. Actual column displays the actual value the configurator was able to achieve.

	Frequency	Actual
<input checked="" type="checkbox"/> GL0	50.000 MHz	50.000 MHz
<input checked="" type="checkbox"/> GL1	100.000 MHz	100.000 MHz
<input checked="" type="checkbox"/> GL2	200.000 MHz	200.000 MHz
<input type="checkbox"/> GL3	100.000 MHz	MHz

Figure 1-3 • Output Clock Frequency

## PLL Reference Clock Source and Frequency

The following sources are available from the reference clock pull-down menu.

**Dedicated Input Pad** - The clock source is one of the four regular FPGA I/Os that have a dedicated path to the CCC.

**Fabric Input** - The clock source is one of the four signals coming from the FPGA Fabric:

- FPGA Fabric Input 0
- FPGA Fabric Input 1
- FPGA Fabric Input 2
- FPGA Fabric Input 3

**Oscillators** - The source is from the 50MHz on-chip oscillator.

## Advanced Configuration

For advanced use-cases, Microsemi recommends using the following flow to configure the clock generated by the CCC (flow proceeds from right to left in the GUI):

1. Select the number of desired output clocks (up to four).
2. For each selected output clock, set the required output frequency. Output frequency cannot be set when the selected output clock has an input from Clock generated by Clock Recovery Circuitry.
3. For each selected output clock, select the desired reference (input) clock from which the output will be derived. It can be:
  - One of CCC input clocks (PLL bypass mode), which can be one of four Dedicated Pads or one of four FPGA Fabric Inputs
  - One of 8 PLL output phases
  - 50 MHz Oscillator
  - Clock Recovery Circuitry
4. If required:
  - Select the PLL reference clock source and frequency

- Select the PLL feedback source
- 5. Enter the frequency of each selected source clock(s) (either as the PLL reference or direct source for the output). The configurator uses those frequencies to compute the division factor of the PLL reference and feedback dividers as well as the GPD dividers.

The configurator automatically tries to compute a configuration that meets the frequency requirements and all the internal CCC/PLL constraints. If the configurator is unable to find an exact solution for all requirements, it finds a configuration that globally minimizes the error between the required and actual frequency.

Actual data (divider settings, PLL output frequency, and actual outputs frequencies) are shown in the advanced dialog in blue (Figure 1-4).

Click the **Advanced** tab in the CCC Configurator for Advanced configuration.

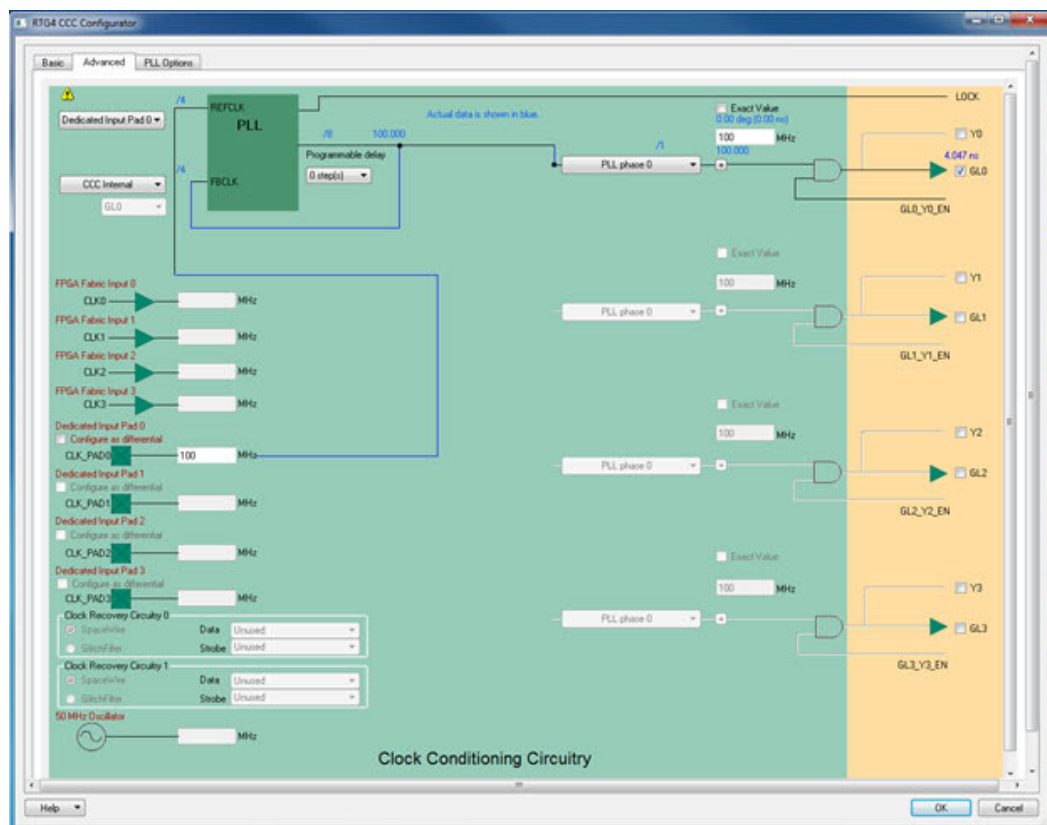


Figure 1-4 • Advanced Options

## Advanced Tab

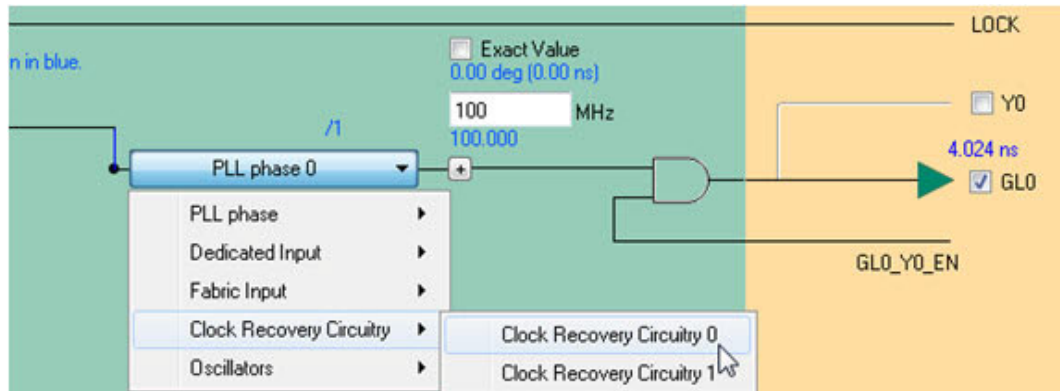
The advanced configuration tab inherits settings from the basic tab. Modifying a parameter in the Advanced tab that cannot be reflected in the Basic tab results in a warning in the Basic tab.

## Output Clocks Selection

You must select at least one of the output clocks. The GL0, GL1, GL2 and GL3 clocks drive a global network in the FPGA fabric; Y0, Y1, Y2 and Y3 drive local routing resources in the FPGA fabric.



## Clock Source Selection



**Figure 1-5 • Clock Source Selection**

The source of the GLx/Yx clocks (Figure 1-5) can be:

**PLL** - The PLL block offers eight phases (0 deg to 315 deg in 45 deg steps). The actual phases and resulting delays are highlighted in blue on the configurator UI. The actual phase is not the same as the selected phase if the output divider is not 1 (actual\_phase = selected\_phase / output\_divider).

**Dedicated Input Pad** - The clock source is one of the four regular FPGA I/O's that has a dedicated path to the CCC.

**FPGA Fabric Input** - The clock source is one of the four fabric input signals coming from the FPGA Fabric.

**Clock Recovery Circuitry** - Two RX Clock Recovery Circuitry Blocks are available: Block 0 and Block 1 for each CCC. If your design has Spacewire soft IPs, configure the source of your GLx to use the Clock Recovery Circuitry. The GLx output can then be used to drive the Spacewire Soft IPs.

**Oscillators** - The source is from the on-chip 50MHz oscillator.

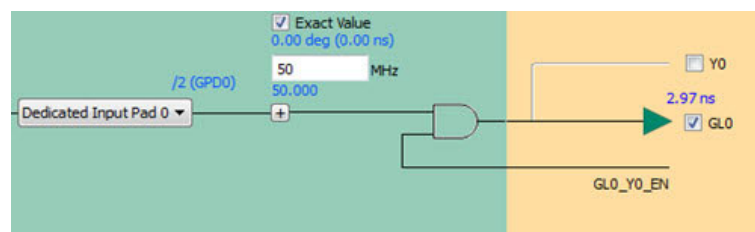
### Output Clock Frequency

You must specify the required output clock frequency. Those frequencies are used by the CCC Configurator to compute the configuration of the CCC dividers and PLL to meet the requirements. The dividers and their names are highlighted in blue in the UI (Figure 1-6).

#### Exact Value Option

When you click the Exact Value checkbox to turn on this option, it forces the CCC Configurator to generate the nearest actual frequency with a tolerance of 0.5 KHz. If this is not possible, it generates an error with the following error message:

*Exact Value option is used. No divider combination was found to satisfy the current settings. Consider adjusting or relaxing the configuration requirements.*



**Figure 1-6 • Output Frequency**

## Gated Clock Configuration

For GLx/Yx, Clock Gating is an inherent feature for RTG4 CCC. It is enabled for both GL# and Y#. GL#\_Y#\_EN gates the global network driven by GL#\_Y#\_EN where x can be 0, 1, 2, or 3 (Figure 1-7).

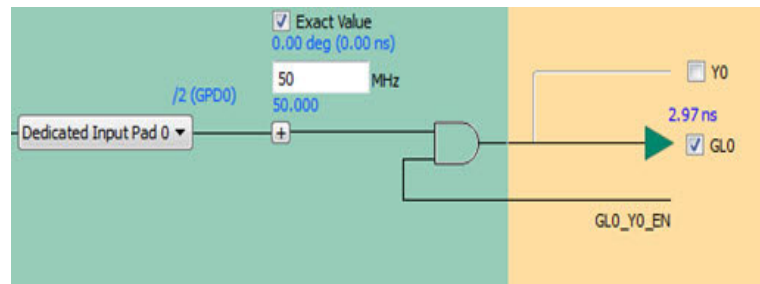


Figure 1-7 • GL#\_Y#\_EN Signal

## Inversion Configuration

The output can be inverted if required (Figure 1-8). The inversion affects GLx and Yx clock. Click the + sign to get the inverted output.

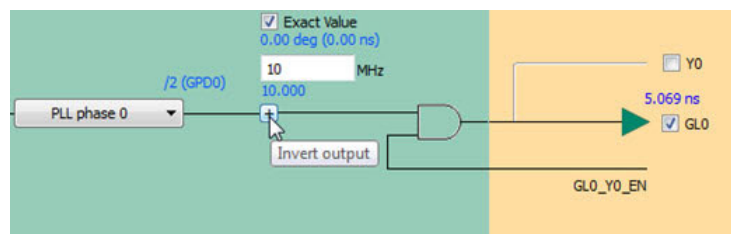


Figure 1-8 • Inverted Configuration

## Total Output Delay

The CCC Configurator automatically computes the total input to output delay of Y0/1/2/3 and GL0/1/2/3 and displays the delay number (ns) in blue (Figure 1-9).

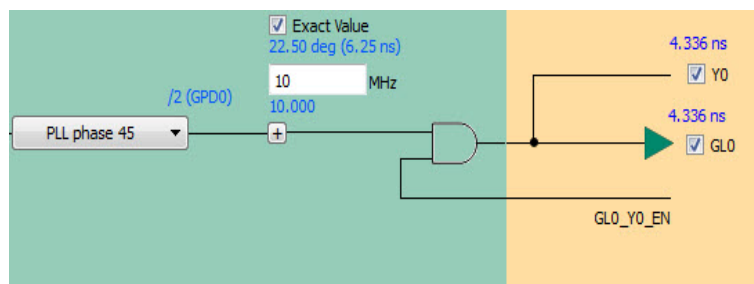


Figure 1-9 • Total Delay

## PLL Configuration

### PLL Reference Clock Source

The following sources are available from the reference clock pull-down menu (Figure 1-10):

**Dedicated Input Pad** - The clock source is one of the four regular FPGA I/Os that has a dedicated path to the CCC. The Configure as differential option allows you to configure any dedicated Input Pad as differential I/O.

**FPGA Fabric Input** - The clock source can be one of the four input signals coming from the FPGA Fabric.

**Oscillators** - The source is from the on-chip 50MHz oscillator.

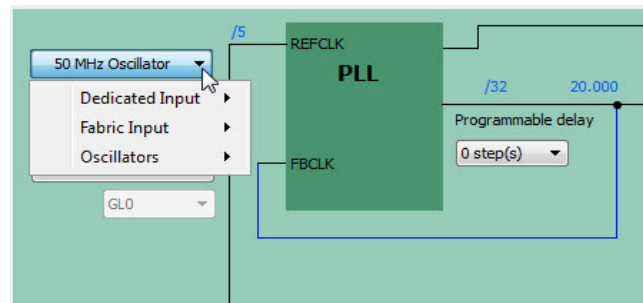


Figure 1-10 • PLL Reference Clock Source

### PLL Feedback Source

If you use the PLL you can choose to use an internal or an external feedback loop depending on your system level requirements (Figure 1-11).

In some cases, the PLL can experience a loss of lock event from which it does not automatically self-recover. In these cases, the assertion of the PLL ARST\_N input is required to regain lock. By default, an additional fabric logic circuit will be added by the CCC Configurator to monitor the PLL lock signal and issue a reset command to the PLL, if loss of lock is detected. This circuit requires a 50 MHz clock that is readily available from the on-chip RC oscillator. You need to instantiate the **RCOSC\_50MHZ** macro and distribute its output through a GLx of any one CCC as described in the **Output Clock Selection** section above and eventually connect to the exposed **CLK50\_MHZ** input pin of this CCC. The CCC connected to **RCOSC\_50MHZ** could even be the same CCC as this one. If you do not want to use the on-chip RC oscillator, the CLK50\_MHZ input pin of the CCC can be driven by an external free-running oscillator running at 50MHz or slower.

**Note:** Feedback Configuration other than PLL Internal will configure the PLL in non-triplicated mode. Single PLL mode is mitigated for radiation but does not provide the same level of radiation tolerance as the three working together.

#### Internal Feedback Loop:

- **CCC Internal** - Default option
- **PLL Internal** - This is a shorter feedback path integrated into the PLL. Note: Programmable delay and output synchronization are not available in this mode.

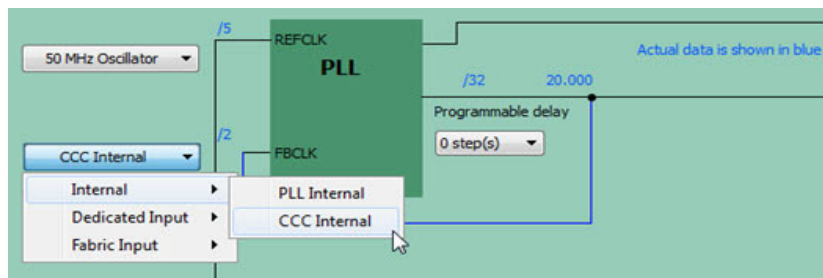
When PLL Internal feedback mode is selected, the PLL will be configured in Triple Module Redundant mode, which includes three sub PLLs with a voted lock to help mitigate single event effects in a radiation environment. The triple redundant PLL mode is more robust than the single PLL mode with respect to loss of lock events.

#### External Feedback Loop:

The external feedback is driven from the selected GLx/Yx fabric CCC output either through the fabric or externally to the chip.

- **Dedicated Input Pad** - The clock source is one of the four regular FPGA I/Os that has a dedicated path to the CCC.

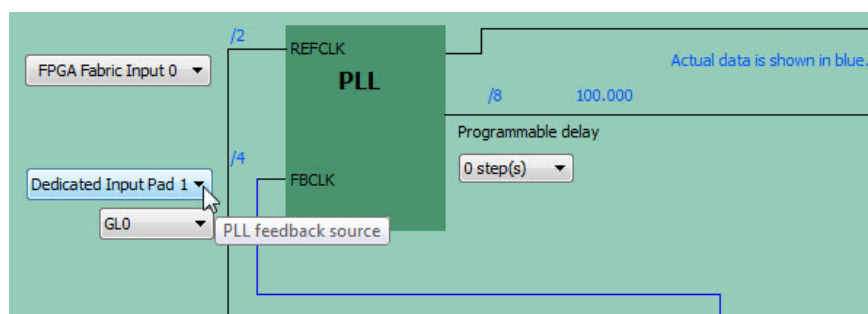
- **FPGA Fabric Input** - The clock source can be one of the four input signals coming from the FPGA Fabric.



**Figure 1-11 • PLL Internal Feedback Source**

### **PLL External Feedback Source**

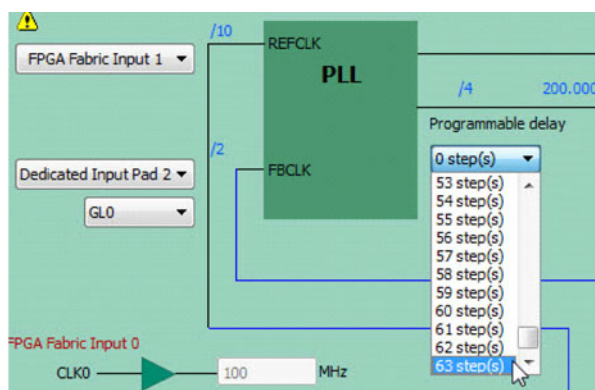
If you use the PLL with an external feedback source, all engine computations are based on the assumptions that the external feedback is driven from the selected GLx/Yx fabric CCC output whether through the fabric or externally to the chip (Figure 1-12).



**Figure 1-12 • PLL External Feedback Source**

### **Programmable Delay Line**

The programmable delay line enables you to delay (or advance) the PLL output clock with respect to the PLL reference clock by applying a delay to the reference clock path (or feedback path), as in Figure 1-13.

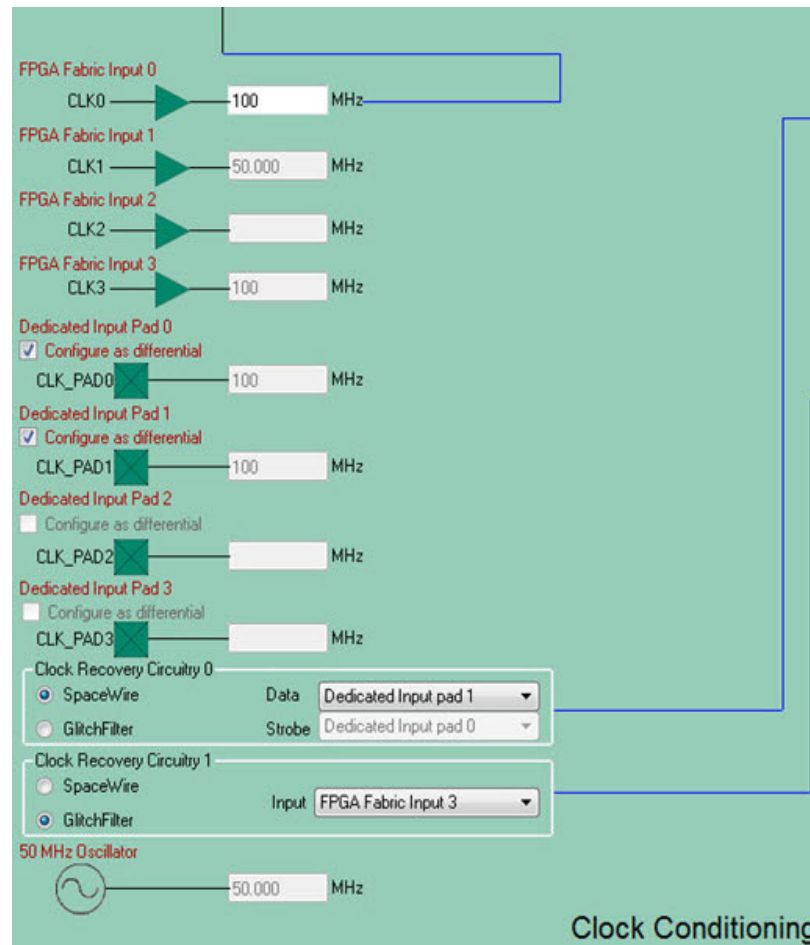


**Figure 1-13 • Programmable Delay Line**

## Input Clocks Configuration

You must enter the clock frequency each CCC input used in the configuration as the PLL reference clock, PLL feedback clock or Output direct connection (Figure 1-15). Those frequencies are used to compute the PLL configuration and divider configuration that meet the output frequencies requirements.

Use Rx Clock Recovery Circuitry to configure the CCC outputs to drive SpaceWire Soft IPs.



**Figure 1-15 • Input Clocks Configuration**

**Dedicated Input Pad** - Some of the dedicated inputs to the CCC can be configured to use a differential I/O technology. The location, I/O technology and attributes available for each CCC dedicated input pad is described in the Microsemi RTG4 Datasheet.

### Clock Recovery Circuitry:

Each CCC block has two dedicated RX Clock Recovery Circuitry Blocks: Block 0 and Block 1. The Clock Recovery Circuitry Blocks 0 and Block 1 can be used in either the SpaceWire mode (Default) or the GlitchFilter mode.

**Note:** For RT4G150-ES devices, the Glitch Filtering mode is not available and it is disabled.

The RX clock is based on Data and Strobe Inputs, which are from external dedicated I/Os. The Clock Recovery Circuitry Blocks also include a de-glitching circuit to prevent any undesirable narrow clock pulse at output.

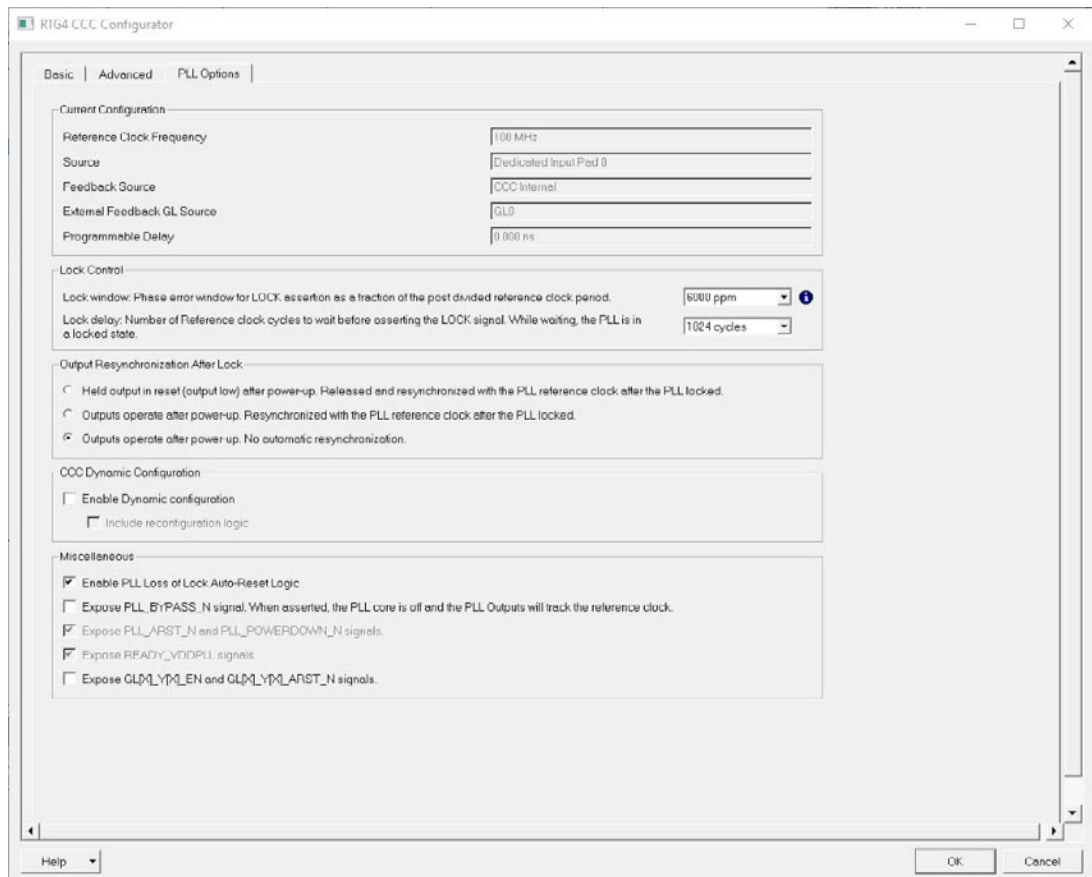
1. You can select Dedicated input pad [1 and 3] for Data signal. Dedicated input pads[0 and 2] will be automatically set as corresponding Strobe signal.

2. The same pair of Dedicated input pads cannot be used simultaneously in Clock Recovery Circuitry.
3. Dedicated input pads which are used as Data and Strobe signals for Clock Recovery Circuitry block cannot be used as input to PLL Reference Clock and PLL Feedback Clock.
4. You cannot set input frequency values for Dedicated pads which are configured as Data and Strobe signals for RX Clock Recovery Circuitry.
5. Clock Recovery Circuitry Block 0 and 1 cannot have the same input source when both are configured for SpaceWire mode.
6. Clock Recovery Circuitry Block 0 and 1 cannot have the same input source when both are configured for Glitch Filter mode.
7. Clock Recovery Circuitry Block 0 and 1 cannot have the same input source when one is configured for SpaceWire mode and the other is configured for Glitch Filter mode.
8. It is valid to select the same input for PLL REFCLK (and CGL secondary clock) and Glitch Filter.

## 2 – PLL Options

The PLL Options enable you to configure advanced PLL options, such as output resynchronization and reset signals.

Click the **PLL Options** tab in the CCC Configurator for the PLL Options (Figure 2-1).



**Figure 2-1 • PLL Options**

The PLL Options summarizes your PLL configuration (Figure 2-2).



**Figure 2-2 • PLL Configuration Summary**

## Lock Control

**Lock Window** - Enables you to configure the maximum phase error allowed for the PLL to indicate it has locked. The lock window is expressed as part per million of the post divided reference clock period.

Refer to [UG0586: RTG4 FPGA Clocking Resources User Guide](#) for guidelines on selecting the appropriate PLL Lock Window. This is especially important for applications requiring phase alignment between the CCC input reference clock and the CCC outputs.

**Lock Delay** - Enables you to set the number of Reference REFCLK clock cycles to wait before asserting the LOCK signal. While waiting, the PLL is in a locked state.

**Note:** Lock Delay is not supported in Simulation.

## Output Resynchronization After Lock Configuration

RTG4 CCC contains four General Purpose Dividers (GPD). These dividers' source and division settings are automatically configured based on the frequency requirement you specified in the CCC Configurator. GPDs can be used as the source of any outputs. For example, GPD0 can be used on a path to the GL1 output. Microsemi recommends that you re-synchronize GPDs driven by the PLL output clock after the PLL locks to ensure that the first edge of each GPD is aligned with the PLL reference clock and with each other.

There are three different resynchronization options for GPDs/outputs:

### **Held Output in reset (output low) after power up. Released and resynchronized with the PLL Reference clock after the PLL locked**

- If enabled, GPD(s) (driven by the PLL) are held in reset low after power-up. Hence the output(s) (GLx/Yx) connected to those GPD(s) are held low (or high if inverted) after power-up.
- After the PLL lock, the GPD(s) reset are released synchronously with the PLL reference clock.
- The CCC Configurator automatically inserts a GPD on each GL/Y output driven by the PLL even if the division factor is 1. This ensures the GL/Y driven by the PLL is held in reset at power-up.
- Does not apply to the output(s)/GPD(s) on the PLL external feedback path (if any).
- Does not apply for the output(s)/GPD(s) not driven by one of the PLL 8 phases output.

**Note:** If you select PLL internal as a feedback source and the option "Output Resynchronization After Lock", outputs will be resynchronized between each other after the PLL locks, but will not be resynchronized with the PLL reference clock.

### **Outputs Operate after power up. Released and resynchronized with the PLL reference clock after the PLL locked**

- If enabled, GPD(s) (driven by the PLL) output are operational after power-up. Hence the output(s) (GLx/Yx) connected to those GPD(s) are operational after power-up.
- After the PLL lock, the GPD(s) is synchronously reset with the PLL reference clock.
- Does not apply to the output(s)/GPD(s) on the PLL external feedback path (if any).
- Does not apply for the output(s)/GPD(s) not driven by one of the PLL 8 phases output.

**Note:** If you select PLL internal as a feedback source and the option "Output Resynchronization After Lock", outputs will be resynchronized between each other after the PLL locks, but will not be resynchronized with the PLL reference clock.

### **Outputs Operate after power up. No automatic resynchronization**

- If enabled, the corresponding GPD(s) output is operating after power-up. Hence the outputs (GLx/Yx) connected to this GPD are operating after power-up.
- There is no resynchronization after the PLL lock.
- All GPD(s) directly connected to one of the nine input clocks (bypassing the PLL) are configured in this mode.

**Note:** For RT4G150-ES devices in modes other than PLL\_INTERNAL feedback mode, this is the only supported option. If you select options other than this supported option and click **OK** and **Save**, an error message appears as follows:



*The selected option of Output Resynchronization after Lock is not supported for ES devices and the only supported option is Outputs Operate after power-up with No automatic resynchronization.*

**Note:** When the CCC is used without the PLL, such as when performing clock frequency division, the GPD(s) require a manual assertion and release of the GPDx\_ARST\_N input to synchronize the GPD output(s) to the input reference clock, after it has become stable. For example, the lock signal output of an upstream PLL could be used to release the GPDx\_ARST\_N input so that this CCC's divided output(s) are synchronized to the input clock.

## CCC Dynamic Configuration

**Enable Dynamic configuration** - When selected, the CCCDYN macro is instantiated during generation. An APB slave interface is exposed to the FPGA fabric. There is one APB slave interface per corner of the fabric, and thus the two CCCs in a given corner share the same dynamic configuration APB interface. This interface can be used to read or modify the CCC configuration registers from the FPGA fabric. Refer to the [RTG4 Clocking Resources User Guide](#) for the list of CCC Configuration registers.

When enabled, the user has the option to include or not include the Reconfiguration logic associated with the CCCDYN.

**Include reconfiguration logic** - When checked, the CCCAPB macro is instantiated during generation. Check this box for single CCC operation. Uncheck this box for Dual CCC operation.

**Note:** This box is disabled when **Enable Dynamic configuration** is not selected.

When both **Enable Dynamic configuration** and **Include reconfiguration logic** are checked, the top-level ports are connected to the CCCAPB ports which are connected to the ports on the CCCDYN macro.

When only **Enable Dynamic configuration** is checked, and **Include reconfiguration logic** is not checked, the CCCDYN is instantiated and the top-level ports are directly connected to the CCCDYN macro.

When neither **Enable Dynamic configuration** nor **Include reconfiguration logic** is checked, the regular CCC macro is instantiated and the top-level ports are directly connected to the CCC macro.

## Miscellaneous Options

**Enable PLL Loss of Lock Auto Reset Logic** - This option is enabled by default whenever the PLL is used. Disabling this option will result in a Warning Exclamation Icon with a tool-tip message that states:

*Warning: The insertion of PLL loss of lock auto-reset logic has been disabled. Auto-reset is helpful in the event the PLL lock is lost during operation. Please review Customer Notifications 19009 and 18009.7 on the Microsemi website to understand the consequences of disabling this option.*

**Expose PLL\_BYPASS\_N signal** - When selected, the input signal PLL\_BYPASS\_N is exposed to the FPGA Fabric. When this signal is asserted, the PLL core is turned off and the PLL outputs track the reference clock. This signal is active low.

**Expose PLL\_ARST\_N and PLL\_POWERDOWN\_N signals** - When selected, the signals PLL\_ARST\_N and PLL\_POWERDOWN\_N are exposed to the FPGA Fabric. When PLL\_ARST\_N is asserted, the PLL core is turned off and the PLL outputs are low. When PLL\_POWERDOWN\_N is asserted, PLL is off and is in the lowest power consumption mode. The PLL outputs are low. Both signals are active low. When PLL is not bypassed, both PLL\_ARST\_N and PLL\_POWERDOWN\_N signals are always exposed.

**Expose READY\_VDDPLL signals** - When selected, the READY\_VDDPLL signal is exposed to the FPGA Fabric. When READY\_VDDPLL is low, the PLL core is turned off and the PLL outputs are low. Tie READY\_VDDPLL to high if you are certain that VDDPLL will not be the last supply to ramp up, per the RTG4 Datasheet and Board Design Guideline recommendations. For applications which cannot meet the guideline of ensuring VDDPLL is not the last supply to ramp up, select this option to expose READY\_VDDPLL and drive the input from 1 of the 2 suggested circuits described in the [RTG4 Clocking Resources User Guide](#). One solution uses internal logic to delay the assertion of VDDPLL by 73ms while the other uses external components and a user input pin to sense when VDDPLL has reached the recommended operating voltage. When PLL is not bypassed, READY\_VDDPLL is always exposed.

**Expose GL[X]\_Y[X]\_EN and GL[X]\_Y[X]\_ARST\_N signals** - When selected, the GL[X]\_Y[X]\_EN and GL[X]\_Y[X]\_ARST\_N signals are exposed to the FPGA fabric. By default, these signals are not exposed.

**Expose GPD[X]\_ARST\_N signals for all used GPDs** - This option is only available when the input clock to the GPD(s) is not sourced from the PLL. For example, a CCC output configured to use an input clock source coming from a Dedicated Input, a Fabric Input, or an internal oscillator will cause this option to appear and be enabled. When selected, the GPD[X]\_ARST\_N signals are exposed for all used GPDs. For CCC output configurations which use the PLL output, this option is not listed in the PLL Options tab because the GPD reset signal is used inside the CCC to achieve the desired "Output Resynchronization After Lock" setting. This input has a built-in glitch filter to mitigate the impact of Single Event Transients on this signal.

## Clock Frequency Requirements

You must specify the clock source frequency. Note the following frequency requirements:

- The On-chip 50MHz Oscillator clock frequency is fixed at 50 MHz.
- PLL reference clock frequency must be between 10 MHz and 200 MHz
- Output clock frequencies must be less than 400 MHz.
- Input used in bypass mode frequency must be less than 400 MHz

## 3 – Port Description

**Table 3-1 • Fabric CCC Port Description**

Port Name	Direction	Polarity	Description
CLK0_PAD	Input	-	Input clock when using <b>Dedicated Input Pad 0</b> configured as single ended I/O
CLK0_[PADP and PADN]	Input	-	Input clock when using <b>Dedicated Input Pad 0</b> configured as differential I/O. P side and N side
CLK1_PAD	Input	-	Input clock when using <b>Dedicated Input Pad 1</b> configured as single ended I/O
CLK1_[PADP and PADN]	Input	-	Input clock when using <b>Dedicated Input Pad 1</b> configured as differential I/O. P side and N side
CLK2_PAD	Input	-	Input clock when using <b>Dedicated Input Pad 2</b> configured as single ended I/O
CLK2_[PADP and PADN]	Input	-	Input clock when using <b>Dedicated Input Pad 2</b> configured as differential I/O. P side and N side
CLK3_PAD	Input	-	Input clock when using <b>Dedicated Input Pad 3</b> configured as single ended I/O
CLK3_[PADP and PADN]	Input	-	Input clock when using <b>Dedicated Input Pad 3</b> configured as differential I/O. P side and N side
CLK0_SPWR_STROBE_[PADP and PADN]	Input	-	Input Clock when Dedicated pad 0 is used as input to <b>Strobe</b> of Clock Recovery Circuitry in differential mode. SpaceWire Mode only.
CLK1_SPWR_DATA_[PADP and PADN]	Input	-	Input Clock when Dedicated Pad 1 is used as input to <b>Data</b> of Clock Recovery Circuitry in differential mode. SpaceWire Mode only.
CLK2_SPWR_STROBE_[PADP and PADN]	Input	-	Input Clock when Dedicated pad 2 is used as input to <b>Strobe</b> of Clock Recovery Circuitry in differential mode. SpaceWire Mode only.
CLK3_SPWR_DATA_[PADP and PADN]	Input	-	Input Clock when Dedicated Pad 3 is used as input to <b>Data</b> of Clock Recovery Circuitry in differential mode. SpaceWire Mode only.
CLK0_SPWR_STROBE_PAD	Input	-	Input Clock when Dedicated pad 0 is used as input to <b>Strobe</b> of Clock Recovery Circuitry configured as single ended I/O. SpaceWire Mode only.
CLK1_SPWR_DATA_PAD	Input	-	Input Clock when Dedicated pad 1 is used as input to <b>Data</b> of Clock Recovery Circuitry configured as single ended I/O. SpaceWire Mode only.
CLK2_SPWR_STROBE_PAD	Input	-	Input Clock when Dedicated pad 2 is used as input to <b>Strobe</b> of Clock Recovery Circuitry configured as single ended I/O. SpaceWire Mode only.

**Table 3-1 • Fabric CCC Port Description (continued)**

Port Name	Direction	Polarity	Description
CLK3_SPWR_DATA_PAD	Input	-	Input Clock when Dedicated pad 3 is used as input to <b>Data</b> of Clock Recovery Circuitry configured as single ended I/O. SpaceWire Mode only.
CLK0	Input	-	Input clock from FPGA core when using <b>FPGA Fabric Input 0</b>
CLK1	Input	-	Input clock from FPGA core when using <b>FPGA Fabric Input 1</b>
CLK2	Input	-	Input clock from FPGA core when using <b>FPGA Fabric Input 2</b>
CLK3	Input	-	Input clock from FPGA core when using <b>FPGA Fabric Input 3</b>
RCOSC_50MHZ	Input	-	Input clock when using <b>50 MHz Oscillator</b>
GL0	Output	-	Generated clock driving FPGA fabric global network 0
GL1	Output	-	Generated clock driving FPGA fabric global network 1
GL2	Output	-	Generated clock driving FPGA fabric global network 2
GL3	Output	-	Generated clock driving FPGA fabric global network 3
GL0_Y0_EN	Input	High	Enable signal for the clock driving FPGA fabric global network 0 (GL0) and fabric local routing (Y0) network 0
GL1_Y1_EN	Input	High	Enable signal for the clock driving FPGA fabric global network1 (GL1) and fabric local routing (Y1)
GL2_Y2_EN	Input	High	Enable signal for the clock driving FPGA fabric global network 2 (GL2) and fabric local routing (Y2) network 2
GL3_Y3_EN	Input	High	Enable signal for the clock driving FPGA fabric global network 3 (GL3) and fabric local routing (Y3) network 3
GL0_Y0_ARST_N	Input	Low	(GL0/Y0) CGL reset signal. Asynchronous reset signal
GL1_Y1_ARST_N	Input	Low	(GL1/Y1) CGL reset signal. Asynchronous reset signal
GL2_Y2_ARST_N	Input	Low	(GL2/Y2) CGL reset signal. Asynchronous reset signal
GL3_Y3_ARST_N	Input	Low	(GL3/Y3) CGL reset signal. Asynchronous reset signal
Y0	output	-	Generated clock driving FPGA fabric local routing resource
Y1	output	-	Generated clock driving FPGA fabric local routing resource
Y2	output	-	Generated clock driving FPGA fabric local routing resource
Y3	output	-	Generated clock driving FPGA fabric local routing resource

**Table 3-1 • Fabric CCC Port Description (continued)**

Port Name	Direction	Polarity	Description
RX0_DATA_PORT	output	-	Output port for RX0 Data. Same signal that is driving the RX0 Spacewire clock recovery Data input
RX1_DATA_PORT	output	-	Output port for RX1 Data. Same signal that is driving the RX1 Spacewire clock recovery Data input
LOCK	output	High	PLL Lock indicator signal. This signal is asserted (lock) high.
PLL_BYPASS_N	Input	Low	Powers-down the PLL core and bypasses it such that PLL_OUT tracks reference clock. This has higher priority than reset.
PLL_ARST_N	Input	Low	Powers-down the PLL core and asynchronously reset all its internal digital blocks such that the PLL outputs are driven low.
PLL_POWERDOWN_N	Input	Low	Powers-down the PLL for the lowest quiescent current and the PLL outputs are Low. This has higher priority than reset and bypass
READY_VDDPLL	Input	High	Tie to high if you are certain that VDDPLL will not be the last supply to ramp up. Otherwise, connect to a circuit that delays the assertion of VDDPLL by 73ms as described in the <a href="#">RTG4 Clocking Resources User Guide</a> .
CLK50_MHZ	Input	-	Input clock to issue reset command to the PLL, if loss of lock is detected. The frequency of this clock must be 50 MHz max. You may connect to the GLx output of any CCC that is distributing the <b>RCOSC_50MHZ</b> signal. You cannot directly connect a <b>RCOSC_50MHZ</b> macro to this input port. Alternatively, an external free-running oscillator clock can be used as long as the frequency is 50MHz or less.
<b>Fabric CCC Configuration Bus Interface Signals – APB3 Bus Interface</b>			
APB_S_PCLK	Input	-	APB3 interface clock signal
APB_S_PRESET_N	Input	Low	APB3 interface active low reset signal.
APB_S_PADDR[7:2]	Input	-	APB3 interface address bus. This port is used to address fabric CCC internal registers.
APB_S_PSEL	Input	-	APB3 interface slave select signal.
APB_S_PENABLE	Input	High	APB3 interface strobe signal to indicate the second cycle of an APB3 transfer.
APB_S_PWRITE	Input	-	APB3 interface read/write control signal. When High, this signal indicates an APB3 write access and when Low, a read access.
APB_S_PWDATA[7:0]	Input	-	APB3 interface write data bus.
APB_S_PRDATA[7:0]	Output	-	APB3 interface read data bus.

**Table 3-1 • Fabric CCC Port Description (continued)**

APB_S_PREADY	Output	-	APB3 interface ready indication output to master.
APB_S_PSLVERR	Output	-	APB3 interface error indication signal.

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## A – Product Support

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Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

### Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call **800.262.1060**

From the rest of the world, call **650.318.4460**

Fax, from anywhere in the world, **650.318.8044**

### Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

### Technical Support

For Microsemi SoC Products Support, visit <http://www.microsemi.com/products/fpga-soc/design-support/fpga-soc-support>.

### Website

You can browse a variety of technical and non-technical information on the Microsemi SoC Products Group [home page](http://www.microsemi.com/soc), at [www.microsemi.com/soc](http://www.microsemi.com/soc).

### Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

#### Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is [soc\\_tech@microsemi.com](mailto:soc_tech@microsemi.com).

## My Cases

Microsemi SoC Products Group customers may submit and track technical cases online by going to [My Cases](#).

## Outside the U.S.

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Visit [About Us](#) for sales office listings and corporate contacts.

Sales office listings can be found at [www.microsemi.com/soc/company/contact/default.aspx](http://www.microsemi.com/soc/company/contact/default.aspx).

## ITAR Technical Support

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