Libero® SoC v2021.3

RTG4™ FCCC with Enhanced PLL Calibration Configurator User Guide

Introduction

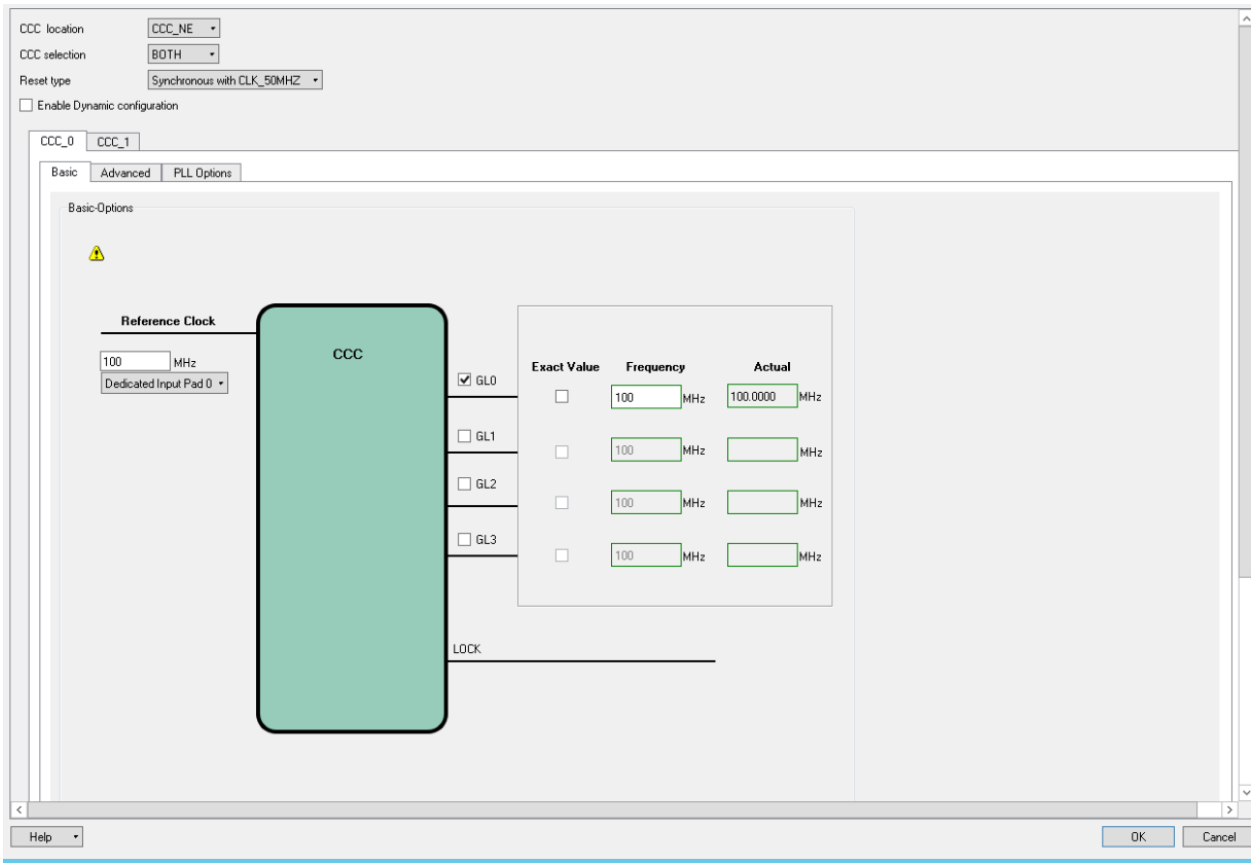
The RTG4™ FCCC with Enhanced PLL Calibration Configurator generated circuit includes soft logic that performs calibration at power-up or when the PLL is reset. This ensures that the PLL lock is stable during normal operation within the supported RTG4 operating junction temperature range.

This document describes the RTG4 FCCC with Enhanced PLL Calibration Configurator. This configurator enables the configuration of two CCCs —CCC_0 and CCC_1. You must configure one or both of the CCCs. Enhanced lock PLL calibration soft logic is implemented for all the configured CCCs.

The enhanced PLL calibration removes any Fabric PLL lock stability dependence on the operating junction temperature across the supported RTG4 operating temperature range for non-triplicated PLL. For more information about the configuration options for the RTG4 FCCC with Enhanced PLL Calibration Configurator, see 2. Configuration Options.

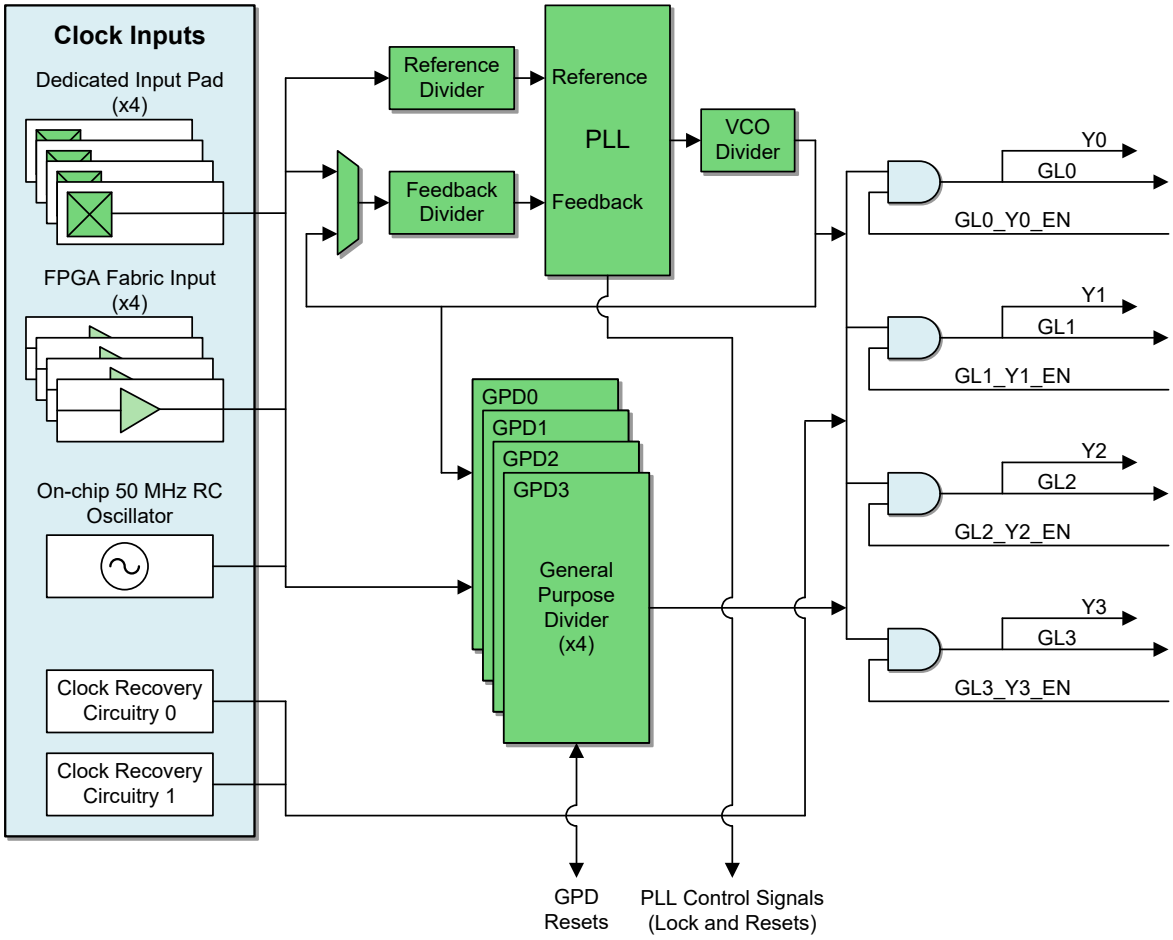
The following figure shows the top-view of the RTG4 FCCC with Enhanced PLL Calibration Configurator.

Figure 1. RTG4 FCCC with Enhanced PLL Calibration Configurator



The RTG4 FCCC with Enhanced PLL Calibration Configurator enables you to configure two of the eight CCC/PLL blocks available on the RTG4 devices.

Figure 2. Clock Paths Overview



The Fabric CCC can condition up to 11 input clocks to generate up to four clocks. Each of the four output clocks can directly drive the global network and/or the local routing network.

Each of the four output clocks can be driven by:

- One of the eight PLL output phases
- One of the four General Purpose Divider (GPD) outputs
- One of the eleven input clocks:
  - Dedicated Input Pad 0
  - Dedicated Input Pad 1
  - Dedicated Input Pad 2
  - Dedicated Input Pad 3
  - FPGA Fabric Input 0
  - FPGA Fabric Input 1
  - FPGA Fabric Input 2
  - FPGA Fabric Input 3
  - 50 MHz On-chip Oscillator
  - Clock Recovery Circuitry 0
  - Clock Recovery Circuitry 1

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The reference clock of the PLL can be driven by one of the nine input clocks:

- Four Dedicated Input Pads
- Four FPGA Fabric Inputs
- 50 MHz On-chip Oscillator

Each of the four GPDs can be driven by either one of the nine input clocks (Dedicated Input Pad 0 through 3, Dedicated Fabric Input 0 through 3, and the 50 MHz Oscillator) or one of the eight PLL output phases. The configuration of the CCC can be broken down into the following three major blocks:

- Output Clocks GL[x]/Y[x] configuration
  - Clock source selection
  - Clocks frequency and phase configurations
- PLL configuration
  - PLL clock generation configuration including external feedback support
- GPD configuration

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1. Calibration

Calibration consists of two processes:

- Calibration
- Recalibration

1.1 Calibration

PLLs present in the fabric CCC in the RTG4 family might loose ‘LOCK’ at high temperatures. Review Customer Notifications19009A for more information.

In the CCC, ‘loss of PLL lock’ issue is addressed using soft logic that is added as part of the RTG4 FCCCECALIB generated circuit. The soft logic performs calibration at power-up or when the CCC is reset to ensure that the PLL lock is stable during the normal operation.

Internally, controller core, CorePLL_ELOCK, writes the PLL registers through the APB interface. The register values are chosen such that the high VCO values are written first, wait for 150 us and then writes the Actual VCO values.

High VCO is chosen such that the value is in the range from 1.5 to 1.9 times of the actual VCO.

If both the CCCs are used in the design, then the CCC_0 registers is loaded first followed by the CCC_1 registers.

1.2 Recalibration

Recalibration is the process of performing calibration again and this can happen in following scenarios:

1. When the **Enable Auto Reset on PLL loss of lock** in the **PLL Options** tab is selected and the lock signal goes low, then the recalibration process gets triggered.
2. Reset is applied using PLL_RST_N.
3. If both the CCCs are used and if the power-down signal (CCC_0_POWERDOWN_N or CCC_1_POWERDOWN_N) goes low, then recalibration gets triggered for the corresponding CCC.
4. If READY_VDDPLL goes low, then the calibration process gets triggered—in this case, both the CCCs are calibrated.

During the recalibration process, the lock signals of the CCC that is CCC_0_LOCK and CCC_1_LOCK goes low if both CCC’s are getting recalibrated. Otherwise, the corresponding CCC lock goes down and CCC_<id>_LOCK becomes low.

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2. Configuration Options

The RTG4 FCCC with Enhanced PLL Calibration Configurator consists of the below configuration options.

2.1 Basic Configuration

This section describes basic configuration of the RTG4 FCCC with Enhanced PLL Calibration Configurator.

2.1.1 CCC Location

You must choose a physical location for the CCC pair:

- CCC_NW
- CCC_NE
- CCC_SW
- CCC_SE

The package pin names for the selected location are displayed next to the dedicated pads in the **Advanced** tab of each CCC. It is important to ensure that the dedicated input pad selected in the configurator GUI matches the board-level clock input pin assignment.

2.1.2 CCC Selection

Make your CCC selection (CCC_0, CCC_1, or BOTH). The Basic, Advanced, and PLL Options tabs will reflect the selections you made by graying-out any CCC tab that is not selected for configuration.

2.1.3 Reset Type

Following reset type options are added for the PLL_RST_N port in the configurator:

1. Synchronous with CLK_50MHZ
2. Async Assert, Sync De-assert

Note:
Reset synchronizer for both the options are implemented internally.

2.1.3.1 Synchronous with CLK_50MHZ

Synchronous with CLK_50MHZ has assertion and de-assertion of reset synchronous to CLK_50MHZ. Default reset type is synchronous reset.

2.1.3.2 Async Assert, Sync De-assert

Async Assert, Sync De-assert has asynchronous assertion and synchronus de-assertion of reset to CLK_50MHZ.

When you select asynchronous reset, the following warning message is shown:

⚠WARNING When selecting the Asynchronous Assertion, Synchronous De - assertion reset type, it is recommended to use an SET mitigated approach when connecting an async reset signal to the PLL_RST_N input of this core. An external reset can enter the device using a CLKBUF macro on a GB# pin, or an RGRESET macro can be manually instantiated and connected to a triplicated internal logic cone. For more information, refer to *App Note AC463*.

2.1.4 CCC Dynamic Configuration

Enable Dynamic configuration —When the **Enable Dynamic configuration** option is selected, an APB target interface is exposed to the FPGA fabric. There is one APB target interface per corner of the fabric, and thus the two CCCs in a given corner share the same dynamic configuration APB interface. This interface can be used to read or modify the CCC configuration registers from the FPGA fabric. Refer to the RTG4 Clocking Resources User Guide for the list of CCC Configuration registers.

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You can choose to have Dynamic configuration for both CCCs. The Dynamic changes cannot alter any parameter that could result in loss of lock.

Note:
It is recommended to configure CCC's in dynamic configuration only when locks of the CCC's are high.

When user performs dynamic configuration its user responsibility to not change the PLL registers as changing these registers will cause Loss of LOCK and which causes recalibration process to trigger again and user written PLL registers will be lost.

2.1.5 Basic Flow

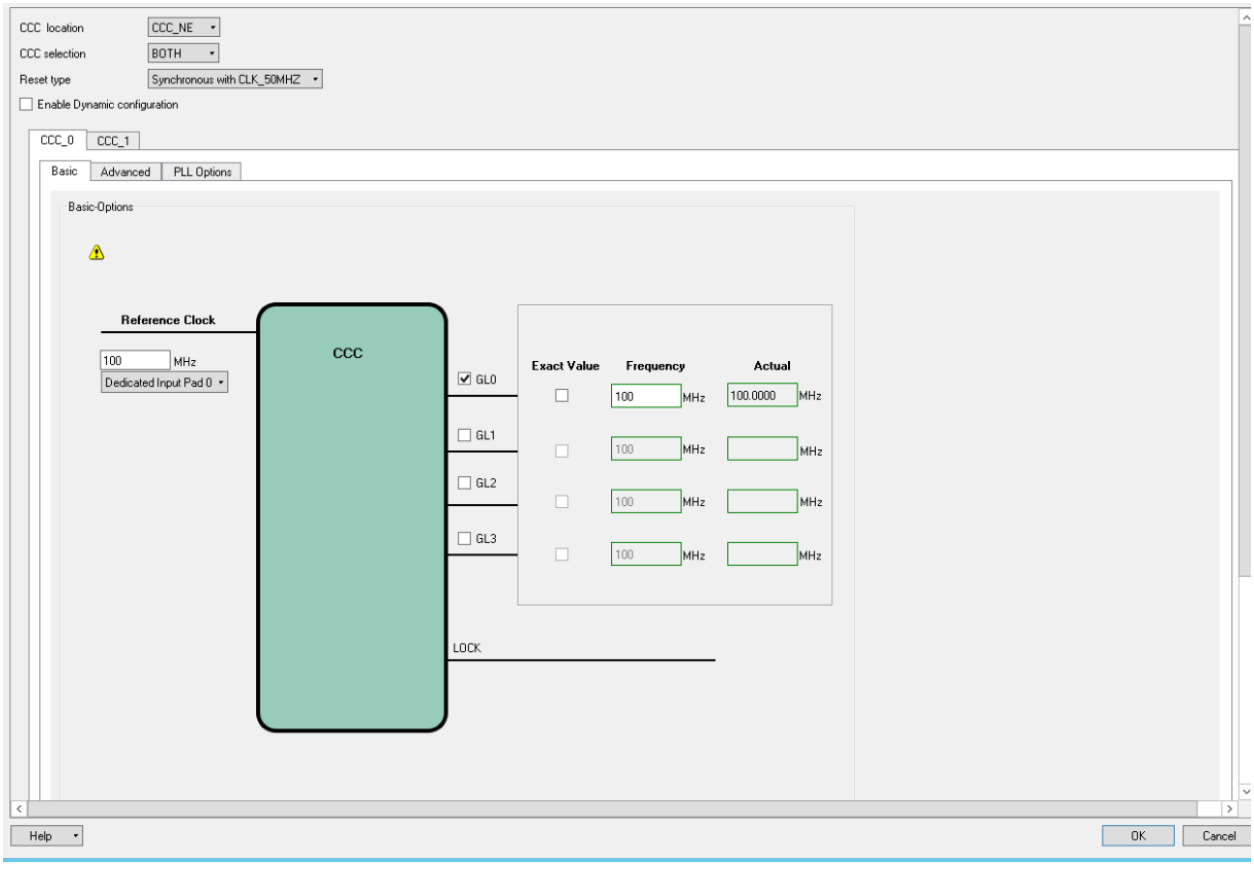
The following flow is recommended to configure the clock generated by the selected CCC for basic use cases:

1. Select the number of desired output clocks (up to four).
2. Set the required output frequency, for each selected output clock.
3. Configure the CCC/PLL reference clock source and frequency. For an oscillator input, a 50 MHz oscillator is available.

In basic configuration, the PLL is always used to generate the output frequency. The feedback of the PLL is internal to the CCC. Click the **Basic** tab of the RTG4 FCCC with Enhanced PLL Calibration Configurator for the basic configuration of the selected CCC.

Actual output frequencies achieved by the RTG4 FCCC with Enhanced PLL Calibration Configurator are shown in the Actual column.

Figure 2-1. Basic CCC Configuration Tab



2.2 Basic Tab

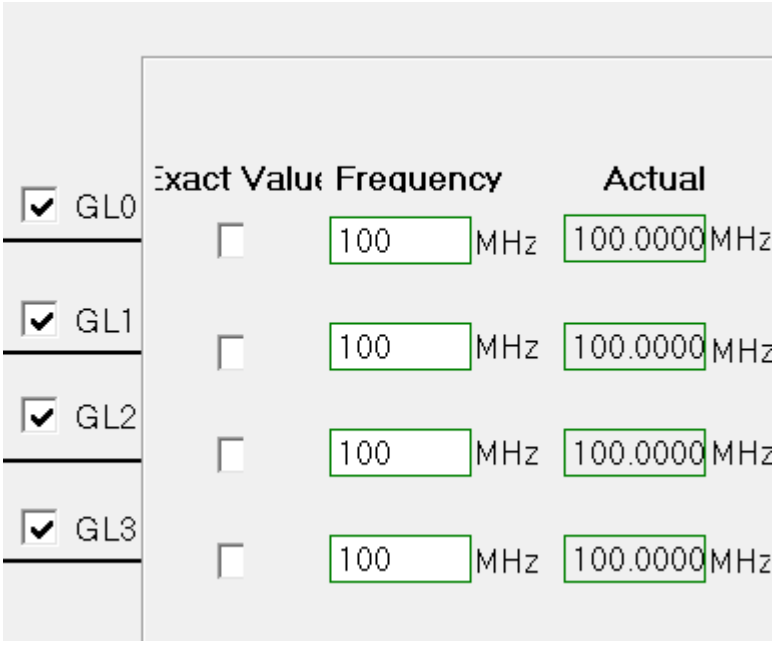
Below are the features available in Basic Tab of the RTG4 FCCC with Enhanced PLL Calibration Configurator.

2.2.1 Output Clocks Selection

The GL0, GL1, GL2, and GL3 output clocks drive a global network in the FPGA fabric. Select at least one of the output clocks to specify the actual value of the configurator.

For output clock frequency, specify the required output clock frequency in the **Frequency** column. The **Actual** column displays the actual value that the configurator can achieve.

Figure 2-2. Output Clocks Selection



2.2.2 Exact Value Option

The RTG4 FCCC with Enhanced PLL Calibration Configurator automatically tries to compute a configuration that meets the frequency requirements and all the internal CCC/PLL constraints. If the configurator is unable to find an exact solution for all requirements, it finds a configuration that globally minimizes the error between the required and actual frequency. When you click the **Exact Value** check box to turn on this option, it forces the configurator to generate the nearest actual frequency with a tolerance of 0.5 kHz.

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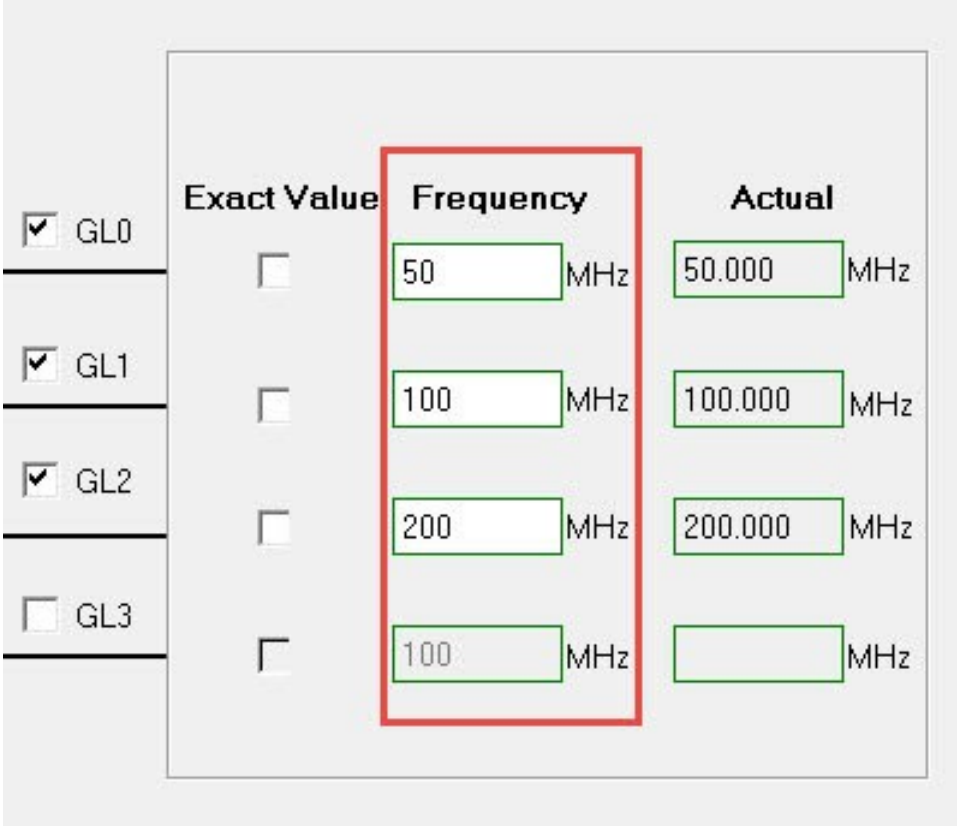
Figure 2-3. Output Clock Frequency



2.2.3 PLL Reference Clock Source and Frequency

The following sources are available from the reference clock menu.

- **Dedicated Input Pad**—The clock source is one of the four regular FPGA I/Os that have a dedicated path to the CCC.
- **Fabric Input**—The clock source is one of the four signals coming from the FPGA Fabric:
  - FPGA Fabric Input 0
  - FPGA Fabric Input 1
  - FPGA Fabric Input 2
  - FPGA Fabric Input 3
- **Oscillators**—The source is from the 50 MHz on-chip oscillator. The RCOSC_50MHZ macro must be manually instantiated and connected to the CCC input pin if selected as the reference clock source.

2.3 Advanced Configuration

For advanced use cases, the following flow is recommended to configure the clock generated by the selected CCC:

Note: Flow proceeds from right to left in the GUI.

1. Select the number of desired output clocks (up to four).
2. Set the required output frequency, for each selected output clock. Output frequency cannot be set when the selected output clock has an input from a clock generated by Clock Recovery Circuitry.
3. Select the desired reference clock input from which the output is derived, for each selected output clock. It can be:
   - One of CCC input clocks (PLL bypass mode), which can be one of four Dedicated Pads or one of four FPGA Fabric Inputs

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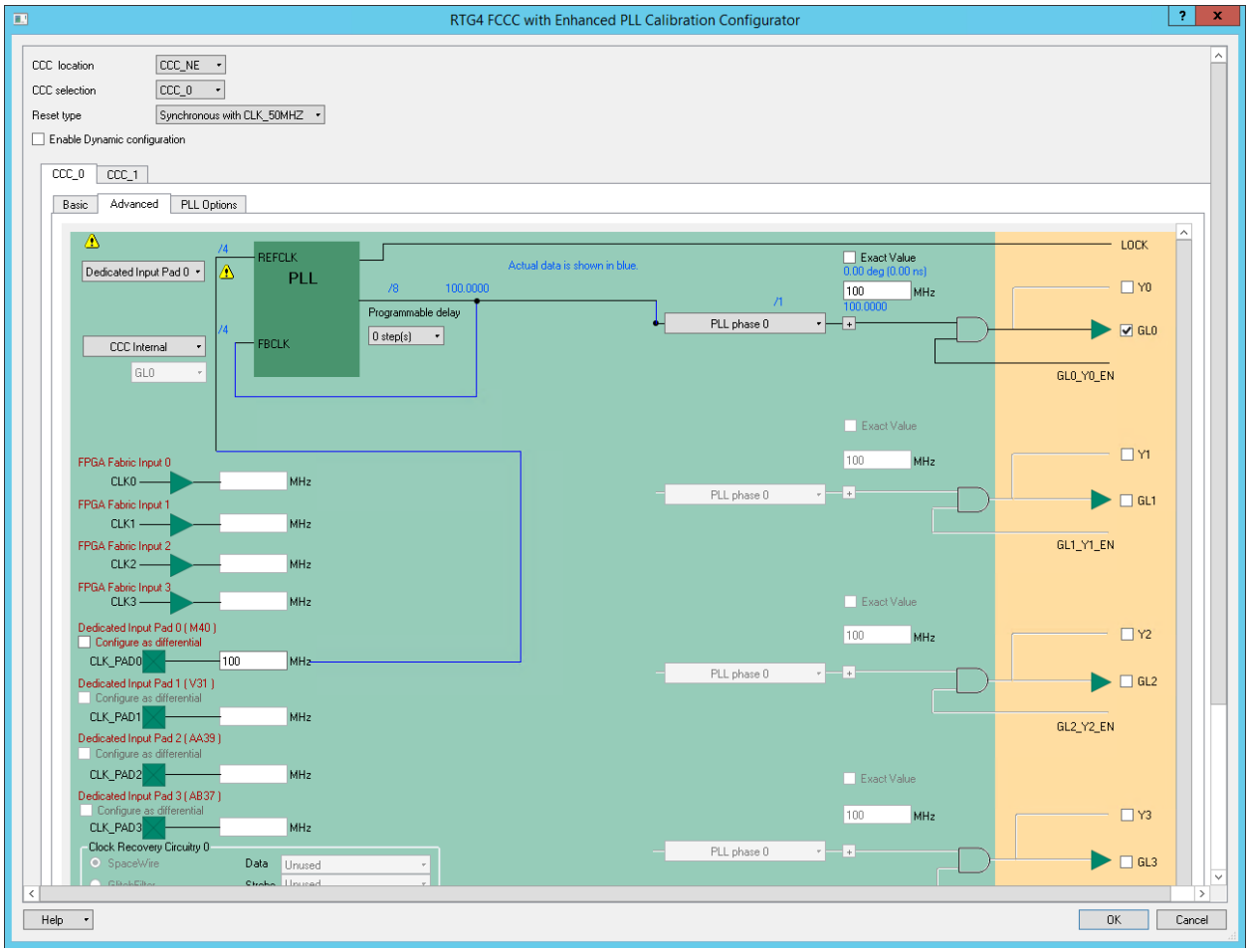
- One of eight PLL output phases
- 50 MHz Oscillator
- One of two Clock Recovery Circuits

4. If required:
   - Select the PLL reference clock source and frequency
   - Select the PLL feedback source
5. Enter the frequency of each selected source clock(s) either as the PLL reference or direct source for the output. The configurator uses those frequencies to compute the division factor of the PLL reference and feedback dividers as well as the GPD dividers.

The configurator automatically tries to compute a configuration that meets the frequency requirements and all the internal CCC/PLL constraints. If the configurator is unable to find an exact solution for all requirements, it finds a configuration that globally minimizes the error between the required and actual frequency.

Actual data (divider settings, PLL output frequency, and actual outputs frequencies) are shown in the **Advanced** tab in blue.

Figure 2-4. Advanced Options



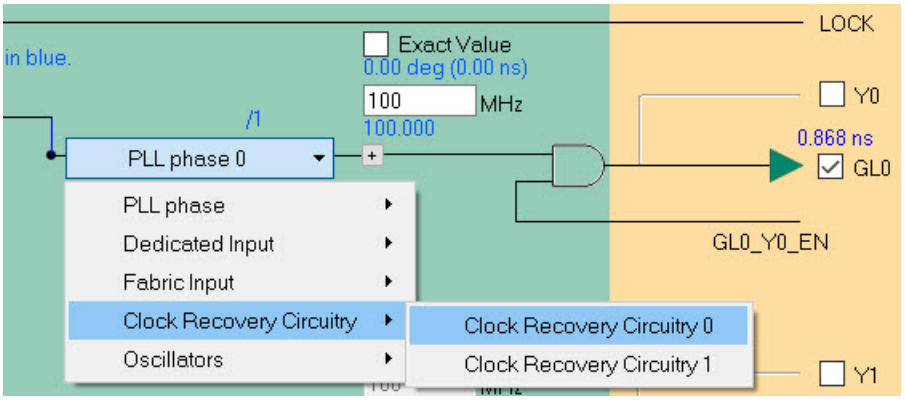
2.4 Advanced Tab

The Advanced tab inherits settings from the Basic tab. Modifying a parameter in the Advanced tab that cannot be reflected in the Basic tab displaying a warning message in the Basic tab.

2.4.1 Output Clocks Selection

You must select at least one of the four output clocks. The GL0, GL1, GL2, and GL3 clocks drive a global network in the FPGA fabric; Y0, Y1, Y2, and Y3 drive local routing resources in the FPGA fabric.

Figure 2-5. Clock Source Selection



The source of the GL[x]/Y[x] clocks can be:

- **PLL** —The PLL block offers eight phases (0° to 315° in 45° steps). The actual phases are highlighted in blue on the configurator dialog. The actual phase is not the same as the selected phase if the output divider is not 1 (`actual_phase = selected_phase / output_divider`).
- **Dedicated Input Pad** —The clock source is one of the four regular FPGA I/Os that have a dedicated path to the CCC. The Configure as differential option allows you to configure any dedicated Input Pad as differential I/O. The package pin names for the selected location are displayed next to the dedicated pads.
- **FPGA Fabric Input** —The clock source is one of the four fabric input signals coming from the FPGA Fabric.
- **Clock Recovery Circuitry** —Two RX Clock Recovery Circuitry blocks are available—Block 0 and Block 1—for each CCC. If the CCC needs to connect to Spacewire or Glitch Filter, configure the source of your GL[x] to use the Clock Recovery Circuitry. The GL[x] output can then be used.
- **Oscillators** —The source is from the on-chip 50 MHz oscillator. The RCOSC_50MHZ macro must be manually instantiated and connected to the CCC input pin if selected as the reference clock source.

2.4.1.1 Output Clock Frequency

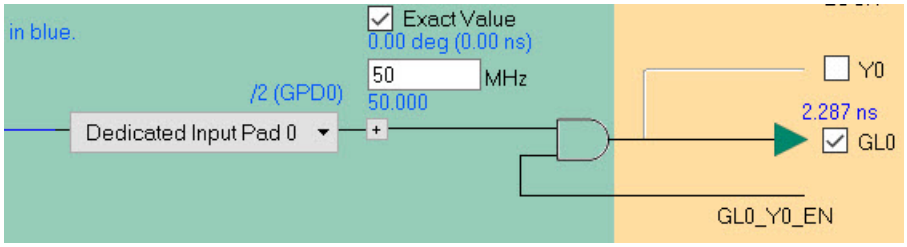
You must specify the required output clock frequency. Those frequencies are used by the RTG4 FCCC with Enhanced PLL Calibration Configurator to compute the configuration of the CCC dividers and PLL to meet the requirements. The dividers and their names are highlighted in blue in the tool.

2.4.1.1.1 Exact Value Option

When you click the **Exact Value** check box to select this option, it forces the RTG4 FCCC with Enhanced PLL Calibration Configurator to generate the nearest actual frequency with a tolerance of 0.5 kHz. If this is not possible, it generates the following error message:

```
Exact Value option is used. No divider combination was found to satisfy the current
settings. Consider adjusting or relaxing the configuration requirements.
```

Figure 2-6. Output Frequency

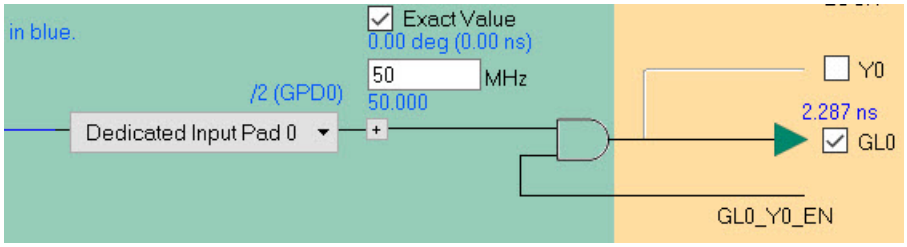


2.4.1.2 Gated Clock Configuration

For GL[x]/Y[x], Clock Gating is an inherent feature for RTG4 CCC. The GL[x]_Y[x]_EN signal gates both the global network driven by the GL[x] and the fabric local routing resource driven by Y[x], where x can be 0, 1, 2, or 3.

Slow GL or Y's must be enabled before the other GL or Y's are enabled, as the lock CCC_[0/1]_LOCK is dependent on the slow [GL/Y] frequency.

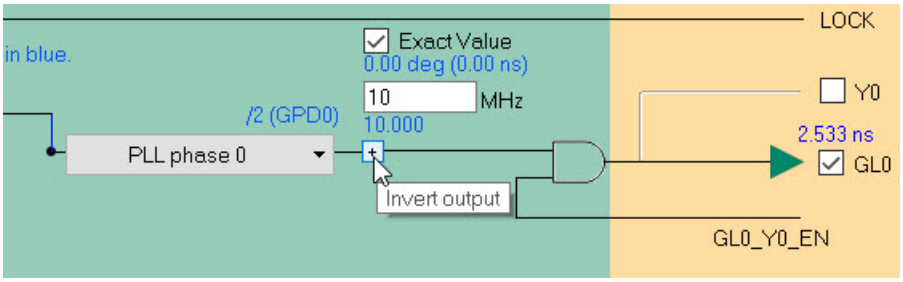
Figure 2-7. GL[x]_Y[x]_EN Signal



2.4.1.3 Inverted Configuration

The output can be inverted if required. The inversion affects GL[x] and Y[x] clock. Click the + sign to get the inverted output.

Figure 2-8. Inverted Configuration



2.4.2 PLL Configuration

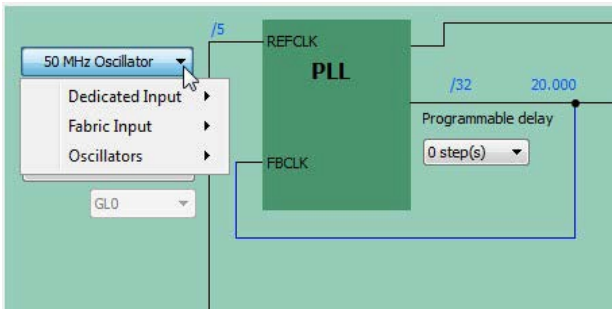
The following section describes the different types of PLL configuration options.

2.4.2.1 PLL Reference Clock Source

The following sources are available from the reference clock menu.

- **Dedicated Input Pad** —The clock source is one of the four regular FPGA I/Os that have a dedicated path to the CCC. The Configure as differential option allows you to configure any dedicated Input Pad as differential I/O. The package pin names for the selected CCC location are displayed next to the dedicated pads.
- **FPGA Fabric Input** —The clock source can be one of the four input signals coming from the FPGA Fabric.
- **Oscillators** —The source is from the on-chip 50 MHz oscillator.

Figure 2-9. PLL Reference Clock Source



2.4.2.2 PLL Feedback Source

If you use the PLL, you can choose to use an internal or external feedback loop, depending on your system level requirements.

Internal Feedback Loop
The following section describes the different types of internal feedback loop.

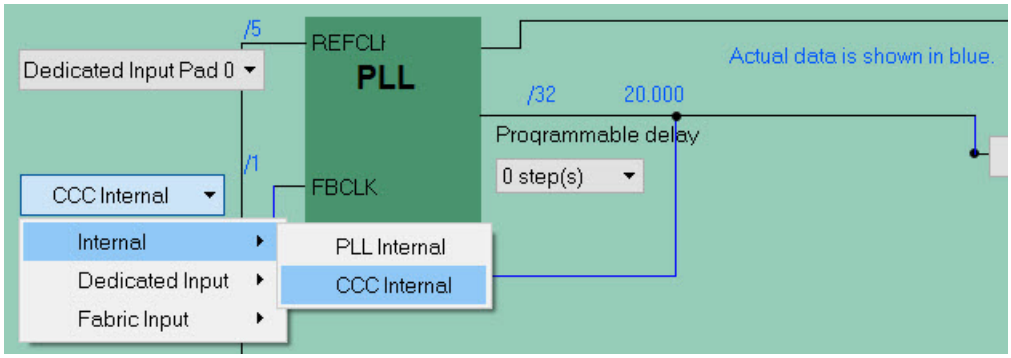
- **CCC Internal**—Default option.
- **PLL Internal**—The triplicated PLL mode is not supported in this version of the RTG4 FCCC with Enhanced PLL Calibration, and thus PLL Internal Feedback mode is not available.
  You can continue to use this core with Single PLL Feedback mode (all other modes except PLL Internal) to prevent the issue described in Customer Notification CN19009.

  Alternatively, the triplicated PLL is available in the RTG4 FCCC core, but will be subject to the issue described in CN19009. Also refer to the RTG4 PLL Radiation Test Report to decide which PLL mode is suitable for your application's reliability requirements.

External Feedback Loop
The external feedback is driven from the selected GL[x]/Y[x] fabric CCC output either through the fabric or externally to the chip.

- **Dedicated Input Pad**—The clock source is one of the four regular FPGA I/Os that have a dedicated path to the CCC.
- **FPGA Fabric Input**—The clock source can be one of the four input signals coming from the FPGA Fabric.

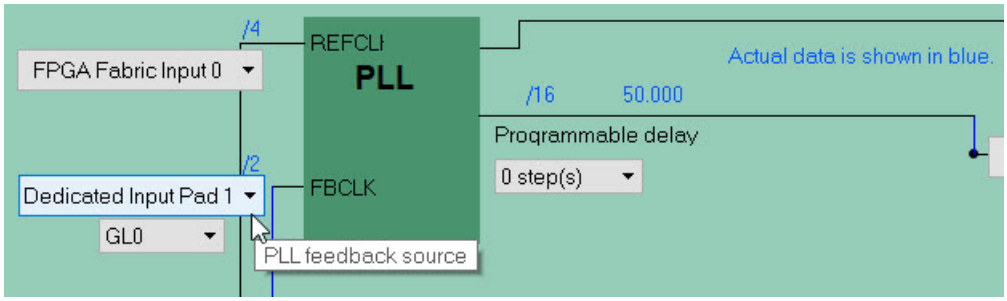
Figure 2-10. Internal Feedback Source



2.4.2.3 PLL External Feedback Source

If you use the PLL with an external feedback source, all engine computations are based on the assumptions that the external feedback is driven from the selected GL[x]/Y[x] fabric CCC output whether through the fabric or externally to the chip.

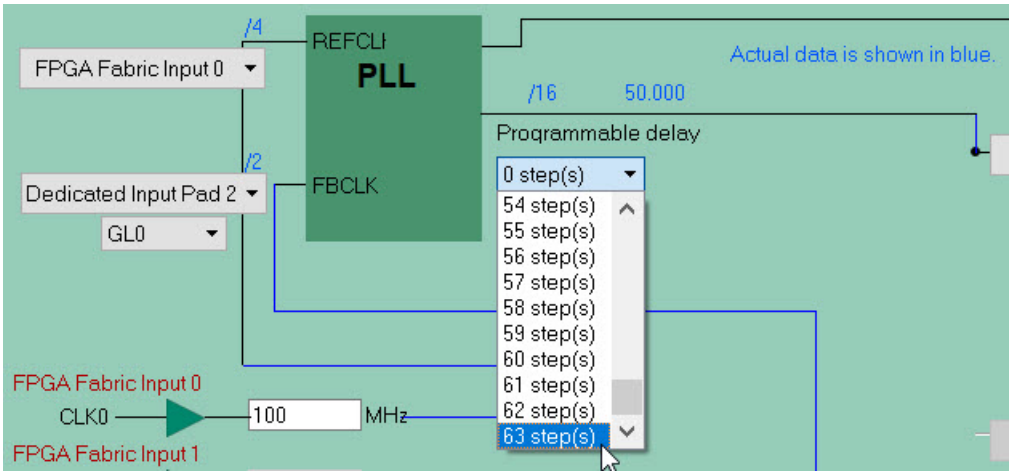
Figure 2-11. PLL External Feedback Source



2.4.2.4 Programmable Delay Line

The programmable delay line enables you to delay (or advance) the PLL output clock with respect to the PLL reference clock by applying a delay to the reference clock path (or feedback path), as shown in figure below.

Figure 2-12. Programmable Delay Line



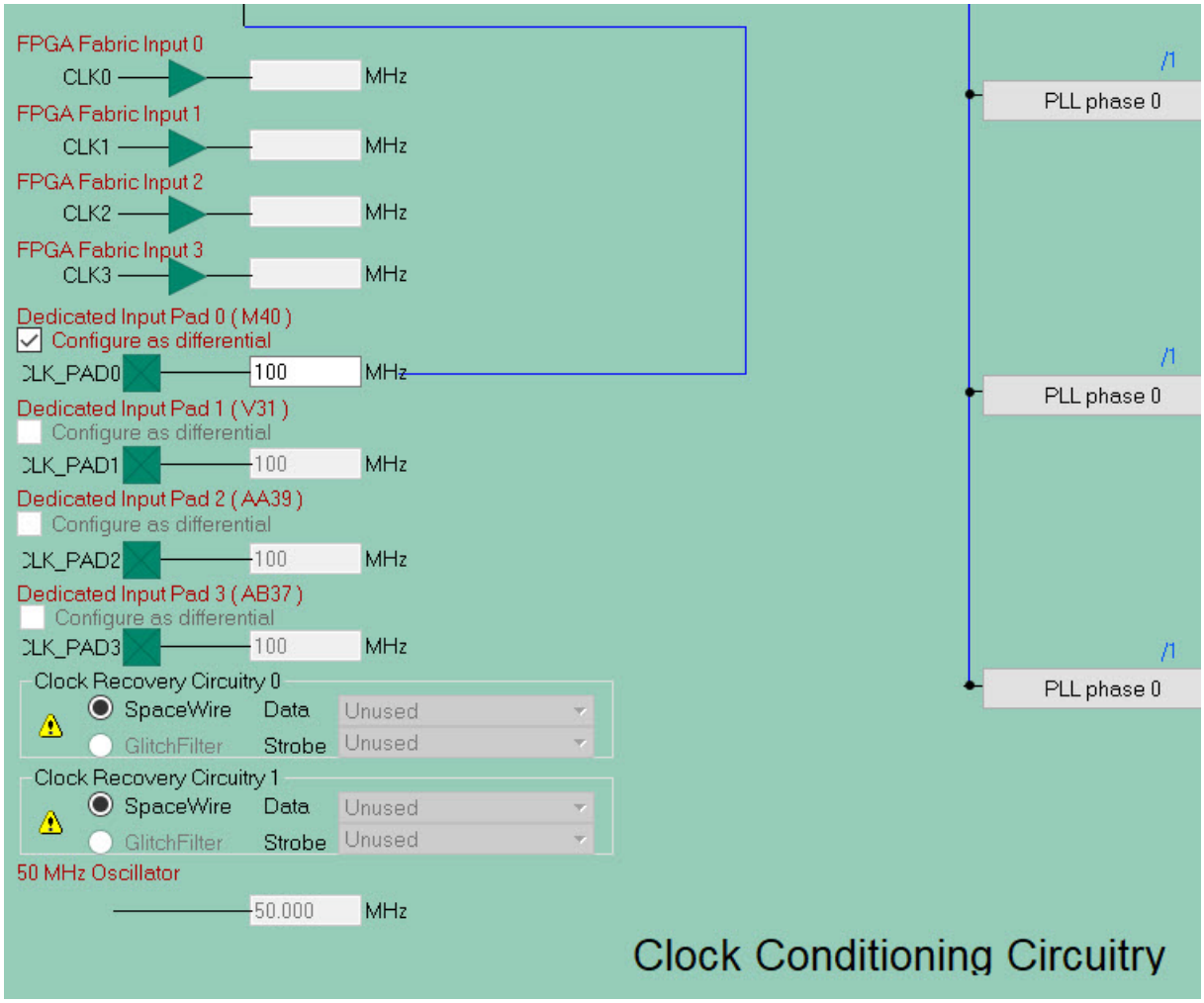
2.4.2.5 Input Clocks Configuration

You must enter the clock frequency of each CCC input used in the configuration as the PLL reference clock, PLL feedback clock, or Output direct connection. These frequencies are used to compute the PLL configuration and divider configuration that meet the output frequencies requirements.

Use Clock Recovery Circuitry to configure the CCC outputs to connect to Spacewire or Glitch Filter.
Note: If you enter a frequency greater than 400 MHz for either PLL reference clock or for other output clock sources, an error message is reported.

The following figure shows the DRCs reported. The dedicated input pad[#] frequency must be less than 400 MHz.

Figure 2-13. Input Clocks Configuration



Dedicated Input Pad

Some of the dedicated inputs to the CCC can be configured to use a differential I/O technology. The location, I/O technology and attributes available for each CCC dedicated input pad is described in the DS0131 RTG4 FPGA Datasheet.

Clock Recovery Circuitry

Each CCC block has two dedicated Clock Recovery Circuitry blocks: Block 0 and Block 1. These can be used in either the SpaceWire mode (Default) or the Glitch Filter mode.

Note:
For RT4G150-ES devices, the Glitch Filter mode is not available, and it is disabled.

The RX clock is based on Data and Strobe Inputs, which are from external dedicated I/Os. The Clock Recovery Circuitry Blocks also include a de-glitching circuit to prevent any undesirable narrow clock pulse at output.

1. You can select the Dedicated input pad 1 and 3 for Data signal. Dedicated input pads 0 and 2 are automatically set as corresponding Strobe signal.
2. The same pair of Dedicated input pads cannot be simultaneously used in Clock Recovery Circuitry.
3. Dedicated input pads, which are used as Data and Strobe signals for Clock Recovery Circuitry block cannot be used as input to PLL Reference Clock and PLL Feedback Clock.
4. You cannot set input frequency values for Dedicated pads, which are configured as Data and Strobe signals for RX Clock Recovery Circuitry.

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5. Clock Recovery Circuitry Block 0 and 1 cannot have the same input source when both are configured for SpaceWire mode.
6. Clock Recovery Circuitry Block 0 and 1 cannot have the same input source when both are configured for Glitch Filter mode.
7. Clock Recovery Circuitry Block 0 and 1 cannot have the same input source when one is configured for SpaceWire mode and the other is configured for Glitch Filter mode.
8. It is valid to select the same input for PLL REFCLK (and CGL secondary clock) and Glitch Filter.

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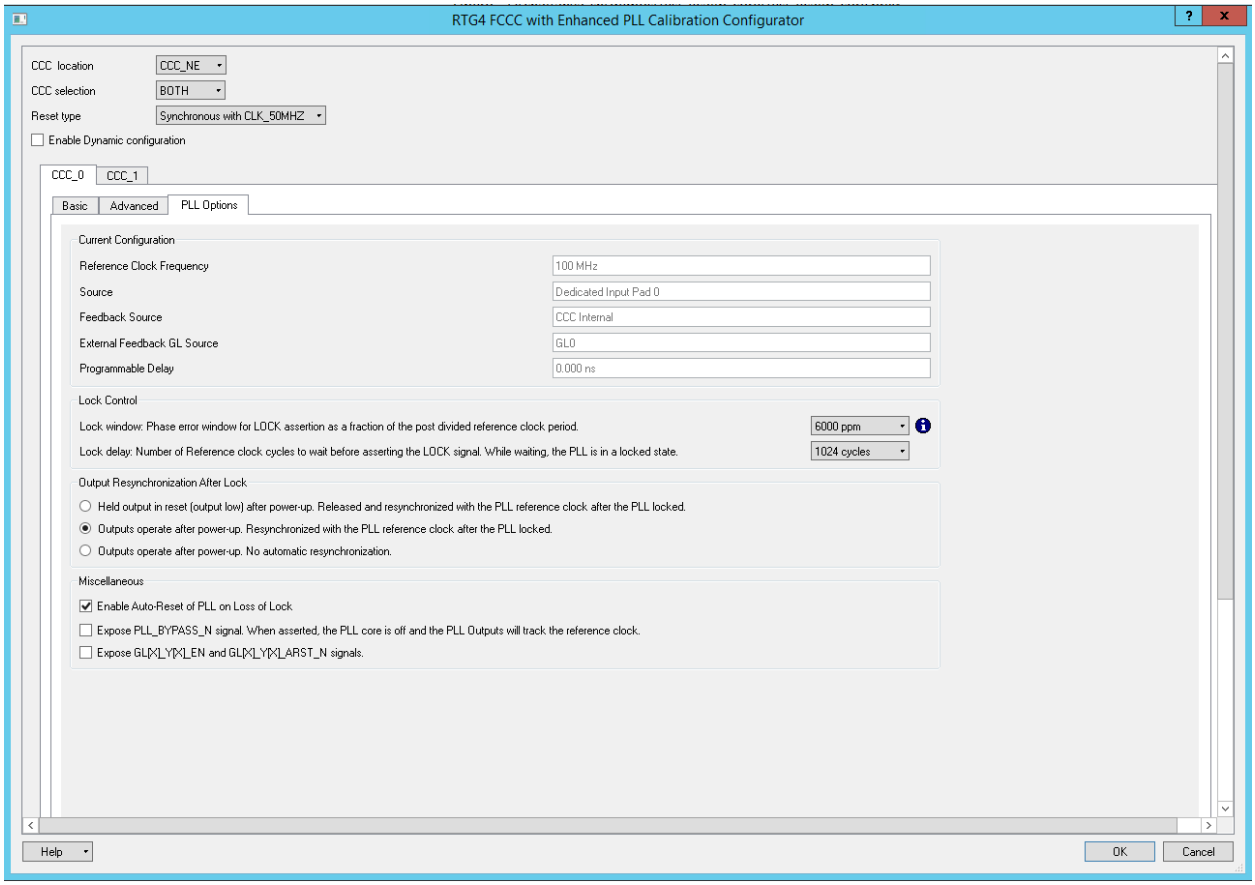
3. PLL Options

The PLL Options tab enables you to configure advanced PLL options, such as output resynchronization and reset signals. Click the **PLL Options** tab in the RTG4 FCCC with Enhanced PLL Calibration Configurator for the selected CCC.

Figure 3-1. PLL Options



The PLL Options summarizes your PLL configuration.

Figure 3-2. PLL Configuration Summary

3.1 Lock Control

Lock window
Enables you to configure the maximum phase error allowed for the PLL to indicate that it has locked. The lock window is expressed as part per million of the post divided reference clock period. Upon generation, the PLL lock window setting is validated against the maximum Phase and Frequency Detector (PFD) rate.

Refer to UG0586: RTG4 FPGA Clocking Resources User Guide for guidelines on selecting the appropriate PLL Lock Window. This is essential for applications that require phase alignment between the CCC input reference clock and the CCC outputs.

Lock delay
Enables you to set the number of Reference (REFCLK) clock cycles to wait before asserting the LOCK signal. While waiting, the PLL is in a locked state.

Important:
Lock Delay is not supported in Simulation. You must not leave the LOCK output ports CCC_0_LOCK and CCC_1_LOCK as dangling because it will cause synthesis optimization that will lead to Derived Constraints to fail during Place and Route.

3.2 Output Resynchronization After Lock Configuration

RTG4 CCC contains four General Purpose Dividers (GPDs). These dividers' source and division settings are automatically configured based on the frequency requirement you specified in the RTG4 FCCC with Enhanced PLL Calibration Configurator. GPDs can be used as the source of any outputs. For example, GPD0 can be used on a path to the GL1 output. It is recommended that you re-synchronize GPDs driven by the PLL output clock after the PLL locks to ensure that the first edge of each GPD is aligned with the PLL reference clock and with each other.

The following sections describe the three different resynchronization options for GPDs/outputs.

Held output in reset (output low) after power-up. Released and resynchronized with the PLL reference clock after the PLL locked

- If enabled, GPD(s) (driven by the PLL) are held in reset low after power-up. Therefore, the output(s) (GLx/Yx) connected to those GPD(s) are held low (or high if inverted) after power-up.
- After the PLL lock, the GPD(s) resets are released synchronously with the PLL reference clock.
- The RTG4 FCCC with Enhanced PLL Calibration Configurator automatically inserts a GPD on each GL/Y output driven by the PLL even if the division factor is 1. This ensures that the GL/Y driven by the PLL is held in reset at power-up.
- Does not apply to the output(s)/GPD(s) on the PLL external feedback path (if any).
- Does not apply for the output(s)/GPD(s) not driven by one of the PLL eight phases output.

Note: In this Resynchronization option, GL output clocks appear before the LOCK signal is asserted. This is because, the RTG4 FCCC instance LOCK is delayed by three clock cycles with the slowest GLx output, before it appear as the final core LOCK.

Outputs operate after power-up. Resynchronized with the PLL reference clock after the PLL locked *(default selection)*

- If enabled, GPD(s) (driven by the PLL) output are operational after power-up. Therefore, the output(s) (GLx/Yx) connected to those GPD(s) are operational after power-up.
- After the PLL lock, the GPD(s) is synchronously reset with the PLL reference clock.
- Does not apply to the output(s)/GPD(s) on the PLL external feedback path (if any).
- Does not apply for the output(s)/GPD(s) not driven by one of the PLL eight phases output.

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Outputs operate after power-up. No automatic resynchronization

- If enabled, the corresponding GPD(s) output operates after power-up. Therefore, the outputs (GLx/Yx) connected to this GPD operates after power-up.
- There is no resynchronization after the PLL lock.
- All GPD(s) directly connected to one of the nine input clocks (bypassing the PLL) are configured in this mode.

Note:
For RT4G150-ES devices, this is the only supported option. If you select other options and click **OK** and **Save**, an error message appears as follows:

```
The selected option of Output Resynchronization after Lock is not supported for ES devices and the only supported option is Outputs Operate after power-up with No automatic resynchronization.
```

Note:
When the CCC is used without the PLL, such as while performing clock frequency division, the GPD(s) require a manual assertion and release of the GPDx_ARST_N input to synchronize the GPD output(s) to the input reference clock, after it gets stable. For example, the lock signal output of an upstream PLL could be used to release the GPDx_ARST_N input so that this CCC's divided output(s) are synchronized to the input clock.

3.3 Miscellaneous Options

- **Enable Auto-Reset of PLL on Loss of Lock**—The option is enabled by default whenever the PLL is used. Disabling this option results in a Warning Exclamation Icon with a tool-tip message that states.

  WARNING The insertion of PLL loss of lock auto-reset logic has been disabled. Auto-reset is helpful in the event the PLL lock is lost during operation. Please review Customer Notifications 19009 and 18009.7 on the Microchip website to understand the consequences of disabling this option.

- **Expose PLL_BYPASS_N signal**—When selected, the input signal PLL_BYPASS_N is exposed to the FPGA Fabric. When this signal is asserted, the PLL core is turned off and the PLL outputs track the reference clock. This signal is active-low.
- **Expose GL[X]_Y[X]_EN and GL[X]_Y[X]_ARST_N signals**—When selected, the GL[X]_Y[X]_EN and GL[X]_Y[X]_ARST_N signals are exposed to the FPGA Fabric. By default, these signals are not exposed.
  Note: In post-layout simulations, if a clock does not appear on GLx output or LOCK de-asserts unexpectedly even though the reference clock input is available, then add **transport_path_delays** switch in VSIM command and select the check box **Disable pulse filtering** option in VSIM commands of Libero project settings. Re-run the simulation with this and then you must see check the GLx and LOCK output.

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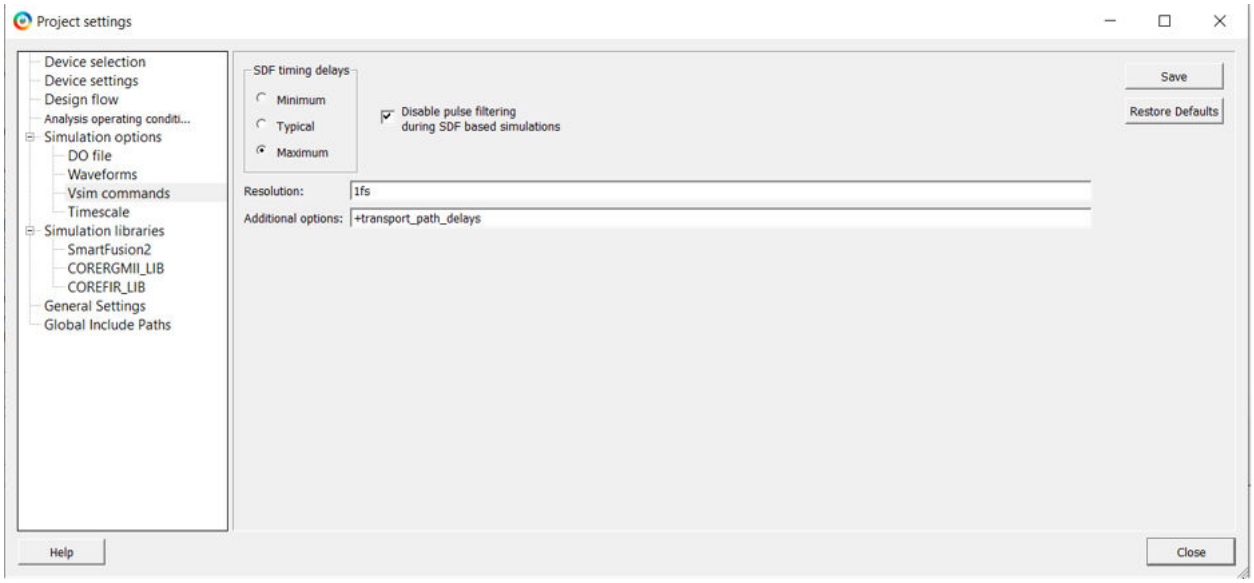
Figure 3-3. Libero Project Settings



Calibration note during Simulation
The following message appears during simulations.

```
# ************************NOTE*****************************
# This message can be safely ignored during the time
# period when the PLL used in the RTG4FCCCECALIB,
# RTG4 FDDR, or RTG4 SERDES PCIe/XAUI core is
# performing VCO calibration. During this time, the
# calibration logic dynamically configures the clock
# conditioning circuitry dividers to run the PLL VCO at
# greater than 1.5x the desired frequency. Refer to the
# following User Guides for more information about the
# Enhanced PLL Calibration:
# - RTG4 Clocking Resources User Guide (UG0586), Enhanced PLL Calibration Fabric IP section.
# - RTG4 FPGA High-Speed Serial Interfaces User Guide (UG0567), Calibration Initialization
section.
# - RTG4 FPGA DDR Memory Controller User Guide (UG0573), Initialization section.
# ************************Attention***********************
# The output frequency of PLLOUT_0 is too fast!
# The frequency on the output is above 500MHz. The PLL
# is operating out of spec, therefore the current sim-
# ulation results may not be accurate!
# This is likely due to the setting of the DIVR, DIVF,
# DIVQ, or the frequency of REFCK. Please check these
# values and rerun the simulation.
# Instance: Top_JJS.Top_0.RTG4FCCCECALIB_C0_0.RTG4FCCCECALIB_C0_0.CCC_INST_0.u_pll.u_pll.
Simulation time is 180813668
# ************************************************************
```

3.4 Recommendations for Dynamic Configuration

Following are the recommendations for dynamic configuration:

1. It is recommended that user shouldn't perform register read/write when LOCK signal is low (when calibration/re calibration is in progress).
2. User must ensure that register write operation is successful by reading back the same register. If user doesn't get the expected value then user should write the register again.
3. The list of registers user must not access when Enable Auto-Reset of PLL on Loss of Lock is selected.

Table 3-1. PLL registers(not to be altered)

Register Name	Address	Description
FCCC_RFMUX_CR	0x01	RFMUX Configuration register
FCCC_RFDIV_CR	0x02	RFDIV Configuration register
FCCC_FBMUX_CR	0x03	FBMUX Configuration register
FCCC_FBDIV_CR	0x04	FBDIV Configuration register
FCCC_PLL_CR0	0x16	PLL lock window Configuration register
FCCC_PLL_CR1	0x17	PLL lock counter configuration and lock status register
FCCC_PLL_CR2	0x18	Write one pulse for reload of Flash bits
FCCC_PLL_CR3	0x1B	PLL internal or external feedback path selection register
FCCC_GPDS_SYNC_CR	0x1C	GPDs outputs realignment request Configuration register
FCCC_PLL_CR4	0x1D	PLL internal output divider Configuration register
FCCC_PLL_CR5	0x1F	PLL internal reference clock divider Configuration register
FCCC_PLL_CR6	0x20	PLL internal feedback clock divider Configuration register
FCCC_PLL_CR7	0x21	PLL loop filter range Configuration register
FCCC_PDLY_CR	0x26	Programmable delay elements Configuration register

3.5 Clock Frequency Requirements

You must specify the clock source frequency. Note the following frequency requirements:

- The On-chip 50 MHz Oscillator clock frequency is fixed at 50 MHz.
- The input clock frequency is driven by CLK_50MHz input and this must be 50 MHz.
- PLL reference clock frequency must be between 10 MHz and 200 MHz.
- Output clock frequencies must be less than 400 MHz.
- Input used in bypass mode frequency must be less than 400 MHz.
- In Dynamic configuration, the same clock CLK_50MHz is used as input to the APB interface clock (APB_S_PCLK).

3.6 Constraints

After generating the core, the following constraint files are generated automatically.

- Clocks and False paths related constraints are generated in `.sdc` file.
- Constraints related to SET mitigation are generated in `.ndc` file.

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- A clock constraint for CLK50_MHZ, which is an input clock for soft logic that performs calibration, is automatically generated if the source is an internal oscillator or CCC. Otherwise, it is user's responsibility to add a proper constraint.

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4. Port Description

The following table provides a list of Fabric CCC ports and description.

Table 4-1. Fabric CCC Port Description

Port Name	Direction	Polarity	Description
CCC_[0/1]_CLK0_PAD	Input	—	Input clock when using Dedicated Input Pad 0 configured as a single-ended I/O.
CCC_[0/1]_CLK0_[PADP and PADN]	Input	—	Input clock when using Dedicated Input Pad 0 configured as differential I/O. P side and N side.
CCC_[0/1]_CLK1_PAD	Input	—	Input clock when using Dedicated Input Pad 1 configured as a single-ended I/O.
CCC_[0/1]_CLK1_[PADP and PADN]	Input	—	Input clock when using Dedicated Input Pad 1 configured as differential I/O. P side and N side.
CCC_[0/1]_CLK2_PAD	Input	—	Input clock when using Dedicated Input Pad 2 configured as a single-ended I/O.
CCC_[0/1]_CLK2_[PADP and PADN]	Input	—	Input clock when using Dedicated Input Pad 2 configured as differential I/O. P side and N side.
CCC_[0/1]_CLK3_PAD	Input	—	Input clock when using Dedicated Input Pad 3 configured as a single-ended I/O.
CCC_[0/1]_CLK3_[PADP and PADN]	Input	—	Input clock when using Dedicated Input Pad 3 configured as differential I/O. P side and N side.
CCC_[0/1]_CLK0_SPWR_STROBE_[PADP and PADN]	Input	—	Input Clock when Dedicated pad 0 is used as input to Strobe of Clock Recovery Circuitry in differential-mode. SpaceWire Mode only.
CCC_[0/1]_CLK1_SPWR_DATA_[PADP and PADN]	Input	—	Input Clock when Dedicated Pad 1 is used as input to Data of Clock Recovery Circuitry in differential-mode. SpaceWire Mode only.
CCC_[0/1]_CLK2_SPWR_STROBE_[PADP and PADN]	Input	—	Input Clock when Dedicated pad 2 is used as input to Strobe of Clock Recovery Circuitry in differential-mode. SpaceWire Mode only.
CCC_[0/1]_CLK3_SPWR_DATA_[PADP and PADN]	Input	—	Input Clock when Dedicated Pad 3 is used as input to Data of Clock Recovery Circuitry in differential-mode. SpaceWire Mode only.
CCC_[0/1]_CLK0_SPWR_STROBE_PAD	Input	—	Input Clock when Dedicated pad 0 is used as input to Strobe of Clock Recovery Circuitry configured as single-ended I/O. SpaceWire Mode only.
CCC_[0/1]_CLK1_SPWR_DATA_PAD	Input	—	Input Clock when Dedicated pad 1 is used as input to Data of Clock Recovery Circuitry configured as single-ended I/O. SpaceWire Mode only.
CCC_[0/1]_CLK2_SPWR_STROBE_PAD	Input	—	Input Clock when Dedicated pad 2 is used as input to Strobe of Clock Recovery Circuitry configured as single-ended I/O. SpaceWire Mode only.

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.....continued

Port Name	Direction	Polarity	Description
CCC_[0/1]_CLK3_SPWR_DATA_PAD	Input	—	Input Clock when Dedicated pad 3 is used as input to Data of Clock Recovery Circuitry configured as single-ended I/O. SpaceWire Mode only.
CCC_[0/1]_CLK0	Input	—	Input clock from FPGA core when using FPGA Fabric Input 0.
CCC_[0/1]_CLK1	Input	—	Input clock from FPGA core when using FPGA Fabric Input 1.
CCC_[0/1]_CLK2	Input	—	Input clock from FPGA core when using FPGA Fabric Input 2.
CCC_[0/1]_CLK3	Input	—	Input clock from FPGA core when using FPGA Fabric Input 3.
CCC_[0/1]_RCOSC_50MHZ	Input	—	Input clock when using 50 MHz Oscillator.
CCC_[0/1]_GL0	Output	—	Generated clock driving FPGA fabric global network 0.
CCC_[0/1]_GL1	Output	—	Generated clock driving FPGA fabric global network 1.
CCC_[0/1]_GL2	Output	—	Generated clock driving FPGA fabric global network 2.
CCC_[0/1]_GL3	Output	—	Generated clock driving FPGA fabric global network 3.
CCC_[0/1]_GL0_Y0_EN	Input	High	Enable signal for the clock driving FPGA fabric global network 0 (GL0) and fabric local routing (Y0) network 0.
CCC_[0/1]_GL1_Y1_EN	Input	High	Enable signal for the clock driving FPGA fabric global network1 (GL1) and fabric local routing (Y1) network 1.
CCC_[0/1]_GL2_Y2_EN	Input	High	Enable signal for the clock driving FPGA fabric global network 2 (GL2) and fabric local routing (Y2) network 2.
CCC_[0/1]_GL3_Y3_EN	Input	High	Enable signal for the clock driving FPGA fabric global network 3 (GL3) and fabric local routing (Y3) network 3.
CCC_[0/1]_GL0_Y0_ARST_N	Input	Low	(GL0/Y0) CGL reset signal. Asynchronous reset signal.
CCC_[0/1]_GL1_Y1_ARST_N	Input	Low	(GL1/Y1) CGL reset signal. Asynchronous reset signal.
CCC_[0/1]_GL2_Y2_ARST_N	Input	Low	(GL2/Y2) CGL reset signal. Asynchronous reset signal.
CCC_[0/1]_GL3_Y3_ARST_N	Input	Low	(GL3/Y3) CGL reset signal. Asynchronous reset signal.
CCC_[0/1]_Y0	Output	—	Generated clock driving FPGA fabric local routing resource.

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.....continued			
Port Name	**Direction**	**Polarity**	**Description**
CCC_[0/1]_Y1	Output	—	Generated clock driving FPGA fabric local routing resource.
CCC_[0/1]_Y2	Output	—	Generated clock driving FPGA fabric local routing resource.
CCC_[0/1]_Y3	Output	—	Generated clock driving FPGA fabric local routing resource.
CCC_[0/1]_RX0_DATA_PORT	Output	—	Output port for RX0 data. Same signal that is driving the RX0 Spacewire clock recovery data input.
CCC_[0/1]_RX1_DATA_PORT	Output	—	Output port for RX1 data. Same signal that is driving the RX1 Spacewire clock recovery data input.
CCC_[0/1]_LOCK	Output	High	PLL Lock indicator signal. This signal is asserted (lock) high.
CCC_[0/1]_PLL_BYPASS_N	Input	Low	Powers-down the PLL core and bypasses it such that PLL_OUT tracks reference clock. This has higher priority than reset.
CCC_[0/1]_PLL_POWERDOWN_N	Input	Low	Powers-down the PLL for the lowest quiescent current and the PLL outputs are low. This has higher priority than reset and bypass.
PLL_RST_N	Input	Low	PLL_RST_N is internally synchronized with CLK_50MHZ. Synchronization method can be selected using Reset type option. If Reset type selected is Synchronous then assertion and de-assertion of reset is synchronous to CLK_50MHZ. For successful synchronization, PLL_RST_N must be asserted for a minimum of three clock cycles of CLK_50MHZ. If Reset type selected is Async-Assert, Sync-Deassert then assertion of reset is asynchronous and de-assertion is synchronous with CLK_50MHZ.
READY_VDDPLL	Input	High	Tie to High if you are certain that VDDPLL not the last supply to ramp up. Otherwise, connect to a circuit that delays the assertion of VDDPLL by 73 ms as described in the RTG4 Clocking Resources User Guide.
CLK50_MHZ	Input	—	Input clock for soft logic that performs calibration at power-up or when the PLL is reset. The frequency of this clock must be 50 MHz max. You may connect to the GLx output of any CCC that is distributing the RCOSC_50MHZ signal. You cannot directly connect a RCOSC_50MHZ macro to this input port. Alternatively, an external free-running oscillator clock can be used as long as the frequency is 50 MHz or less. CLK_50MHZ will be used for the APB3 interface when "Enable Dynamic configuration" is selected in the configurator.
Fabric CCC Configuration bus Interface Signals – APB3 bus Interface			

.....continued			
Port Name	**Direction**	**Polarity**	**Description**
APB_S_PRESET_N	Input	Low	APB3 interface is a active-low reset signal. You have to synchronize APB_S_PRESET_N with CLK_50MHZ externally.
APB_S_PADDR[8:2]	Input	—	APB3 interface is an address bus. This port is used to address fabric CCC internal registers. APB_S_PADDR shall be synchronous with CLK_50MHZ.
APB_S_PSEL	Input	—	APB3 interface target is a select signal. APB_S_PSEL shall be synchronous with CLK_50MHZ.
APB_S_PENABLE	Input	High	APB3 interface is a strobe signal to indicate the second cycle of an APB3 transfer. APB_S_PENABLE shall be synchronous with CLK_50MHZ.
APB_S_PWRITE	Input	—	APB3 interface is a read/write-control signal. When high, this signal indicates an APB3 write access and when low, a read access. APB_S_PWRITE shall be synchronous with CLK_50MHZ.
APB_S_PWDATA[7:0]	Input	—	APB3 interface is a write data bus. APB_S_PWDATA shall be synchronous with CLK_50MHZ.
APB_S_PRDATA[7:0]	Output	—	APB3 interface is a read data bus. APB_S_PRDATA is synchronous with CLK_50MHZ.
APB_S_PREADY	Output	—	APB3 interface is a ready indication output to initiator. APB_S_PREADY is synchronous with CLK_50MHZ.
APB_S_PSLVERR	Output	—	APB3 interface error indication signal. APB_S_PSLVERR is synchronous with CLK_50MHZ.

Note: APB_S_PCLK is removed and it is from CLK_50MHz.

5. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
D	12/2021	• Updated 2.2.1. Output Clocks Selection. • Removed "Output Clock Frequency" section. • Updated 3.3. Miscellaneous Options.
C	08/2021	• Updated 3.6. Constraints. • Added Note in 3.2. Held output in reset (output low) after power-up. Released and resynchronized with the PLL reference clock after the PLL locked.
B	08/2021	• Added 1. Calibration. • Added 2.1.3. Reset Type. • Added 3.6. Constraints. • Added Note regarding APB_S_PCLK. • Updated Introduction. • Updated Table 4-1.
A	04/2021	2.4.1.2. Gated Clock Configuration - Added information about slow GL or Y's. 3.3. Miscellaneous Options - Added message that appears during simualtions. 3.1. Lock Control - Added note that users should not leave the LOCK output ports CCC_0_LOCK and CCC_1_LOCK dangling because it will cause synthesis optimization that will lead to Derive Constraints failure during Place and Route.

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