Revision History

**Revision 2.0**
Updated the contact information and added this revision history.

**Revision 1.0**
First publication of this document.
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Introduction

The RTG4 FCCC with Enhanced PLL Calibration Configurator generated circuit includes soft logic that performs calibration at power-up or when the PLL is reset. This ensures that the PLL lock is stable during normal operation within the supported RTG4 operating junction temperature range.

This document describes the RTG4 FCCC with Enhanced PLL Calibration Configurator. This configurator enables the configuration of two CCCs—CCC_0 and CCC_1. You must configure one or both of the CCCs. Enhanced lock PLL calibration soft logic is implemented for all configured CCCs.

The enhanced PLL calibration removes any Fabric PLL lock stability dependence on the operating junction temperature across the supported RTG4 operating temperature range for non-triplicated PLL. The configuration options for the RTG4 FCCC with Enhanced PLL Calibration Configurator are described in Chapter 1 – Configuration Options.

Figure 1 shows the top view of the RTG4 FCCC with Enhanced PLL Calibration Configurator.

Figure 1 • RTG4 FCCC with Enhanced PLL Calibration Configurator (CCC_0 selected)
The RTG4 FCCC with Enhanced PLL Calibration Configurator enables you to configure two of eight CCC/PLL blocks available on RTG4 devices (Figure 2).

The Fabric CCC can condition up to eleven input clocks to generate up to four clocks. Each of the four output clocks can directly drive the global network and/or the local routing network.

Each of the four output clocks can be driven by:

- One of eight PLL output phases
- One of four General Purpose Divider (GPD) outputs
- One of eleven input clocks:
  - Dedicated Input Pad 0
  - Dedicated Input Pad 1
  - Dedicated Input Pad 2
  - Dedicated Input Pad 3
  - FPGA Fabric Input 0
  - FPGA Fabric Input 1
  - FPGA Fabric Input 2
  - FPGA Fabric Input 3
  - 50 MHz On-chip Oscillator
  - Clock Recovery Circuitry 0
  - Clock Recovery Circuitry 1
The reference clock of the PLL can be driven by one of nine input clocks:

• Four Dedicated Input Pads
• Four FPGA Fabric Inputs
• 50 MHz On-chip Oscillator

Each of the four GPDs can be driven by either one of nine input clocks (Dedicated Input Pad 0 through 3, Dedicated Fabric Input 0 through 3 and the 50 MHz Oscillator) or one of eight PLL output phases. The configuration of the CCC can be broken down into the following three major blocks:

• Output Clocks GL[x]/Y[x] configuration
  – Clock source selection
  – Clocks frequency and phase configurations

• PLL configuration
  – PLL clock generation configuration including external feedback support

• General Purpose Divider (GPD) configuration
1 – Configuration Options

Basic Configuration
This section describes basic configuration of the RTG4 FCCC with Enhanced PLL Calibration Configurator.

CCC Location
You must choose a physical location for the CCC pair:
- CCC_NW
- CCC_NE
- CCC_SW
- CCC_SE
The package pin names for the selected location are displayed next to the dedicated pads in the Advanced tab of each CCC. It is important to ensure that the dedicated input pad selected in the configurator GUI matches the board-level clock input pin assignment.

CCC Selection
Make your CCC selection (CCC_0, CCC_1, or BOTH). The Basic, Advanced, and PLL Options tabs will reflect the selections you make by graying-out any CCC tab not selected for configuration.

CCC Dynamic Configuration
Enable Dynamic configuration - When selected, an APB slave interface is exposed to the FPGA fabric. There is one APB slave interface per corner of the fabric, and thus the two CCCs in a given corner share the same dynamic configuration APB interface. This interface can be used to read or modify the CCC configuration registers from the FPGA fabric. Refer to the RTG4 Clocking Resources User Guide for the list of CCC Configuration registers.
You can choose to have Dynamic configuration for both CCCs. The Dynamic changes cannot alter any parameter that could result in loss of lock.

Basic Flow
The following flow is recommended to configure the clock generated by the selected CCC for basic use cases:
1. Select the number of desired output clocks (up to four).
2. For each selected output clock, set the required output frequency.
3. Configure the CCC/PLL reference clock source and frequency. For Oscillator input, a 50 MHz Oscillator is available.
In basic configuration, the PLL is always used to generate the output frequency. The feedback of the PLL is internal to the CCC.
Click the Basic tab of the RTG4 FCCC with Enhanced PLL Calibration Configurator for the basic configuration of the selected CCC (Figure 1-1).
Actual output frequencies achieved by the RTG4 FCCC with Enhanced PLL Calibration Configurator are shown in the Actual column.

Figure 1-1 • Basic CCC Configuration Tab (CCC_0 selected)
Basic Tab

Output Clocks Selection
You must select at least one of the output clocks (Figure 1-2). The GL0, GL1, GL2 and GL3 output clocks drive a global network in the FPGA fabric.

![Output Clocks Selection](image)

**Figure 1-2 • Output Clocks Selection**

Output Clock Frequency
You must specify the required output clock frequency (Figure 1-3). Those frequencies are used by the RTG4 FCCC with Enhanced PLL Calibration configurator to compute the configuration of the CCC dividers and PLL to meet the requirements. Actual column displays the actual value the configurator was able to achieve.

Exact Value Option
The RTG4 FCCC with Enhanced PLL Calibration configurator automatically tries to compute a configuration that meets the frequency requirements and all the internal CCC/PLL constraints. If the configurator is unable to find an exact solution for all requirements, it finds a configuration that globally minimizes the error between the required and actual frequency. When you click the Exact Value checkbox to turn on this option, it forces the configurator to generate the nearest actual frequency with a tolerance of 0.5 KHz.
PLL Reference Clock Source and Frequency

The following sources are available from the reference clock pull-down menu.

**Dedicated Input Pad** - The clock source is one of the four regular FPGA I/Os that have a dedicated path to the CCC.

**Fabric Input** - The clock source is one of the four signals coming from the FPGA Fabric:
- FPGA Fabric Input 0
- FPGA Fabric Input 1
- FPGA Fabric Input 2
- FPGA Fabric Input 3

**Oscillators** - The source is from the 50MHz on-chip oscillator. The RCOSC_50MHZ macro must be manually instantiated and connected to the CCC input pin, if selected as the reference clock source.

![Figure 1-3 • Output Clock Frequency](image)

<table>
<thead>
<tr>
<th>Exact Value</th>
<th>Frequency</th>
<th>Actual</th>
</tr>
</thead>
<tbody>
<tr>
<td>GL0</td>
<td>50 MHz</td>
<td>50.000 MHz</td>
</tr>
<tr>
<td>GL1</td>
<td>100 MHz</td>
<td>100.000 MHz</td>
</tr>
<tr>
<td>GL2</td>
<td>200 MHz</td>
<td>200.000 MHz</td>
</tr>
<tr>
<td>GL3</td>
<td>100 MHz</td>
<td>MHz</td>
</tr>
</tbody>
</table>
Advanced Configuration

For advanced use-cases, the following flow is recommended to configure the clock generated by the selected CCC (flow proceeds from right to left in the GUI):

1. Select the number of desired output clocks (up to four).
2. For each selected output clock, set the required output frequency. Output frequency cannot be set when the selected output clock has an input from Clock generated by Clock Recovery Circuitry.
3. For each selected output clock, select the desired reference (input) clock from which the output will be derived. It can be:
   - One of CCC input clocks (PLL bypass mode), which can be one of four Dedicated Pads or one of four FPGA Fabric Inputs
   - One of 8 PLL output phases
   - 50 MHz Oscillator
   - One of two Clock Recovery Circuits
4. If required:
   - Select the PLL reference clock source and frequency
   - Select the PLL feedback source
5. Enter the frequency of each selected source clock(s) (either as the PLL reference or direct source for the output). The configurator uses those frequencies to compute the division factor of the PLL reference and feedback dividers as well as the GPD dividers.

The configurator automatically tries to compute a configuration that meets the frequency requirements and all the internal CCC/PLL constraints. If the configurator is unable to find an exact solution for all requirements, it finds a configuration that globally minimizes the error between the required and actual frequency.

Actual data (divider settings, PLL output frequency, and actual outputs frequencies) are shown in the advanced dialog in blue (Figure 1-4).

Click the Advanced tab in the RTG4 FCCC with Enhanced PLL Calibration Configurator for Advanced configuration.
Advanced Tab

The advanced configuration tab inherits settings from the basic tab. Modifying a parameter in the Advanced tab that cannot be reflected in the Basic tab results in a warning in the Basic tab.

Output Clocks Selection

You must select at least one of the output clocks. The GL0, GL1, GL2 and GL3 clocks drive a global network in the FPGA fabric; Y0, Y1, Y2 and Y3 drive local routing resources in the FPGA fabric.
**Clock Source Selection**

The source of the GL[x]/Y[x] clocks (Figure 1-5) can be:

**PLL** - The PLL block offers eight phases (0 deg to 315 deg in 45 deg steps). The actual phases are highlighted in blue on the configurator UI. The actual phase is not the same as the selected phase if the output divider is not 1 (actual_phase = selected_phase / output_divider).

**Dedicated Input Pad** - The clock source is one of the four regular FPGA I/O's that has a dedicated path to the CCC. The Configure as differential option allows you to configure any dedicated Input Pad as differential I/O. The package pin names for the selected location are displayed next to the dedicated pads.

**FPGA Fabric Input** - The clock source is one of the four fabric input signals coming from the FPGA Fabric.

**Clock Recovery Circuitry** - Two RX Clock Recovery Circuitry Blocks are available: Block 0 and Block 1 for each CCC. If the CCC needs to connect to Spacewire or Glitch Filter, configure the source of your GL[x] to use the Clock Recovery Circuitry. The GL[x] output can then be used.

**Oscillators** - The source is from the on-chip 50MHz oscillator. The RCOSC_50MHZ macro must be manually instantiated and connected to the CCC input pin, if selected as the reference clock source.

### Output Clock Frequency

You must specify the required output clock frequency. Those frequencies are used by the RTG4 FCCC with Enhanced PLL Calibration Configurator to compute the configuration of the CCC dividers and PLL to meet the requirements. The dividers and their names are highlighted in blue in the UI (Figure 1-6).

**Exact Value Option**

When you click the Exact Value checkbox to turn on this option, it forces the RTG4 FCCC with Enhanced PLL Calibration Configurator to generate the nearest actual frequency with a tolerance of 0.5 KHz. If this is not possible, it generates an error with the following error message:

*Exact Value option is used. No divider combination was found to satisfy the current settings. Consider adjusting or relaxing the configuration requirements.*

---

**Figure 1-5 • Clock Source Selection**

**Figure 1-6 • Output Frequency**
**Gated Clock Configuration**

For GL[x]/Y[x], Clock Gating is an inherent feature for RTG4 CCC. GL[x]_Y[x]_EN signal gates both the global network driven by the GL[x] and the fabric local routing resource driven by Y[x], where x can be 0, 1, 2, or 3 (Figure 1-7).

**Inversion Configuration**

The output can be inverted if required (Figure 1-8). The inversion affects GL[x] and Y[x] clock. Click the + sign to get the inverted output.

**PLL Configuration**

**PLL Reference Clock Source**

The following sources are available from the reference clock pull-down menu (Figure 1-9):

- **Dedicated Input Pad** - The clock source is one of the four regular FPGA I/Os that has a dedicated path to the CCC. The Configure as differential option allows you to configure any dedicated Input Pad as differential I/O. The package pin names for the selected CCC location are displayed next to the dedicated pads.

- **FPGA Fabric Input** - The clock source can be one of the four input signals coming from the FPGA Fabric.

- **Oscillators** - The source is from the on-chip 50MHz oscillator.
PLL Feedback Source

If you use the PLL, you can choose to use an internal or an external feedback loop, depending on your system level requirements (Figure 1-10 and Figure 1-11).

Internal Feedback Loop:

- **CCC Internal** - Default option
- **PLL Internal** - The triplicated PLL mode is not supported in this version of the RTG4 FCCC with Enhanced PLL Calibration, and thus PLL Internal Feedback mode is not available.
  
  You can continue to use this core with Single PLL Feedback mode (all other modes except PLL Internal) to prevent the issue described in Customer Notification CN19009.
  
  Alternatively, the Triplicated PLL is available in the RTG4 FCCC core, but will be subject to the issue described in CN19009. Also refer to the RTG4 PLL Radiation Test Report to decide which PLL mode is suitable for your application’s reliability requirements.

External Feedback Loop:

The external feedback is driven from the selected GL[x]/Y[x] fabric CCC output either through the fabric or externally to the chip.

- **Dedicated Input Pad** - The clock source is one of the four regular FPGA I/Os that has a dedicated path to the CCC.
- **FPGA Fabric Input** - The clock source can be one of the four input signals coming from the FPGA Fabric.

![Figure 1-10 • Internal Feedback Source](image-url)
PLL External Feedback Source

If you use the PLL with an external feedback source, all engine computations are based on the assumptions that the external feedback is driven from the selected GL[x]/Y[x] fabric CCC output whether through the fabric or externally to the chip (Figure 1-11).

![PLL External Feedback Source](image)

Programmable Delay Line

The programmable delay line enables you to delay (or advance) the PLL output clock with respect to the PLL reference clock by applying a delay to the reference clock path (or feedback path), as in Figure 1-12.

![Programmable Delay Line](image)

Input Clocks Configuration

You must enter the clock frequency of each CCC input used in the configuration as the PLL reference clock, PLL feedback clock or Output direct connection. Those frequencies are used to compute the PLL configuration and divider configuration that meet the output frequencies requirements.
Use Clock Recovery Circuitry to configure the CCC outputs to connect to Spacewire or Glitch Filter.

Figure 1-13 • Input Clocks Configuration

**Dedicated Input Pad** - Some of the dedicated inputs to the CCC can be configured to use a differential I/O technology. The location, I/O technology and attributes available for each CCC dedicated input pad is described in the RTG4 Datasheet.

**Clock Recovery Circuitry:**
Each CCC block has two dedicated Clock Recovery Circuitry Blocks: Block 0 and Block 1. The Clock Recovery Circuitry Blocks 0 and Block 1 can be used in either the SpaceWire mode (Default) or the Glitch Filter mode.

**Note:** For RT4G150-ES devices, the Glitch Filtering mode is not available and it is disabled.

The RX clock is based on Data and Strobe Inputs, which are from external dedicated I/Os. The Clock Recovery Circuitry Blocks also include a de-glitching circuit to prevent any undesirable narrow clock pulse at output.

1. You can select Dedicated input pad [1 and 3] for Data signal. Dedicated input pads[0 and 2] will be automatically set as corresponding Strobe signal.
2. The same pair of Dedicated input pads cannot be used simultaneously in Clock Recovery Circuitry.
3. Dedicated input pads which are used as Data and Strobe signals for Clock Recovery Circuitry block cannot be used as input to PLL Reference Clock and PLL Feedback Clock.
4. You cannot set input frequency values for Dedicated pads which are configured as Data and Strobe signals for RX Clock Recovery Circuitry.
5. Clock Recovery Circuitry Block 0 and 1 cannot have the same input source when both are configured for SpaceWire mode.
6. Clock Recovery Circuitry Block 0 and 1 cannot have the same input source when both are configured for Glitch Filter mode.
7. Clock Recovery Circuitry Block 0 and 1 cannot have the same input source when one is configured for SpaceWire mode and the other is configured for Glitch Filter mode.

8. It is valid to select the same input for PLL REFCLK (and CGL secondary clock) and Glitch Filter.
2 – PLL Options

The PLL Options enable you to configure advanced PLL options, such as output resynchronization and reset signals.

Click the PLL Options tab in the RTG4 FCCC with Enhanced PLL Calibration Configurator for the selected CCC (Figure 2-1).

![PLL Options (CCC_0 selected)](image)

**Figure 2-1 • PLL Options (CCC_0 selected)**

The PLL Options summarizes your PLL configuration (Figure 2-2).

![PLL Configuration Summary](image)

**Figure 2-2 • PLL Configuration Summary**
Lock Control

**Lock window** - Enables you to configure the maximum phase error allowed for the PLL to indicate it has locked. The lock window is expressed as part per million of the post divided reference clock period. Upon generation, the PLL lock window setting is validated against the maximum Phase and Frequency Detector (PFD) rate.

Refer to UG0586: RTG4 FPGA Clocking Resources User Guide for guidelines on selecting the appropriate PLL Lock Window. This is especially important for applications requiring phase alignment between the CCC input reference clock and the CCC outputs.

**Lock delay** - Enables you to set the number of Reference REFCLK clock cycles to wait before asserting the LOCK signal. While waiting, the PLL is in a locked state.

**Note:** Lock Delay is not supported in Simulation.

Output Resynchronization After Lock Configuration

RTG4 CCC contains four General Purpose Dividers (GPD). These dividers' source and division settings are automatically configured based on the frequency requirement you specified in the RTG4 FCCC with Enhanced PLL Calibration Configurator. GPDs can be used as the source of any outputs. For example, GPD0 can be used on a path to the GL1 output. It is recommended that you re-synchronize GPDs driven by the PLL output clock after the PLL locks to ensure that the first edge of each GPD is aligned with the PLL reference clock and with each other.

There are three different resynchronization options for GPDs/outputs:

- **Held output in reset (output low) after power-up. Released and resynchronized with the PLL reference clock after the PLL locked**
  - If enabled, GPD(s) (driven by the PLL) are held in reset low after power-up. Hence the output(s) (GLx/Yx) connected to those GPD(s) are held low (or high if inverted) after power-up.
  - After the PLL lock, the GPD(s) reset are released synchronously with the PLL reference clock.
  - The RTG4 FCCC with Enhanced PLL Calibration Configurator automatically inserts a GPD on each GL/Y output driven by the PLL even if the division factor is 1. This ensures the GL/Y driven by the PLL is held in reset at power-up.
  - Does not apply to the output(s)/GPD(s) on the PLL external feedback path (if any).
  - Does not apply for the output(s)/GPD(s) not driven by one of the PLL 8 phases output.

- **Outputs operate after power-up. Resynchronized with the PLL reference clock after the PLL locked (default selection)**
  - If enabled, GPD(s) (driven by the PLL) output are operational after power-up. Hence the output(s) (GLx/Yx) connected to those GPD(s) are operational after power-up.
  - After the PLL lock, the GPD(s) is synchronously reset with the PLL reference clock.
  - Does not apply to the output(s)/GPD(s) on the PLL external feedback path (if any).
  - Does not apply for the output(s)/GPD(s) not driven by one of the PLL 8 phases output.

- **Outputs operate after power-up. No automatic resynchronization**
  - If enabled, the corresponding GPD(s) output is operating after power-up. Hence the outputs (GLx/ Yx) connected to this GPD are operating after power-up.
  - There is no resynchronization after the PLL lock.
  - All GPD(s) directly connected to one of the nine input clocks (bypassing the PLL) are configured in this mode.

**Note:** For RT4G150-ES devices, this is the only supported option. If you select options other than this supported option and click **OK** and **Save**, an error message appears as follows:

*The selected option of Output Resynchronization after Lock is not supported for ES devices and the only supported option is Outputs Operate after power-up with No automatic resynchronization.*

**Note:** When the CCC is used without the PLL, such as when performing clock frequency division, the GPD(s) require a manual assertion and release of the GPDx_ARST_N input to synchronize the GPD output(s) to the input reference clock, after it has become stable. For example, the lock signal...
output of an upstream PLL could be used to release the GPDx_ARST_N input so that this CCC's divided output(s) are synchronized to the input clock.

**Miscellaneous Options**

**Enable Auto-Reset of PLL on Loss of Lock** - This option is enabled by default whenever the PLL is used.

Disabling this option will result in a Warning Exclamation Icon with a tool-tip message that states: *Warning: The insertion of PLL loss of lock auto-reset logic has been disabled. Auto-reset is helpful in the event the PLL lock is lost during operation. Please review Customer Notifications 19009 and 18009.7 on the Microsemi website to understand the consequences of disabling this option.*

**Expose PLL_BYPASS_N signal** - When selected, the input signal PLL_BYPASS_N is exposed to the FPGA Fabric. When this signal is asserted, the PLL core is turned off and the PLL outputs track the reference clock. This signal is active low.

**Expose GL[X]_Y[X]_EN and GL[X]_Y[X]_ARST_N signals** - When selected, the GL[X]_Y[X]_EN and GL[X]_Y[X]_ARST_N signals are exposed to the FPGA fabric. By default, these signals are not exposed.

**Clock Frequency Requirements**

You must specify the clock source frequency. Note the following frequency requirements:

- The On-chip 50MHZ Oscillator clock frequency is fixed at 50 MHz.
- PLL reference clock frequency must be between 10 MHz and 200 MHz.
- Output clock frequencies must be less than 400 MHz.
- Input used in bypass mode frequency must be less than 400 MHz.
## 3 – Port Description

### Table 3-1 • Fabric CCC Port Description

<table>
<thead>
<tr>
<th>Port Name</th>
<th>Direction</th>
<th>Polarity</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CCC_[0/1]_CLK0_PAD</td>
<td>Input</td>
<td>-</td>
<td>Input clock when using Dedicated Input Pad 0 configured as single ended I/O</td>
</tr>
<tr>
<td>CCC_[0/1]<em>CLK0</em>[PADP and PADN]</td>
<td>Input</td>
<td>-</td>
<td>Input clock when using Dedicated Input Pad 0 configured as differential I/O. P side and N side</td>
</tr>
<tr>
<td>CCC_[0/1]_CLK1_PAD</td>
<td>Input</td>
<td>-</td>
<td>Input clock when using Dedicated Input Pad 1 configured as single ended I/O</td>
</tr>
<tr>
<td>CCC_[0/1]<em>CLK1</em>[PADP and PADN]</td>
<td>Input</td>
<td>-</td>
<td>Input clock when using Dedicated Input Pad 1 configured as differential I/O. P side and N side</td>
</tr>
<tr>
<td>CCC_[0/1]_CLK2_PAD</td>
<td>Input</td>
<td>-</td>
<td>Input clock when using Dedicated Input Pad 2 configured as single ended I/O</td>
</tr>
<tr>
<td>CCC_[0/1]<em>CLK2</em>[PADP and PADN]</td>
<td>Input</td>
<td>-</td>
<td>Input clock when using Dedicated Input Pad 2 configured as differential I/O. P side and N side</td>
</tr>
<tr>
<td>CCC_[0/1]_CLK3_PAD</td>
<td>Input</td>
<td>-</td>
<td>Input clock when using Dedicated Input Pad 3 configured as single ended I/O</td>
</tr>
<tr>
<td>CCC_[0/1]<em>CLK3</em>[PADP and PADN]</td>
<td>Input</td>
<td>-</td>
<td>Input clock when using Dedicated Input Pad 3 configured as differential I/O. P side and N side</td>
</tr>
<tr>
<td>CCC_[0/1]<em>CLK0_SPWR_STROBE</em>[PADP and PADN]</td>
<td>Input</td>
<td>-</td>
<td>Input Clock when Dedicated pad 0 is used as input to Strobe of Clock Recovery Circuitry in differential mode. SpaceWire Mode only.</td>
</tr>
<tr>
<td>CCC_[0/1]<em>CLK1_SPWR_DATA</em>[PADP and PADN]</td>
<td>Input</td>
<td>-</td>
<td>Input Clock when Dedicated Pad 1 is used as input to Data of Clock Recovery Circuitry in differential mode. SpaceWire Mode only.</td>
</tr>
<tr>
<td>CCC_[0/1]<em>CLK2_SPWR_STROBE</em>[PADP and PADN]</td>
<td>Input</td>
<td>-</td>
<td>Input Clock when Dedicated pad 2 is used as input to Strobe of Clock Recovery Circuitry in differential mode. SpaceWire Mode only.</td>
</tr>
<tr>
<td>CCC_[0/1]<em>CLK3_SPWR_DATA</em>[PADP and PADN]</td>
<td>Input</td>
<td>-</td>
<td>Input Clock when Dedicated Pad 3 is used as input to Data of Clock Recovery Circuitry in differential mode. SpaceWire Mode only.</td>
</tr>
<tr>
<td>CCC_[0/1]_CLK0_SPWR_STROBE_PAD</td>
<td>Input</td>
<td>-</td>
<td>Input Clock when Dedicated pad 0 is used as input to Strobe of Clock Recovery Circuitry configured as single ended I/O. SpaceWire Mode only.</td>
</tr>
<tr>
<td>CCC_[0/1]_CLK1_SPWR_DATA_PAD</td>
<td>Input</td>
<td>-</td>
<td>Input Clock when Dedicated pad 1 is used as input to Data of Clock Recovery Circuitry configured as single ended I/O. SpaceWire Mode only.</td>
</tr>
<tr>
<td>CCC_[0/1]_CLK2_SPWR_STROBE_PAD</td>
<td>Input</td>
<td>-</td>
<td>Input Clock when Dedicated pad 2 is used as input to Strobe of Clock Recovery Circuitry configured as single ended I/O. SpaceWire Mode only.</td>
</tr>
</tbody>
</table>
### Table 3-1 • Fabric CCC Port Description (continued)

<table>
<thead>
<tr>
<th>Port Name</th>
<th>Direction</th>
<th>Polarity</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CCC[0/1]_CLK3_SPWR_DATA_PAD</td>
<td>Input</td>
<td>-</td>
<td>Input Clock when Dedicated pad 3 is used as input to Data of Clock Recovery Circuitry configured as single ended I/O. SpaceWire Mode only.</td>
</tr>
<tr>
<td>CCC[0/1]_CLK0</td>
<td>Input</td>
<td>-</td>
<td>Input clock from FPGA core when using FPGA Fabric Input 0</td>
</tr>
<tr>
<td>CCC[0/1]_CLK1</td>
<td>Input</td>
<td>-</td>
<td>Input clock from FPGA core when using FPGA Fabric Input 1</td>
</tr>
<tr>
<td>CCC[0/1]_CLK2</td>
<td>Input</td>
<td>-</td>
<td>Input clock from FPGA core when using FPGA Fabric Input 2</td>
</tr>
<tr>
<td>CCC[0/1]_CLK3</td>
<td>Input</td>
<td>-</td>
<td>Input clock from FPGA core when using FPGA Fabric Input 3</td>
</tr>
<tr>
<td>CCC[0/1]_RCOSC_50MHZ</td>
<td>Input</td>
<td>-</td>
<td>Input clock when using 50 MHz Oscillator</td>
</tr>
<tr>
<td>CCC[0/1]_GL0</td>
<td>Output</td>
<td>-</td>
<td>Generated clock driving FPGA fabric global network 0</td>
</tr>
<tr>
<td>CCC[0/1]_GL1</td>
<td>Output</td>
<td>-</td>
<td>Generated clock driving FPGA fabric global network 1</td>
</tr>
<tr>
<td>CCC[0/1]_GL2</td>
<td>Output</td>
<td>-</td>
<td>Generated clock driving FPGA fabric global network 2</td>
</tr>
<tr>
<td>CCC[0/1]_GL3</td>
<td>Output</td>
<td>-</td>
<td>Generated clock driving FPGA fabric global network 3</td>
</tr>
<tr>
<td>CCC[0/1]_GL0_Y0_EN</td>
<td>Input</td>
<td>High</td>
<td>Enable signal for the clock driving FPGA fabric global network 0 (GL0) and fabric local routing (Y0) network 0</td>
</tr>
<tr>
<td>CCC[0/1]_GL1_Y1_EN</td>
<td>Input</td>
<td>High</td>
<td>Enable signal for the clock driving FPGA fabric global network 1 (GL1) and fabric local routing (Y1) network 1</td>
</tr>
<tr>
<td>CCC[0/1]_GL2_Y2_EN</td>
<td>Input</td>
<td>High</td>
<td>Enable signal for the clock driving FPGA fabric global network 2 (GL2) and fabric local routing (Y2) network 2</td>
</tr>
<tr>
<td>CCC[0/1]_GL3_Y3_EN</td>
<td>Input</td>
<td>High</td>
<td>Enable signal for the clock driving FPGA fabric global network 3 (GL3) and fabric local routing (Y3) network 3</td>
</tr>
<tr>
<td>CCC[0/1]_GL0_Y0_ARST_N</td>
<td>Input</td>
<td>Low</td>
<td>(GL0/Y0) CGL reset signal. Asynchronous reset signal</td>
</tr>
<tr>
<td>CCC[0/1]_GL1_Y1_ARST_N</td>
<td>Input</td>
<td>Low</td>
<td>(GL1/Y1) CGL reset signal. Asynchronous reset signal</td>
</tr>
<tr>
<td>CCC[0/1]_GL2_Y2_ARST_N</td>
<td>Input</td>
<td>Low</td>
<td>(GL2/Y2) CGL reset signal. Asynchronous reset signal</td>
</tr>
<tr>
<td>CCC[0/1]_GL3_Y3_ARST_N</td>
<td>Input</td>
<td>Low</td>
<td>(GL3/Y3) CGL reset signal. Asynchronous reset signal</td>
</tr>
<tr>
<td>CCC[0/1]_Y0</td>
<td>output</td>
<td>-</td>
<td>Generated clock driving FPGA fabric local routing resource</td>
</tr>
<tr>
<td>CCC[0/1]_Y1</td>
<td>output</td>
<td>-</td>
<td>Generated clock driving FPGA fabric local routing resource</td>
</tr>
<tr>
<td>CCC[0/1]_Y2</td>
<td>output</td>
<td>-</td>
<td>Generated clock driving FPGA fabric local routing resource</td>
</tr>
<tr>
<td>CCC[0/1]_Y3</td>
<td>output</td>
<td>-</td>
<td>Generated clock driving FPGA fabric local routing resource</td>
</tr>
</tbody>
</table>
### Table 3-1 • Fabric CCC Port Description (continued)

<table>
<thead>
<tr>
<th>Port Name</th>
<th>Direction</th>
<th>Polarity</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CCC[0/1]_RX0_DATA_PORT</td>
<td>output</td>
<td>-</td>
<td>Output port for RX0 Data. Same signal that is driving the RX0 Spacewire clock recovery Data input</td>
</tr>
<tr>
<td>CCC[0/1]_RX1_DATA_PORT</td>
<td>output</td>
<td>-</td>
<td>Output port for RX1 Data. Same signal that is driving the RX1 Spacewire clock recovery Data input</td>
</tr>
<tr>
<td>CCC[0/1]_LOCK</td>
<td>output</td>
<td>High</td>
<td>PLL Lock indicator signal. This signal is asserted (lock) high.</td>
</tr>
<tr>
<td>CCC[0/1]_PLL_BYPASS_N</td>
<td>Input</td>
<td>Low</td>
<td>Powers-down the PLL core and bypasses it such that PLL_OUT tracks reference clock. This has higher priority than reset.</td>
</tr>
<tr>
<td>CCC[0/1]_PLL_POWERDOWN_N</td>
<td>Input</td>
<td>Low</td>
<td>Powers-down the PLL for the lowest quiescent current and the PLL outputs are Low. This has higher priority than reset and bypass</td>
</tr>
<tr>
<td>PLL_ARST_N</td>
<td>Input</td>
<td>Low</td>
<td>Powers-down the PLL core and asynchronously reset all its internal digital blocks such that the PLL outputs are driven low.</td>
</tr>
<tr>
<td>READY_VDDPLL</td>
<td>Input</td>
<td>High</td>
<td>Tie to high if you are certain that VDDPLL will not be the last supply to ramp up. Otherwise, connect to a circuit that delays the assertion of VDDPLL by 73ms as described in the RTG4 Clocking Resources User Guide.</td>
</tr>
<tr>
<td>CLK50_MHZ</td>
<td>Input</td>
<td>-</td>
<td>Input clock for soft logic that performs calibration at power-up or when the PLL is reset. The frequency of this clock must be 50 MHz max. You may connect to the GLx output of any CCC that is distributing the RCOSC_50MHZ signal. You cannot directly connect a RCOSC_50MHZ macro to this input port. Alternatively, an external free-running oscillator clock can be used as long as the frequency is 50MHz or less.</td>
</tr>
</tbody>
</table>

### Fabric CCC Configuration Bus Interface Signals – APB3 Bus Interface

<table>
<thead>
<tr>
<th>APB_S_PCLK</th>
<th>Input</th>
<th>-</th>
<th>APB3 interface clock signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>APB_S_PRESET_N</td>
<td>Input</td>
<td>Low</td>
<td>APB3 interface active low reset signal.</td>
</tr>
<tr>
<td>APB_S_PADDR[8:2]</td>
<td>Input</td>
<td>-</td>
<td>APB3 interface address bus. This port is used to address fabric CCC internal registers.</td>
</tr>
<tr>
<td>APB_S_PSEL</td>
<td>Input</td>
<td>-</td>
<td>APB3 interface slave select signal.</td>
</tr>
<tr>
<td>APB_S_PENABLE</td>
<td>Input</td>
<td>High</td>
<td>APB3 interface strobe signal to indicate the second cycle of an APB3 transfer.</td>
</tr>
<tr>
<td>APB_S_PWRITE</td>
<td>Input</td>
<td>-</td>
<td>APB3 interface read/write control signal. When High, this signal indicates an APB3 write access and when Low, a read access.</td>
</tr>
<tr>
<td>APB_S_PWDATA[7:0]</td>
<td>Input</td>
<td>-</td>
<td>APB3 interface write data bus.</td>
</tr>
<tr>
<td>APB_S_PRDATA[7:0]</td>
<td>Output</td>
<td>-</td>
<td>APB3 interface read data bus.</td>
</tr>
<tr>
<td><strong>APB_S_PREADY</strong></td>
<td>Output</td>
<td>-</td>
<td>APB3 interface ready indication output to master.</td>
</tr>
<tr>
<td>------------------</td>
<td>--------</td>
<td>---</td>
<td>---------------------------------</td>
</tr>
<tr>
<td><strong>APB_S_PSLVERR</strong></td>
<td>Output</td>
<td>-</td>
<td>APB3 interface error indication signal.</td>
</tr>
</tbody>
</table>
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