Two-Port Large SRAM Configuration User Guide

Introduction

The RTG4 Two-Port Large SRAM configurator helps to configure a Two-Port Large SRAM instance and define how the signals are connected.

A Two-Port Large SRAM allows write access on one port and read access on the other port (see the following figure). The core configurator cascades Large SRAM blocks automatically to create wide and deep memories by choosing the most efficient aspect ratio. It also handles the grounding of unused bits. The core configurator supports the generation of memories that have different Read and Write aspect ratios.

Two-Port Large SRAM is synchronous with read and write operations, setting up the addresses as well as writing and reading the data. The memory write and read operations are triggered at the rising edge of the clock. The address, data, write-enable, and read-enable inputs are registered.

An optional pipeline register is available at the read data port to improve the clock-to-out delay. When ECC is enabled, output flags are generated to indicate single-bit-correct and double-bit-detect.

For more information about Two-Port Large SRAM, refer to the RTG4 User Guide.

Figure 1. Two-Port Large SRAM Configurator

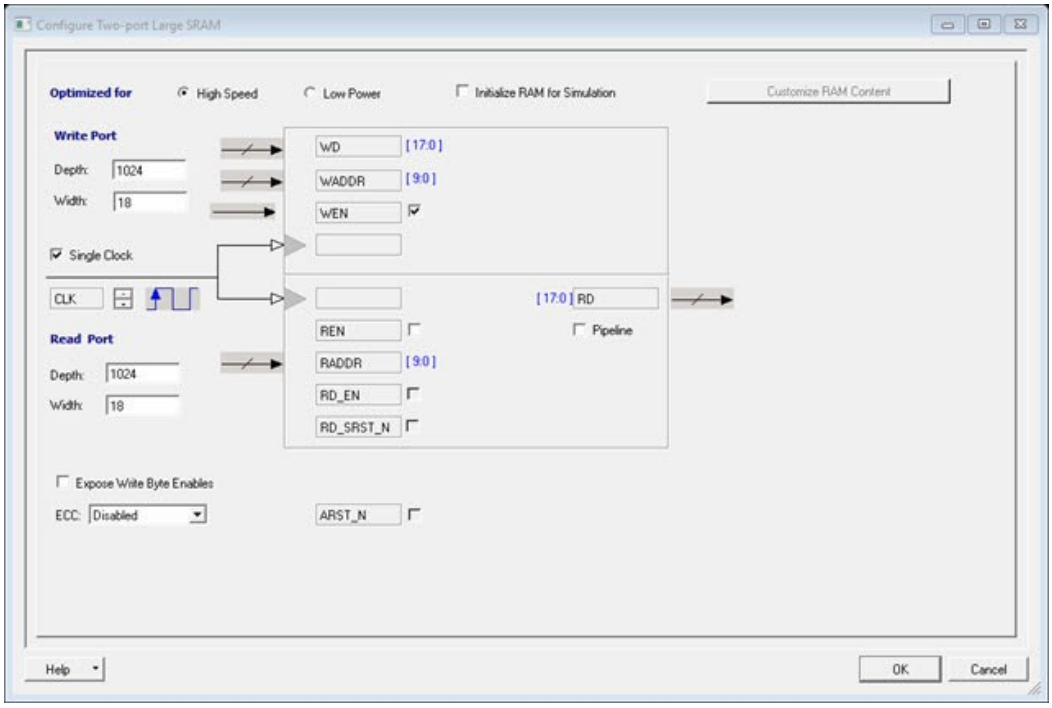


Table of Contents

Introduction....1

1. Using the RTG4 Two-Port Large SRAM....4
   - 1.1. Optimization for High Speed or Low Power....4
   - 1.2. Write Depth/Width and Read Depth/Width....4
   - 1.3. Single Clock (CLK) or Independent Write and Read Clocks (WCLK, RCLK)....4
   - 1.4. Write Enable (WEN)....4
   - 1.5. Read Enable (REN)....4
   - 1.6. Pipeline for Read Data Output....4
   - 1.7. Register Enable (RD_EN)....5
   - 1.8. Synchronous Reset (RD_SRST_N)....5
   - 1.9. Asynchronous Reset (ARST_N)....5
   - 1.10. Expose Write Byte Enables (WBYTE_EN)....5
   - 1.11. Error Correction Code (ECC)....5
   - 1.12. RD Register Truth Table....5

2. Internal Configurator Connections....6
   - 2.1. WEN Connections....6
   - 2.2. REN Connections....6
   - 2.3. WD Connections....7
   - 2.4. RD Logic....7
   - 2.5. SB_CORRECT and DB_DETECT Logic....7

3. Caveats for Two-Port Large SRAM Generation....8

4. RAM Content Manager....9
   - 4.1. Supported Formats....9
   - 4.2. Opening and Using RAM Content Manager....11
   - 4.3. MEMFILE (RAM Content Manager Output File)....12

5. Port Description....14

6. Parameters....15

7. Revision History....19

8. Microchip FPGA Technical Support....20
   - 8.1. Customer Service....20
   - 8.2. Customer Technical Support....20
   - 8.3. Website....20
   - 8.4. Outside the U.S....20

The Microchip Website....21

Product Change Notification Service....21

Customer Support....21

Microchip Devices Code Protection Feature....21

Legal Notice..... 22

Trademarks..... 22

Quality Management System..... 23

Worldwide Sales and Service.....24

1. Using the RTG4 Two-Port Large SRAM

This chapter describes the RTG4 Two-Port Large SRAM functions.

1.1 Optimization for High Speed or Low Power

Selecting High Speed results in a macro optimized for speed and area (width cascading).

Selecting Low Power results in a macro optimized for low power, but uses additional logic at the input and output (depth cascading). Performance for a low power optimized macro may be inferior to that of a macro optimized for speed.

1.2 Write Depth/Width and Read Depth/Width

The depth range for each port is 1-65536. The width range for each port is 1-7524.

The two ports can be independently configured for any depth and width. (Write Depth * Write Width) must equal (Read Depth * Read Width)

1.3 Single Clock (CLK) or Independent Write and Read Clocks (WCLK, RCLK)

The default configuration for Two-Port Large SRAM is a Single clock (CLK) to drive WCLK and RCLK with the same clock. Uncheck the Single clock check box to drive independent clocks (one each for Write and Read).

Click the up or down button next to the waveform of the clock signals to toggle the clock's active edge.

1.4 Write Enable (WEN)

Asserting WEN writes the data WD into the RAM at the address WADDR on the next rising edge of WCLK. Unchecking the WEN option ties the signal to the active state and removes it from the generated macro. Click the signal arrow (

) when available to toggle its polarity.

1.5 Read Enable (REN)

When there is no depth cascading, de-asserting REN holds the previous Read data (RD). When there is depth cascading, de-asserting REN generates zeros on RD. These different behaviors occur because the component's REN input is used to drive either the LSRAM block's A_REN input or the read-port block select input (A_BLK), depending on the cascading configuration.

Asserting REN reads the RAM at the read address RADDR onto the input of the RD register on the next rising edge of RCLK.

The default configuration for REN is unchecked, which ties the signal to the active state and removes it from the generated macro. Click the check box to insert that signal on the generated macro. Click the signal arrow (when available) to toggle its polarity.

1.6 Pipeline for Read Data Output

Click the Pipeline check box to enable pipelining for Read data (RD).

Turning off pipelining of Read data also disables the configuration options of the RD_EN, RD_SRST_N and ARST_N signals.

1.7 Register Enable (RD_EN)

The pipeline register for RD has an active high, enable input. The default configuration is to tie this signal to the active state and remove it from the generated macro. Click the signal's check box to insert that signal on the generated macro. Click the signal arrow (when available) to toggle its polarity.

1.8 Synchronous Reset (RD_SRST_N)

The pipeline register for RD has an active low, synchronous reset input. The default configuration is to tie this signal to the inactive state and remove it from the generated macro. Click the signal's check box to insert that signal on the generated macro. Click the signal arrow (when available) to toggle its polarity.

1.9 Asynchronous Reset (ARST_N)

The pipeline register for RD has an active low, asynchronous reset input. The default configuration is to tie this signal to the inactive state and remove it from the generated macro. Click the signal's check box to insert that signal on the generated macro. Click the signal arrow (when available) to toggle its polarity.

1.10 Expose Write Byte Enables (WBYTE_EN)

When enabled, write byte enables (WBYTE_EN) are available as a top-level bus. Each bit of WBYTE_EN enables writing to an individual byte of data. When ECC is enabled, the state of the WBYTE_EN bits should be identical for each LSRAM block.

1.11 Error Correction Code (ECC)

Three options are available for ECC:

- Disabled
- Pipelined
- Non-Pipelined

When ECC is disabled, each port can be configured to a width of 36 bits, 18 bits, or 9 bits. Alternatively, both ports can be configured to a 12-bit width.

When ECC is enabled (Pipelined or Non-Pipelined), both ports have word widths equal to 36 bits or 18 bits.

1.12 RD Register Truth Table

The following table describes the functionality of the control signals on the RD register.

Table 1-1. RD Register Truth Table

ARST_N	RCLK	RD_EN	RD_SRST_N	D	Q_{n+1}
0	X	X	X	X	0
1	Not rising	X	X	X	Q_n
1	↑	0	X	X	Q_n
1	↑	1	0	X	0
1	↑	1	1	D	D

2. Internal Configurator Connections

This chapter describes an example where a Two-Port LSRAM configuration generates a component with the following address widths.

- WADDR[*WA_MSB:0*]
- RADDR[*RA_MSB:0]*

In this example, assume the following:

- *M* is the width of the address on the write-port of each LSRAM block.
- *N* is the width of the address on the read-port of each LSRAM block.
- The decoder logic function is *decode*(addr*[j:k], i*), where 0 <= *i* < $2^{(j-k+1)}$.
- *D* is the depth of an LSRAM block in the array of blocks, starting at 0.

LSRAM Block Port Depth x Width	*M, N*
2Kx9	11
1Kx18	10

2.1 WEN Connections

The **WEN** signal on the generated component is connected to the write port block select input (**B_BLK**) for each LSRAM block according to the block depth within the component and synchronized with **WCLK**.

Table 2-1. WEN Connections

Depth	B_BLK[2]	B_BLK[1]	B_BLK[0]
WA_MSB < *N*	**WEN**	1	0
WA_MSB = *N*	**WEN**	1	*decode*(**WADDR**[*M*:*M*],*D*%2)
WA_MSB = *M*+1	**WEN**	*decode* (**WADDR**[*M*+1:*M*+1], (*D*/2)%2)	*decode* (**WADDR**[*M*:*M*],*D*%2)
WA_MSB > *M*+1	**WEN** & *decode* (**WADDR**[WA_*MSB*:*M*+2], *D*/4)	*decode* (**WADDR**[*M*+1:*M*+1], (*D*/2)%2)	*decode* (**WADDR**[*M*:*M*], *D*%2)

2.2 REN Connections

The **REN** signal on the generated component is connected to the write port block select input (**A_BLK**) for each LSRAM block according to the block depth within the component and synchronized with **RCLK**.

Table 2-2. REN Connections

Depth	A_BLK[2]	A_BLK[1]	A_BLK[0]	A_REN	Read-Data when REN=0
RA_MSB < *N*	1	1	1	**REN**	Hold
RA_MSB = *N*	**REN**	1	*decode*(**RADDR**[*N:N*], *D* %2)	1	0

.....continued					
Depth	**A_BLK[2]**	**A_BLK[1]**	**A_BLK[0]**	**A_REN**	**Read-Data when REN=0**
RA_MSB = *N*+1	**REN**	*decode*(**RADDR**[*N*+1:*N*+1], (*D*/ 2)%2)	*decode* (**RADDR**[*N:N*], *D* %2)	1	0
RA_MSB > *N*+1	**REN** & *decode*(**RADDR**[*RA_MSB*:*N*+2], *D*/4)	*decode*(**RADDR**[*N*+1:*N*+1], (*D*/ 2)%2)	*decode* (**RADDR**[*N:N*], *D* %2)	1	0

Notes: Observe the different behaviors when **REN** is de-asserted on the top-level generated component:

- If there is no depth cascading (*RA_MSB* < *N*), de-asserting **REN** holds the previously read-data.
- If there is depth cascading (*RA_MSB* >= *N*), de-asserting **REN** generates zeros on the read-data.

The different behavior in these two scenarios occurs because the component's **REN** input is used to drive either the LSRAM block's **A_REN** input or the read-port block select input (**A_BLK**), depending on the cascading configuration.

2.3 WD Connections

The **WD** bits on the generated component are partitioned into slices based on the width of the data on the write port of each LSRAM block. Each bit of **WD** is connected to all blocks in a slice at every depth and synchronized with **WCLK**.

2.4 RD Logic

The **RD** bits on the generated component are partitioned into slices based on the width of the data on the read port of each LSRAM block. Each bit of read-data from all blocks in a slice at every depth is OR'd together to generate a bit of **RD**. The **RD** bits are synchronized with **RCLK** according to the latency in the following table.

Table 2-3. RD Logic Latencies

ECC Pipeline	ECC	RD Pipeline	RD Latency
No	No	No	0
No	No	Yes	1
No	Yes	No	0
No	Yes	Yes	1
Yes	Yes	No	1
Yes	Yes	Yes	2

2.5 SB_CORRECT and DB_DETECT Logic

The **SB_CORRECT** and **DB_DETECT** outputs are synchronized with **RCLK** according to the above **RD** latency.

The **SB_CORRECT** flags of each LSRAM block are gated by the block's **A_BLK** signals that are pipelined one more than the **RD** latency value, and then OR'd together to generate the **SB_CORRECT** output of the component.

Similarly, the **DB_DETECT** flags of each LSRAM block are gated by the block's **A_BLK** signals that are pipelined one more than the **RD** latency value, and then OR'd together to generate the **DB_DETECT** output of the component. As a result, both the outputs are zero whenever **REN** is de-asserted.

3. Caveats for Two-Port Large SRAM Generation

- The core configurator supports depth cascading of up to 32 blocks only.
- The software returns a configuration error for unsupported configurations.
- All unused inputs must be grounded. ARST_N resets only the pipeline register for RD; it does not reset the memory contents.
- Writing to and reading from the same address is undefined and should be avoided.
- Although there is no collision prevention or detection, correct data is expected to be written into the memory.

4. RAM Content Manager

The RAM Content Manager allows you to specify the contents of your memory in a way that avoids the simulation cycles required for initializing the memory, thereby reducing simulation runtime.

The RAM core generator removes much of the complexity required to generate large memory that uses one or more RAM blocks on the device. It does so by using one or more memory blocks to generate a RAM matching your configuration, while creating the surrounding cascading logic.

The configurator cascades RAM blocks three ways:

- Cascaded deep (e.g., 2 blocks of 1024x18 to create a 2048x18)
- Cascaded wide (e.g., 2 blocks of 1024x18 to create a 1024x36)
- Cascaded wide and deep (e.g., 4 blocks of 1024x18 to create a 2048x36, in a 2 blocks width-wise by 2 blocks depth-wise configuration)

Using the configurator, you specify memory content in terms of your total memory size. The configurator partitions your memory file so that content is directed to the appropriate block RAM when multiple blocks are cascaded.

4.1 Supported Formats

The Microchip implementation of these formats interprets data sets in bytes. This means that if the memory width is 7 bits, every 8th bit in the data set is ignored. Alternatively, if the data width is 9, 2 bytes are assigned to each memory address and the upper 7 bits of each 2-byte pair are ignored.

The following examples show how the data is interpreted for various word sizes. These examples assume that for the following given data `FF 11 EE 22 DD 33 CC 44 BB 55`, `55` is the MSB and `FF` is the LSB.

32-bit Word Size

```
0x22EE11FF (address 0)
0x44CC33DD (address 1)
0x000055BB (address 2)
```

16-bit Word Size

```
0x11FF (address 0)
0x22EE (address 1)
0x33DD (address 2)
0x44CC (address 3)
0x55BB (address 4)
```

8-bit Word Size

```
0xFF (address 0)
0x11 (address 1)
0xEE (address 2)
0x22 (address 3)
0xDD (address 4)
0x33 (address 5)
0xCC (address 6)
0x44 (address 7)
0xBB (address 8)
```

```
0x55 (address 9)
```

9-bit Word Size

```
0x11FF -> 0x01FF (address 0)
0x22EE -> 0x00EE (address 1)
0x33DD -> 0x01DD (address 2)
0x44CC -> 0x00CC (address 3)
0x55BB -> 0x01BB (address 4)
```

Note: For the 9-bit word size, the upper 7 bits of the 2 bytes are ignored.

4.1.1 Intel-HEX

Intel-HEX is a standard format created by Intel. Files end with a HEX or IHX extension (for example, `file2.hex` or `file3.ihx`).

Memory contents are stored in ASCII files using hexadecimal characters. Each file contains a series of records (lines of text) delimited by new line, '\n', characters and each record starts with a ':' character. For more information about this format, see the Intel-Hex Record Format Specification document on the web (search Intel Hexadecimal Object File for several examples).

The Intel Hex record is composed of five fields arranged as follows:

```
:llaaaatt[dd...]cc
```

where:

- : is the start code of every Intel Hex record.
- ll is the byte count of the data field.
- aaaa is the 16-bit address of the beginning of the memory position for the data. Address is big Endian.
- tt is the record type that defines the data field:
  - 00 data record
  - 01 end of file record
  - 02 extended segment address record
  - 03 start segment address record (ignored by Microchip SoC tools)
  - 04 extended linear address record
  - 05 start linear address record (ignored by Microchip SoC tools)
- [dd...] is a sequence of n bytes of the data (n is equivalent to what was specified in the ll field).
- cc is a checksum of count, address, and data. The following is an example of an Intel Hex record: `:0300300002337A1E`

4.1.2 Motorola S-Record

Motorola S-Records use the file extension S (for example, `file4.s`).

Like Intel-HEX, Motorola S-records use ASCII files, hex characters, and records to specify memory content. For more information about this format, search the web for several examples of the Motorola S-record description document. The RAM Content Manager uses only the S1 through S3 record types and ignores other record types.

The key difference between Intel-HEX and Motorola S-record types is the record format, along with the extra error-checking features incorporated into Motorola S.

In both formats, memory content is specified by providing a starting address and a data set. The upper bits of the data set are loaded into the starting address and leftovers overflow into the adjacent addresses until the entire data set has been used.

The Motorola S-record is composed of six fields and arranged as follows:

```
Stllaaaa[dd...]cc
```

where:

- S is the start code of every Motorola S-record.
- t is the record type that defines the data field.
- ll is the byte count of the data field.
- aaaa is a 16-bit address of the beginning of the memory position for the data. Address is big Endian.
- [dd...] is a sequence of n bytes of the data; n is equivalent to what was specified in the ll field.
- cc is the checksum of count, address, and data. The following is an example of a Motorola S-record:
  `S10a0000112233445566778899FFFA`

4.2 Opening and Using RAM Content Manager

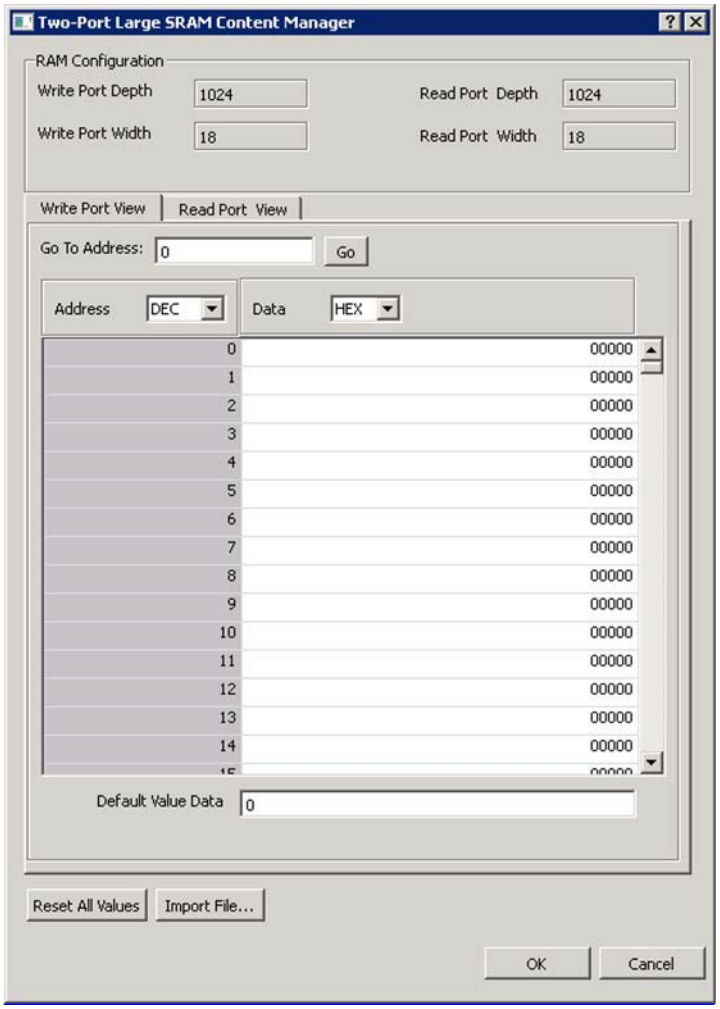
The following sections describe how to open and use the RAM Content Manager.

4.2.1 Opening RAM Content Manager

To open RAM Content Manager:

1. Specify your RAM configuration by setting your Read and Write Depth and Width.
2. Select the **Initialize RAM for Simulation** check box.
3. Click **Customize RAM Content**.
   The RAM Content Manager appears, as shown in the following figure.

Figure 4-1. Customize RAM Content for Simulation



4.2.2 RAM Configuration

RAM Configuration	Description
Write Port Depth	As specified in the RAM core generator dialog box (not editable).
Write Port Width	As specified in the RAM core generator dialog box (not editable).
Read Port Depth	As specified in the RAM core generator dialog box (not editable).
Read Port Width	As specified in the RAM core generator dialog box (not editable).

4.2.3 Write Port View and Read Port View

Write Port and Read Port Views	Description
Go To Address	Allows you to go to a specific address in the manager. Each memory block has many addresses; it is often difficult to scroll through and find a specific one. This task is simplified by allowing you to type a specific address. The number display format (Hex, Bin, Dec) is controlled by the value you set in the drop-down menu above the Address column.
Address	The Address column lists the address of a memory location. The drop-down menu specifies the number format for your address list (hexadecimal, binary, or decimal).
Data	Allows you to control the data format and data value in the manager. Click the value to change it. **Note:** Dialogs show all data with the MSB down to the LSB. For example, if the row shows 0xAABB for a 16-bit word size, the MSB would be AA and the LSP would be BB.
Default Data Value	The value given to memory addresses that have not been explicitly initialized by importing content or editing manually. When changed, all default values in the manager are updated to match the new value. The number display format (Hex, Bin, Dec) is controlled by the value you set in the drop-down menu above the Data column.
Reset All Values	Resets the Data values.
Import from File	Opens the Import Memory Content dialog box; enables you to select a memory content file (Intel-Hex) to load. Intel-Hex file extensions are set to *.hex during import.
OK	Closes the manager and saves all the changes made to the memory and its contents.
Cancel	Closes the manager, cancels all your changes in this instance of the manager, and returns the memory to the state it held before the manager was opened.

4.3 MEMFILE (RAM Content Manager Output File)

To transfer RAM data from the RAM Content Manager to test equipment, use MEM files. RAM contents are first organized into the logical layer, and then reorganized to fit the hardware layer. Then the contents are stored in MEM files that are read by other systems and used for testing.

The MEM files are named according to the logical structure of RAM elements created by the configurator. Using this method, the highest order RAM blocks are named `CORE_R0C0.mem`, where “R” stands for row and “C” stands for column. For multiple RAM blocks, the naming continues with CORE_R0C1, CORE_R0C2, CORE_R1C0, and so on.

Data intended for RAM is stored as ASCII 1s and 0s within the file. Each memory address occupies one line. Words from logical layer blocks are concatenated or split to make them fit efficiently within the hardware blocks. If the logical

layer width is less than the hardware layer, two or more logical layer words are concatenated to form one hardware layer word. In this case, the lowest bits of the hardware word comprise the lower address data bits from the logical layer. If the logical layer width exceeds the hardware layer, the words are split, with the lower bits placed in lower addresses.

If the logical layer words do not fit cleanly into the hardware layer words, the most significant bit of the hardware layer words is not used and defaults to zero. This is also done when the logical layer width is 1 to avoid left over memory at the end of the hardware block.

5. Port Description

The following table lists the Two-Port Large SRAM signals in the generated macro.

Table 5-1. Two-Port Large SRAM Signals

Port	Direction	Default Polarity	Description
CLK	In	Rising Edge	Single clock to drive both WCLK and RCLK.
WD[]	In		Write data.
WADDR[]	In		Write address.
WEN	In	Active high	Write port enable.
WCLK	In	Rising edge	Write clock.
RCLK	In	Rising edge	Read clock.
REN	In	Active high	Read data enable.
RADDR[]	In		Read address.
RD[]	Out		Read data.
RD_EN	In	Active high	Read data register enable.
RD_SRST_N	In	Active low	Read data register Synchronous reset.
ARST_N	In	Active low	Read data register Asynchronous reset.
SB_CORRECT	Out	Active High	Single-bit correct flag.
DB_DETECT	Out	Active High	Double-bit detect flag.
WBYTE_EN[]	In	Active High	Write Byte Enables (per byte).

6. Parameters

The following table lists the Two-Port Large SRAM parameters in the generated macro.

Table 6-1. Two-Port Large SRAM Parameters

Parameter	Valid Range	Default (Condition)	Description
LPMTYPE	LPM_RAM	LPM_RAM	Macro category.
PTYPE	1, 2	1	1: Two-port. 2: Dual-port.
INIT_RAM	F, T	F	F: No RAM initialization for simulation. T: Initialize RAM for simulation.
IMPORT_FILE	—	IMPORT_FILE Dummy parameter (INIT_RAM=T)	Memory file to be imported to initialize RAM. No Tcl support yet
CASCADE	0, 1	0	0: Cascading for WIDTH or Speed. 1: Cascading for DEPTH or Power.
CLKS	1, 2	1	1: Single Read/Write clock. 2: Independent Read and Write clocks.
CLOCK_PN	CLK CLK_N	CLK (CLKS=1)	Single clock Port name.
CLK_EDGE	RISE, FALL	RISE (CLKS=1)	RISE: Rising edge Single clock. FALL: Falling edge Single clock.
WCLOCK_PN	WCLK WCLK_N	WCLK (CLKS=2)	Write clock Port name
RCLOCK_PN	RCLK RCLK_N	RCLK (CLKS=2)	Read clock Port name.
WCLK_EDGE	RISE, FALL	RISE (CLKS=2)	RISE: Rising edge Write clock. FALL: Falling edge Write clock.

.....continued

Parameter	Valid Range	Default (Condition)	Description
RCLK_EDGE	RISE, FALL	RISE (CLKS=2)	RISE: Rising edge Read clock. FALL: Falling edge Read clock.
WWIDTH	1-7524	18	Write data width.
WDEPTH	1-65536	1024	Write address depth.
RWIDTH	1-7524	18	Read data output width.
RDEPTH	1- 65536	1024	Read address depth.
WE_POLARITY	0, 1, 2	1	0: Active-low W_EN_N port will be exposed to exercise Write port enable. 1: Active-high W_EN port will be exposed to exercise Write port enable. 2: Write port enable tied off to be always active.
WE_PN	WEN WEN_N	WEN	Write port enable Port name.
RE_POLARITY	0, 1, 2	2	0: Active-low R_EN_N port will be exposed to exercise Read port enable. 1: Active-high R_EN port will be exposed to exercise Read port enable. 2: Read port enable tied off to be always active.
RE_PN	REN REN_N	REN	Read port enable Port name.
RPMODE	0, 1	0	0: Bypass Read data register. 1: Pipeline Read data.
DATA_OUT_PN	—	RD	Read data Port name.

.....continued

Parameter	Valid Range	Default (Condition)	Description
A_DOUT_EN_POLARITY	0, 1, 2	2 (RPMODE =1)	0: Active-low A_DOUT_EN_N port will be exposed to exercise Port A read data register enable. 1: Active-high A_DOUT_EN port will be exposed to exercise Port A read data register enable. 2: Port A read data register enable tied off to bealways active.
A_DOUT_EN_PN	RD_EN RD_EN_N	RD_EN (RPMODE =1)	Read data register enable Port name.
A_DOUT_SRST_POLARITY	0, 1, 2	2 (RPMODE =1)	0: Active-low A_DOUT_SRST_N port will be exposed to exercise Port A read data register Sync-reset 1: Active-high A_DOUT_SRST port will be exposed to exercise Port A read data register Sync-reset 2: Port A read data register Sync- reset tied off to be always inactive.
A_DOUT_SRST_PN	RD_SRST RD_SRST_N	RD_SRST_N (RPMODE =1)	Read data register Sync-reset Port name.
ARST_N_POLARITY	0, 1, 2	2 (RPMODE =1)	Asynchronous Reset Polarity 0: Active-low ARST_N port will be exposed to exercise Read data register Async reset 1: Active-high ARST port will be exposed to exercise Read data register Async reset 2: Read data register Async-reset tied off to be always inactive
RESET_PN	ARST_N ARST	ARST_N (RPMODE =1)	Read data register Async-reset Port name.

.....continued

Parameter	Valid Range	Default (Condition)	Description
ECC	0, 1, 2	0	0: ECC disabled. 1: ECC Pipelined. 2: ECC Non-pipelined.
DATA_IN_PN	—	WD	Write data Port name.
WADDRESS_PN	—	WADDR	Write address Port name.
RADDRESS_PN	—	RADDR	Read address Port name.
BYTEENABLES	0, 1	0	0: Do not generate WBYTE_EN. 1: Generate WBYTE_EN.
A_WBYTE_EN_PN	—	WBYTE_EN	Write Byte enable port name
BYTE_ENABLE_WIDTH	—	0	Write port Byte Enable width Values are based on the configuration

7. Revision History

Revision	Date	Description
A	11/2020	Initial Revision

8. Microchip FPGA Technical Support

Microchip FPGA Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, and worldwide sales offices. This section provides information about contacting Microchip FPGA Products Group and using these support services.

8.1 Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

- From North America, call **800.262.1060**
- From the rest of the world, call **650.318.4460**
- Fax, from anywhere in the world, **650.318.8044**

8.2 Customer Technical Support

Microchip FPGA Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microchip FPGA Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

You can communicate your technical questions through our Web portal and receive answers back by email, fax, or phone. Also, if you have design problems, you can upload your design files to receive assistance. We constantly monitor the cases created from the web portal throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

Technical support can be reached at soc.microsemi.com/Portal/Default.aspx.

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), log in at soc.microsemi.com/Portal/Default.aspx, go to the **My Cases** tab, and select **Yes** in the ITAR drop-down list when creating a new case. For a complete list of ITAR-regulated Microchip FPGAs, visit the ITAR web page.

You can track technical cases online by going to My Cases.

8.3 Website

You can browse a variety of technical and non-technical information on the Microchip FPGA Products Group home page, at www.microsemi.com/soc.

8.4 Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support at (https://soc.microsemi.com/Portal/Default.aspx) or contact a local sales office.

Visit About Us for sales office listings and corporate contacts.

The Microchip Website

Microchip provides online support via our website at www.microchip.com/. This website is used to make files and information easily available to customers. Some of the content available includes:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip design partner program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

Product Change Notification Service

Microchip's product change notification service helps keep customers current on Microchip products. Subscribers will receive email notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, go to www.microchip.com/pcn and follow the registration instructions.

Customer Support

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Embedded Solutions Engineer (ESE)
- Technical Support

Customers should contact their distributor, representative or ESE for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in this document.

Technical support is available through the website at: www.microchip.com/support

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods being used in attempts to breach the code protection features of the Microchip devices. We believe that these methods require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Attempts to breach these code protection features, most likely, cannot be accomplished without violating Microchip's intellectual property rights.
- Microchip is willing to work with any customer who is concerned about the integrity of its code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is "unbreakable." Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Legal Notice

Trademarks

ISBN: 978-1-5224-7140-0

Quality Management System

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.

Worldwide Sales and Service

AMERICAS	ASIA/PACIFIC	ASIA/PACIFIC	EUROPE
Corporate Office 2355 West Chandler Blvd. Chandler, AZ 85224-6199 Tel: 480-792-7200 Fax: 480-792-7277 Technical Support: www.microchip.com/support Web Address: www.microchip.com **Atlanta** Duluth, GA Tel: 678-957-9614 Fax: 678-957-1455 **Austin, TX** Tel: 512-257-3370 **Boston** Westborough, MA Tel: 774-760-0087 Fax: 774-760-0088 **Chicago** Itasca, IL Tel: 630-285-0071 Fax: 630-285-0075 **Dallas** Addison, TX Tel: 972-818-7423 Fax: 972-818-2924 **Detroit** Novi, MI Tel: 248-848-4000 **Houston, TX** Tel: 281-894-5983 **Indianapolis** Noblesville, IN Tel: 317-773-8323 Fax: 317-773-5453 Tel: 317-536-2380 **Los Angeles** Mission Viejo, CA Tel: 949-462-9523 Fax: 949-462-9608 Tel: 951-273-7800 **Raleigh, NC** Tel: 919-844-7510 **New York, NY** Tel: 631-435-6000 **San Jose, CA** Tel: 408-735-9110 Tel: 408-436-4270 **Canada - Toronto** Tel: 905-695-1980 Fax: 905-695-2078	**Australia - Sydney** Tel: 61-2-9868-6733 **China - Beijing** Tel: 86-10-8569-7000 **China - Chengdu** Tel: 86-28-8665-5511 **China - Chongqing** Tel: 86-23-8980-9588 **China - Dongguan** Tel: 86-769-8702-9880 **China - Guangzhou** Tel: 86-20-8755-8029 **China - Hangzhou** Tel: 86-571-8792-8115 **China - Hong Kong SAR** Tel: 852-2943-5100 **China - Nanjing** Tel: 86-25-8473-2460 **China - Qingdao** Tel: 86-532-8502-7355 **China - Shanghai** Tel: 86-21-3326-8000 **China - Shenyang** Tel: 86-24-2334-2829 **China - Shenzhen** Tel: 86-755-8864-2200 **China - Suzhou** Tel: 86-186-6233-1526 **China - Wuhan** Tel: 86-27-5980-5300 **China - Xian** Tel: 86-29-8833-7252 **China - Xiamen** Tel: 86-592-2388138 **China - Zhuhai** Tel: 86-756-3210040	**India - Bangalore** Tel: 91-80-3090-4444 **India - New Delhi** Tel: 91-11-4160-8631 **India - Pune** Tel: 91-20-4121-0141 **Japan - Osaka** Tel: 81-6-6152-7160 **Japan - Tokyo** Tel: 81-3-6880- 3770 **Korea - Daegu** Tel: 82-53-744-4301 **Korea - Seoul** Tel: 82-2-554-7200 **Malaysia - Kuala Lumpur** Tel: 60-3-7651-7906 **Malaysia - Penang** Tel: 60-4-227-8870 **Philippines - Manila** Tel: 63-2-634-9065 **Singapore** Tel: 65-6334-8870 **Taiwan - Hsin Chu** Tel: 886-3-577-8366 **Taiwan - Kaohsiung** Tel: 886-7-213-7830 **Taiwan - Taipei** Tel: 886-2-2508-8600 **Thailand - Bangkok** Tel: 66-2-694-1351 **Vietnam - Ho Chi Minh** Tel: 84-28-5448-2100	**Austria - Wels** Tel: 43-7242-2244-39 Fax: 43-7242-2244-393 **Denmark - Copenhagen** Tel: 45-4485-5910 Fax: 45-4485-2829 **Finland - Espoo** Tel: 358-9-4520-820 **France - Paris** Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79 **Germany - Garching** Tel: 49-8931-9700 **Germany - Haan** Tel: 49-2129-3766400 **Germany - Heilbronn** Tel: 49-7131-72400 **Germany - Karlsruhe** Tel: 49-721-625370 **Germany - Munich** Tel: 49-89-627-144-0 Fax: 49-89-627-144-44 **Germany - Rosenheim** Tel: 49-8031-354-560 **Israel - Ra'anana** Tel: 972-9-744-7705 **Italy - Milan** Tel: 39-0331-742611 Fax: 39-0331-466781 **Italy - Padova** Tel: 39-049-7625286 **Netherlands - Drunen** Tel: 31-416-690399 Fax: 31-416-690340 **Norway - Trondheim** Tel: 47-72884388 **Poland - Warsaw** Tel: 48-22-3325737 **Romania - Bucharest** Tel: 40-21-407-87-50 **Spain - Madrid** Tel: 34-91-708-08-90 Fax: 34-91-708-08-91 **Sweden - Gothenberg** Tel: 46-31-704-60-40 **Sweden - Stockholm** Tel: 46-8-5090-4654 **UK - Wokingham** Tel: 44-118-921-5800 Fax: 44-118-921-5820