SmartFusion2

Micro SRAM Configuration

Microsemi

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Introduction

A Micro SRAM block is 16 times smaller than a Two-Port Large SRAM block, but it has three ports. Ports A and B allow read access and Port C allows write access (Figure 1).

The core configurator automatically cascades Micro SRAM blocks to create wider and deeper memories by choosing the most efficient aspect ratio. It also handles the grounding of unused bits. The core configurator supports the generation of memories that have different aspect ratios on each port.

Write operations to Port C are synchronous for setting up the address as well as writing the data. The memory write operations will be triggered at the rising edge of the clock.

Read operations from Ports A and B can be either asynchronous or synchronous (for setting up the address as well as reading the data). An optional pipeline register is available at the address of ports A and B to improve the setup. An optional pipeline register is available at the read data of ports A and B to improve the clock-to-out delay. Disabling both the address and read data registers creates the asynchronous mode for read operations. For synchronous read operations, the memory read operations will be triggered at the rising edge of the clock.

In this document we describe how you can configure a Micro SRAM instance and define how the signals are connected. For more details about the Micro SRAM, please refer to the SmartFusion2 User Guide.

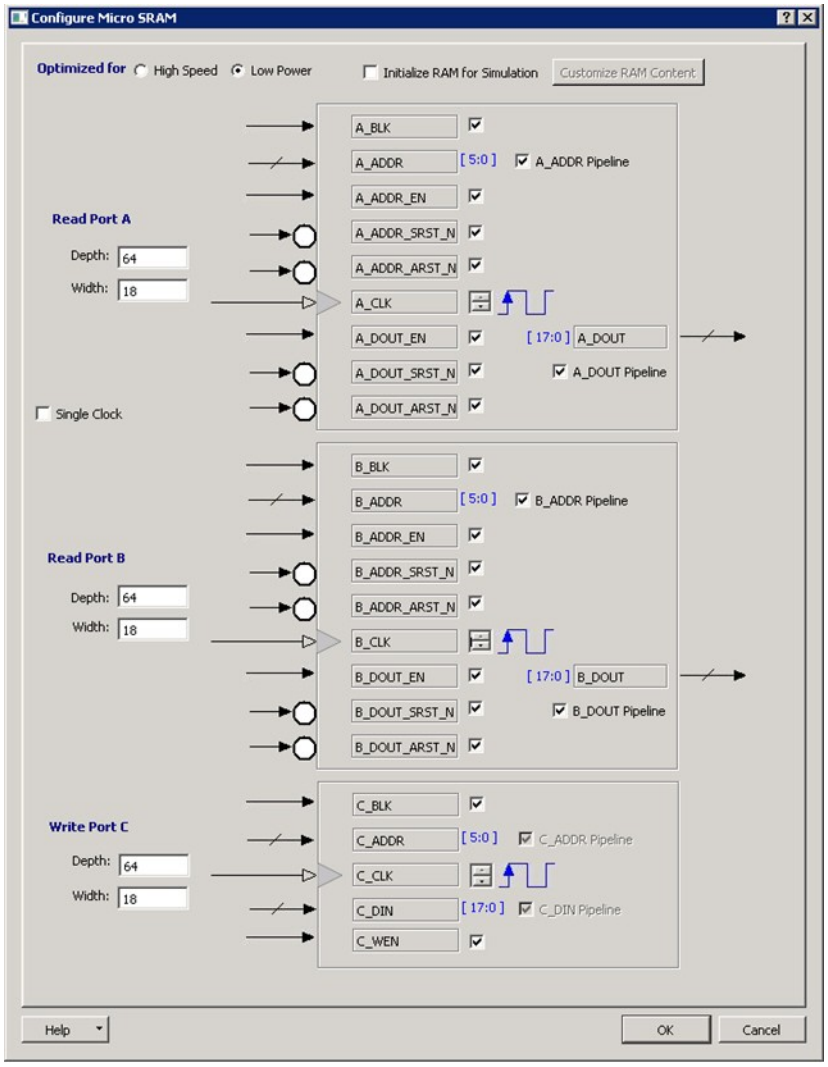

Figure 1 • **Micro SRAM Configurator**

1 – Functionality

Optimization for High Speed or Low Power

Selecting High Speed results in a macro optimized for speed and area (width cascading).

Selecting Low Power results in a macro optimized for low power, but uses additional logic at the input and output (depth cascading). Performance for a low power optimized macro may be inferior to that of a macro optimized for speed.

Depth/Width for Ports A, B and C

The depth range for each port is 1-32768. The width range for each port is 1-1296.

The three ports can be independently configured for any depth and width. (Port A Depth * Port A Width) must equal (Port B Depth * Port B Width) must equal (Port C Depth * Port C Width).

Single Clock (CLK) or Independent Write and Read Clocks (A_CLK, B_CLK, C_CLK)

The default configuration for Micro SRAM is a Single clock (CLK) to drive all three ports with the same clock. Uncheck the Single clock checkbox to drive independent clocks - one for each port (A_CLK, B_CLK and C_CLK).

Click the waveform control next to any of the clock signals to toggle its active edge.

Block Select for Ports A and B (A_BLK, B_BLK)

De-asserting A_BLK forces A_DOUT to zero.

De-asserting B_BLK forces B_DOUT to zero.

Asserting A_BLK reads the RAM at the address given by the output of the A_ADDR register onto the input of the A_DOUT register.

Asserting B_BLK reads the RAM at the address given by the output of the B_ADDR register onto the input of the B_DOUT register.

The default configuration for A_BLK and B_BLK is unchecked, which ties the signal to the active state and removes it from the generated macro. Click the respective checkbox to insert that signal on the generated macro. Click the signal arrow (when available) to toggle its polarity.

Block Select for Port C (C_BLK) and Write Enable (C_WEN)

Asserting C_BLK when C_WEN is high will write the data C_DIN into the RAM at the address C_ADDR on the next rising edge of C_CLK.

Un-checking the C_BLK option ties the signal to the active state and removes it from the generated macro. Click the signal arrow (when available) to toggle its polarity.

The default configuration for C_WEN is unchecked, which ties the signal to the active state and removes it from the generated macro. Click the C_WEN checkbox to insert that signal on the generated macro. Click the signal arrow (when available) to toggle its polarity.

Pipeline for Read Address for Ports A and B

The default configuration for Micro SRAM is to enable the Pipeline of Read address (A_ADDR or B_ADDR). Uncheck the Pipeline option to turn off pipelining. This is a static selection and cannot be changed dynamically by driving it with a signal.

Turning off pipelining of Read address of a port also disables the configuration options of the respective ADDR_EN, ADDR_SRST_N and ADDR_ARST_N signals.

Pipeline for Read Data Output for Ports A and B

Click the Pipeline checkbox to enable pipelining of Read data (A_DOUT or B_DOUT). This is a static selection and cannot be changed dynamically by driving it with a signal.

Turning off pipelining of Read data of a port also disables the configuration options of the respective DOUT_EN, DOUT_SRST_N and DOUT_ARST_N signals.

Register Enable (A_ADDR_EN, A_DOUT_EN, B_ADDR_EN and B_DOUT_EN)

The address and pipeline registers for ports A and B have active high, enable inputs. The default configuration is to tie these signals to the active state and remove them from the generated macro. Click each signal's checkbox to insert that signal on the generated macro.

Click the signal arrow (when available) to toggle its polarity.

Synchronous Reset (A_ADDR_SRST_N, A_DOUT_SRST_N, B_ADDR_SRST_N and B_DOUT_SRST_N)

The address and pipeline registers for ports A and B have active low, synchronous reset inputs. The default configuration is to tie these signals to the inactive state and remove them from the generated macro. Click each signal's checkbox to insert that signal on the generated macro.

Click the signal arrow (when available) to toggle its polarity.

Asynchronous Reset (A_ADDR_ARST_N, A_DOUT_ARST_N, B_ADDR_ARST_N and B_DOUT_ARST_N)

The address and pipeline registers for ports A and B have active low, asynchronous reset inputs. The default configuration is to tie these signals to the inactive state and remove them from the generated macro. Click each signal's checkbox to insert that signal on the generated macro.

Click the signal arrow (when available) to toggle its polarity.

ADDR and DOUT Register Truth Table

Table 1-1 describes the functionality of the control signals on the A_ADDR, B_ADDR, A_DOUT and B_DOUT registers.

***Table 1-1* • Truth Table for A_ADDR, B_ADDR, A_DOUT, and B_DOUT Registers**

_ARST_N	Pipeline	_CLK	_EN	_SRST_N	d	q
0	x	x	x	x	x	0
1	T	Not rising	x	x	x	q
1	T	Rising	0	x	x	q
1	T	Rising	1	0	x	0
1	T	Rising	1	1	x	d
1	F	x	0	x	x	q
1	F	x	1	0	x	0
1	F	x	1	1	x	d

2 – Implementation Rules

Caveats for Micro SRAM generation

- If you use a word width of 9 or 18 for one port then the width of other ports cannot be 1, 2, or 4. However, configurations that do not use the 9th bit (e.g., Port A width of 512x4, Port B width of 256x8 and Port C width of 128x16) are supported.
- The core configurator only supports depth cascading up to 32 blocks.
- The core configurator does not generate RAM based on a specific device. See the datasheet for information on the available RAM64x18 modules in the device.
- The software returns a configuration error for unsupported configurations.

Note:

- All unused inputs must be grounded.
- Writing to and reading from the same address is undefined and should be avoided. There is no collision prevention or detection.
- Read from ports A and B at the same location is allowed.

3 – RAM Content Manager

The RAM Content Manager enables you to specify the contents of your memory so that you can avoid the simulation cycles required for initializing the memory, which reduces simulation runtime.

The RAM core generator takes away much of the complexity required in the generation of large memory that utilize one or more RAM blocks on the device. The configurator uses one or more memory blocks to generate a RAM matching your configuration. In addition, it also creates the surrounding cascading logic.

The configurator cascades RAM blocks in three different ways.

- Cascaded deep (e.g. 2 blocks of 1024x1 to create a 2048x1)
- Cascaded wide (e.g. 2 blocks of 1024x1 to create a 1024x2)
- Cascaded wide and deep (e.g. 4 blocks of 1024x1 to create a 2048x2, in a 2 blocks width-wise by 2 blocks depth-wise configuration)

Specify memory content in terms of your total memory size. The configurator must partition your memory file appropriately such that the right content goes to the right block RAM when multiple blocks are cascaded.

Supported Formats

The Microsemi implementation of these formats interprets data sets in bytes. This means that if the memory width is 7 bits, every 8th bit in the data set is ignored. Or, if the data width is 9, two bytes are assigned to each memory address and the upper 7 bits of each 2-byte pair are ignored.

The following examples illustrate how the data is interpreted for various word sizes:

For the given data: FF 11 EE 22 DD 33 CC 44 BB 55 (where 55 is the MSB and FF is the LSB)

For 32-bit word size:

```
0x22EE11FF (address 0)
0x44CC33DD (address 1)
0x000055BB (address 2)
```

For 16-bit word size:

```
0x11FF (address 0)
0x22EE (address 1)
0x33DD (address 2)
0x44CC (address 3)
0x55BB (address 4)
```

For 8-bit word size:

```
0xFF (address 0)
0x11 (address 1)
0xEE (address 2)
0x22 (address 3)
0xDD (address 4)
0x33 (address 5)
0xCC (address 6)
0x44 (address 7)
0xBB (address 8)
0x55 (address 9)
```

For 9-bit word size:

```
0x11FF -> 0x01FF (address 0)
0x22EE -> 0x00EE (address 1)
0x33DD -> 0x01DD (address 2)
0x44CC -> 0x00CC (address 3)
0x55BB -> 0x01BB (address 4)
```

Notice that for 9-bit, that the upper 7-bits of the 2-bytes are ignored.

INTEL-HEX

Industry standard file. Extensions are HEX and IHX. For example, file2.hex or file3.ihx.

A standard format created by Intel. Memory contents are stored in ASCII files using hexadecimal characters. Each file contains a series of records (lines of text) delimited by new line, '\n', characters and each record starts with a ':' character. For more information regarding this format, refer to the Intel-Hex Record Format Specification document available on the web (search Intel Hexadecimal Object File for several examples).

The Intel Hex Record is composed of five fields and arranged as follows:

```
:llaaaatt[dd...]cc
```

Where:

- : is the start code of every Intel Hex record
- ll is the byte count of the data field
- aaaa is the 16-bit address of the beginning of the memory position for the data. Address is big endian.
- tt is record type, defines the data field:
  - 00 data record
  - 01 end of file record
  - 02 extended segment address record
  - 03 start segment address record (ignored by Microsemi SoC tools)
  - 04 extended linear address record
  - 05 start linear address record (ignored by Microsemi SoC tools)
- [dd...] is a sequence of n bytes of the data; n is equivalent to what was specified in the ll field
- cc is a checksum of count, address, and data

Example Intel Hex Record:

```
:0300300002337A1E
```

MOTOROLA S-record

Industry standard file. File extension is S, such as file4.s

This format uses ASCII files, hex characters, and records to specify memory content in much the same way that Intel-Hex does. Refer to the Motorola S-record description document for more information on this format (search Motorola S-record description for several examples). The RAM Content Manager uses only the S1 through S3 record types; the others are ignored.

The major difference between Intel-Hex and Motorola S-record is the record formats, and some extra error checking features that are incorporated into Motorola S.

In both formats, memory content is specified by providing a starting address and a data set. The upper bits of the data set are loaded into the starting address and leftovers overflow into the adjacent addresses until the entire data set has been used.

The Motorola S-record is composed of 6 fields and arranged as follows:

```
Stllaaaa[dd...]cc
```

Where:

- S is the start code of every Motorola S-record
- t is record type, defines the data field
- ll is the byte count of the data field
- aaaa is a 16-bit address of the beginning of the memory position for the data. Address is big endian.

- [dd...] is a sequence of n bytes of the data; n is equivalent to what was specified in the llfield
- cc is the checksum of count, address, anddata

Example Motorola S-Record:

```
S10a0000112233445566778899FFFA
```

RAM Content Manager Functionality

To open the RAM Content Manager, after specifying your RAM configurations (set your Read and Write Depth and Width), select the **Initialize RAM for Simulation** checkbox, and then click **Customize RAM Content**. The RAM Content Manager appears (Figure 3-1).

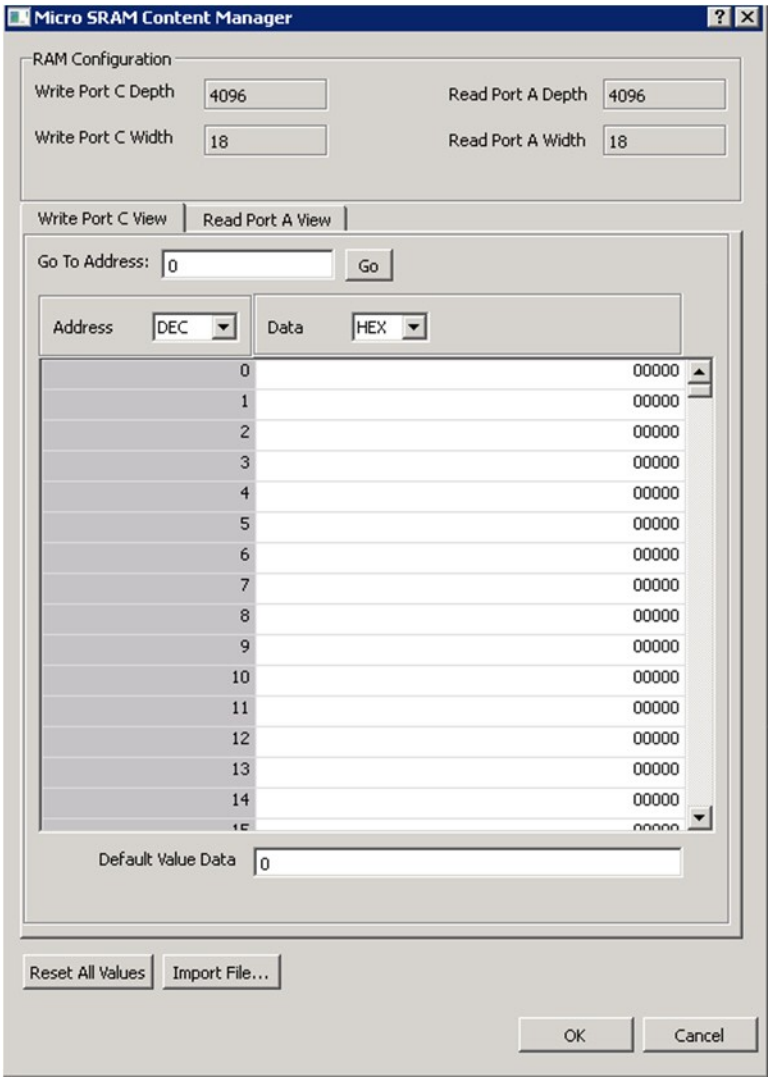

***Figure 3-1* • Customize RAM Content for Simulation**

RAM Configuration

Write Depth and Write Width - As specified in the RAM core generator dialog box (not editable).

Read Depth and Read Width - As specified in the RAM core generator dialog box (not editable).

Write Port View / Read Port View

Go To Address - Enables you to go to a specific address in the manager. Each memory block has many addresses; it is often difficult to scroll through and find a specific one. This task is simplified by enabling you to type in a specific address. The number display format (Hex, Bin, Dec) is controlled by the value you set in the drop-down menu above the Address column.

Address - The Address column lists the address of a memory location. The drop-down menu specifies the number format for your address list (hexadecimal, binary, or decimal).

Data - Enables you to control the data format and data value in the manager. Click the value to change it.

Note that the dialogs show all data with the MSB down to LSB. For example, if the row showed 0xAABB for a 16-bit word size, the AA would the MSB and BB would be LSB.

Default Data Value - The value given to memory addresses that have not been explicitly initialized (by importing content or editing manually). When changed, all default values in the manager are updated to match the new value. The number display format (Hex, Bin, Dec) is controlled by the value you set in the drop-down menu above the Data column.

Reset All Values - Resets the Data values.

Import File - Opens the Import Memory Content dialog box; enables you to select a memory content file (Intel-Hex) to load. Intel-Hex file extensions are set to *.hex during import.

OK - Closes the manager and saves all the changes made to the memory and its contents.

Cancel - Closes the manager, cancels all your changes in this instance of the manager, and returns the memory back to the state it held before the manager was opened.

MEMFILE (RAM Content Manager output file)

Transfer of RAM data (from the RAM Content Manager) to test equipment is accomplished via MEM files. The contents of your RAM is first organized into the logical layer and then reorganized to fit the hardware layer. Then it is stored in MEM files that are read by other systems and used for testing.

The MEM files are named according to the logical structure of RAM elements created by the configurator. In this scheme the highest order RAM blocks are named CORE_R0C0.mem, where "R" stands for row and "C" stands for column. For multiple RAM blocks, the naming continues with CORE_R0C1, CORE_R0C2, CORE_R1C0, etc.

The data intended for the RAM is stored as ASCII 1s and 0s within the file. Each memory address occupies one line. Words from logical layer blocks are concatenated or split in order to make them fit efficiently within the hardware blocks. If the logical layer width is less than the hardware layer, two or more logical layer words are concatenated to form one hardware layer word. In this case, the lowest bits of the hardware word are made up of the lower address data bits from the logical layer. If the logical layer width is more than the hardware layer, the words are split, placing the lower bits in lower addresses.

If the logical layer words do not fit cleanly into the hardware layer words, the most significant bit of the hardware layer words is not used and defaulted to zero. This is also done when the logical layer width is 1 in order to avoid having left over memory at the end of the hardware block.

4 – Port Description

Table 4-1 lists the Micro SRAM signals in the generated macro.

***Table 4-1* • Micro SRAM Signals**

Port	Direction	Polarity	Description
CLK	In	Rising edge	Single clock signal that drives all three ports with the same clock
A_BLK	In	Active High	Port A enable
A_ADDR[]	In		Port A Read address
A_ADDR_EN	In	Active High	Port A address register Enable
A_ADDR_SRST_N	In	Active Low	Port A address register Synchronous reset
A_ADDR_ARST_N	In	Active Low	Port A address register Asynchronous reset
A_CLK	In	Rising edge	Port A clock
A_DOUT[]	Out		Port A Read data
A_DOUT_EN	In	Active High	Port A Read data register Enable
A_DOUT_SRST_N	In	Active Low	Port A Read data register Synchronous reset
A_DOUT_ARST_N	In	Active Low	Port A Read data register Asynchronous reset
B_BLK	In	Active High	Port B Enable
B_ADDR[]	In		Port B Read address
B_ADDR_EN	In	Active High	Port B address register Enable
B_ADDR_SRST_N	In	Active Low	Port B address register Synchronous reset
B_ADDR_ARST_N	In	Active Low	Port B address register Asynchronous reset
B_CLK	In	Rising edge	Port B clock
B_DOUT[]	Out		Port B Read data
B_DOUT_EN	In	Active High	Port B Read data register Enable
B_DOUT_SRST_N	In	Active Low	Port B Read data register Synchronous reset
B_DOUT_ARST_N	iN	Active Low	Port B Read data register Asynchronous reset
C_BLK	In	Active High	Port C Enable
C_ADDR[]	In		Port C Write address
C_CLK	In	Rising edge	Port C clock
C_DIN[]	In		Port C Write data
C_WEN	In	Active High	Port C Write enable

5 – Parameters

Table 5-1 lists the Micro SRAM parameters in the generated macro.

***Table 5-1* • Micro SRAM Parameters**

Parameter	Valid Range	Default	Description
DESIGN			Name of the generated macro
FAM	SmartFusion2		Target family
OUTFORMAT	Verilog, VHDL		Netlist format
LPMTYPE	LPM_URAM		Macro category
DEVICE	500 - 5000	5000	Target device
INIT_RAM	F, T	F	Initialize RAM for simulation
CASCADE	0, 1	0	0: Cascading for WIDTH or Speed 1: Cascading for DEPTH or Power
CLKS	1, 3	1	1: Single Read/Write Clock 3: One Clock per port
RWIDTH1	1-1296	18	Port A Read data width
RDEPTH1	1-32768	64	Port A Read address depth
RWIDTH2	1-1296	18	Port B Read data width
RDEPTH2	1-32768	64	Port B Read address depth
WWIDTH	1-1296	18	Port C Write data width
WDEPTH	1-32768	64	Port C Write address depth
A_BLK_POLARITY	0, 1, 2	2	0: Active-low Port A enable 1: Active-high Port A enable 2: Port A enable tied off to be always active
A_ADDR_LAT	0, 1	0	0: Pipeline Port A Read address 1: Bypass Port A Read address register
A_ADDR_EN_POLARITY	A_ADDR_LAT=0 0, 1, 2	2	0: Active-low Port A read address register enable 1: Active-high Port A read address register enable 2: Port A read address register enable tied off to be always active
A_ADDR_SRST_POLARITY	A_ADDR_LAT=0 0, 1, 2	2	0: Active-low Port A read address register Sync-reset 1: Active-high Port A read address register Sync-reset 2: Port A read address register Sync-reset tied off to be always inactive
A_ADDR_ARST_POLARITY	A_ADDR_LAT=0 0, 1, 2	2	0: Active-low Port A read address register Async-reset 1: Active-high Port A read address register Async-reset 2: Port A read address register Async-reset tied off to be always inactive
A_CLK_EDGE	CLKS=3 RISE, FALL	RISE	RISE: Rising edge Port A clock FALL: Falling edge Port A clock
A_DOUT_LAT	0, 1	1	0: Pipeline Port A Read data 1: Bypass Port A Read data register

***Table 5-1* • Micro SRAM Parameters (continued)**

Parameter	Valid Range	Default	Description
A_DOUT_EN_POLARITY	A_DOUT_LAT=0 0, 1, 2	2	0: Active-low Port A read data register enable 1: Active-high Port A read data register enable 2: Port A read data register enable tied off to be always active
A_DOUT_SRST_POLARITY	A_DOUT_LAT=0 0, 1, 2	2	0: Active-low Port A read data register Sync-reset 1: Active-high Port A read data register Sync-reset 2: Port A read data register Sync-reset tied off to be always inactive
A_DOUT_ARST_POLARITY	A_DOUT_LAT=0 0, 1, 2	2	0: Active-low Port A read data register Async-reset 1: Active-high Port A read data register Async-reset 2: Port A read data register Async-reset tied off to be always inactive
B_BLK_POLARITY	0, 1, 2	2	0: Active-low Port B enable 1: Active-high Port B enable 2: Port B enable tied off to be always active
B_ADDR_LAT	0, 1	0	0: Pipeline Port B Read address 1: Bypass Port B Read address register
B_ADDR_EN_POLARITY	B_ADDR_LAT=0 0, 1, 2	2	0: Active-low Port B read address register enable 1: Active-high Port B read address register enable 2: Port B read address register enable tied off to be always active
B_ADDR_SRST_POLARITY	B_ADDR_LAT=0 0, 1, 2	2	0: Active-low Port B read address register Sync-reset 1: Active-high Port B read address register Sync-reset 2: Port B read address register Sync-reset tied off to be always inactive
B_ADDR_ARST_POLARITY	B_ADDR_LAT=0 0, 1, 2	2	0: Active-low Port B read address register Async-reset 1: Active-high Port B read address register Async-reset 2: Port B read address register Async-reset tied off to be always inactive
B_CLK_EDGE	CLKS=3 RISE, FALL	RISE	RISE: Rising edge Port B clock FALL: Falling edge Port B clock
B_DOUT_LAT	0, 1	1	0: Pipeline Port B Read data 1: Bypass Port B Read data register
B_DOUT_EN_POLARITY	B_DOUT_LAT=0 0, 1, 2	2	0: Active-low Port B read data register enable 1: Active-high Port B read data register enable 2: Port B read data register enable tied off to be always active
B_DOUT_SRST_POLARITY	B_DOUT_LAT=0 0, 1, 2	2	0: Active-low Port B read data register Sync-reset 1: Active-high Port B read data register Sync-reset 2: Port B read data register Sync-reset tied off to be always inactive
B_DOUT_ARST_POLARITY	B_DOUT_LAT=0 0, 1, 2	2	0: Active-low Port B read data register Async-reset 1: Active-high Port B read data register Async-reset 2: Port B read data register Async-reset tied off to be always inactive
C_BLK_POLARITY	0, 1, 2	1	0: Active-low Port C enable 1: Active-high Port C enable 2: Port C enable tied off to be always active
C_CLK_EDGE	RISE, FALL	RISE	RISE: Rising edge Write-clock or Single Clock FALL: Falling edge Write-clock or Single Clock
C_WEN_POLARITY	0, 1, 2	2	0: Active-low Port C Write enable 1: Active-high Port C Write enable 2: Port C Write enable tied off to be always active
CLOCK_PN	CLKS=1	CLK	Single clock Port name

***Table 5-1* • Micro SRAM Parameters (continued)**

Parameter	Valid Range	Default	Description
A_BLK_PN	A_BLK_POLARITY<2	A_BLK	A_BLK Port name
A_ADDR_PN		A_ADDR	A_ADDR Port name
A_ADDR_EN_PN	A_ADDR_LAT=0	A_ADDR_EN	A_ADDR_EN Port name
A_ADDR_SRST_PN	A_ADDR_LAT=0	A_ADDR_SRST_N	A_ADDR_SRST_N Port name
A_ADDR_ARST_PN	A_ADDR_LAT=0	A_ADDR_ARST_N	A_ADDR_ARST_N Port name
A_CLK_PN	CLKS=3	A_CLK	A_CLK Port name
A_DOUT_PN		A_DOUT	A_DOUT Port name
A_DOUT_EN_PN	A_DOUT_LAT=0	A_DOUT_EN	A_DOUT_EN Port name
A_DOUT_SRST_PN	A_DOUT_LAT=0	A_DOUT_SRST_N	A_DOUT_SRST_N Port name
A_DOUT_ARST_PN	A_DOUT_LAT=0	A_DOUT_ARST_N	A_DOUT_ARST_N Port name
B_BLK_PN	B_BLK_POLARITY<2	B_BLK	B_BLK Port name
B_ADDR_PN		B_ADDR	B_ADDR Port name
B_ADDR_EN_PN	B_ADDR_LAT=0	B_ADDR_EN	B_ADDR_EN Port name
B_ADDR_SRST_PN	B_ADDR_LAT=0	B_ADDR_SRST_N	B_ADDR_SRST_N Port name
B_ADDR_ARST_PN	B_ADDR_LAT =0	B_ADDR_ARST_N	B_ADDR_ARST_N Port name
B_CLK_PN	CLKS=3	B_CLK	B_CLK Port name
B_DOUT_PN		B_DOUT	B_DOUT Port name
B_DOUT_EN_PN	B_DOUT_LAT=0	B_DOUT_EN	B_DOUT_EN Port name
B_DOUT_ARST_PN	B_DOUT_LAT=0	B_DOUT_ARST_N	B_DOUT_ARST_N Port name
B_DOUT_SRST_PN	B_DOUT_LAT=0	B_DOUT_SRST_N	B_DOUT_SRST_N Port name
C_BLK_PN	C_BLK_POLARITY<2	C_BLK	C_BLK Port name
C_ADDR_PN		C_ADDR	C_ADDR Port name
C_CLK_PN	CLKS=3	C_CLK	C_CLK Port name
C_DIN_PN		C_DIN	C_DIN Port name
C_WEN_PN	C_WEN_POLARITY<2	C_WEN	C_WEN Port name
COLLISION_WARN_MSGS	-1, 0, >0	-1	-1: All warning messages related to collisions will appear in the simulation log. 0: One warning message related to collisions will appear in the simulation log. >0: More than one warning message equal to the integer value passed to the parameter related to collisions will appear in the simulation log.

A – Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call 800.262.1060
From the rest of the world, call 650.318.4460
Fax, from anywhere in the world, 408.643.6913

Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

Visit the Customer Support website (www.microsemi.com/soc/support/search/default.aspx) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the website.

Website

You can browse a variety of technical and non-technical information on the SoC home page, at www.microsemi.com/soc.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

My Cases

Microsemi SoC Products Group customers may submit and track technical cases online by going to My Cases.

Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office. Sales office listings can be found at www.microsemi.com/soc/company/contact/default.aspx.

ITAR Technical Support

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech_itar@microsemi.com. Alternatively, within My Cases, select **Yes** in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the ITAR web page.

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