SmartFusion2 MSS
Clocks Configuration

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Introduction

The MSS Clock Conditioning Circuitry (MSS CCC) provides a single place where all clocks related to the MSS and the communication between the MSS and the FPGA fabric can be configured.

The MSS_CCC configurator is organized into tabs: System Clocks and Advanced Options (Figure 1).

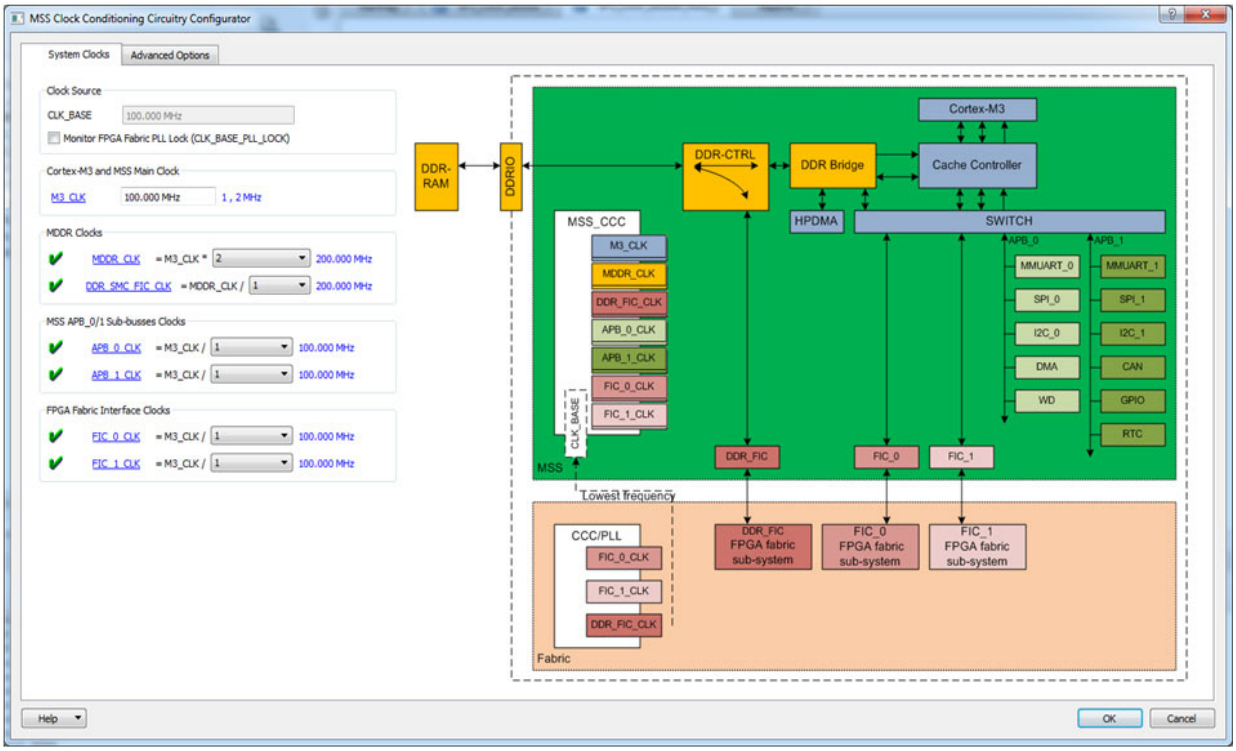

***Figure 1* • MSS CCC Configurator**

System Clocks

The System Clocks tab (Figure 2) enables you to configure/view:

- The MSS CCC clock source CLK_BASE. The Configurator computes the frequency for you based on how the other clocks are configured.
- The main MSS clock M3_CLK
  - Enter a value below 167 MHz to drive the Cortex-M3 Processor.
  - This is a limitation of the Cortex-M3.
- The MDDR related clocks (MDDR_CLK and DDR_SMC_FIC_CLK)
  - MDDR_CLK and DDR_SMC_FIC_CLK must be between 20 MHz and 334 MHz.
- The MSS APB_0 and APB_1 Peripheral clocks (APB_0_CLK and APB_1_CLK)
  - Choose a divisor of 1, 2, 4 or 8 to divide into the M3_CLK frequency to get the APB_0_CLK and APB_1_CLK frequency you want.
- The two Fabric Interface (FIC) clocks (FIC_0_CLK and FIC_1_CLK)
  - Choose a divisor of 1, 2, 4, 8, 16 or 32 to divide into the M3_CLK frequency to get the FIC_0_CLK and FIC_1_CLK frequency you want.

Only the clocks used in your design are editable for configuration in the MSS CCC configurator. Make sure to enable and correctly configure all the MSS sub-blocks you intend to use in your design before configuring the MSS CCC sub-block. What can be configured and how (rules) depends on what is being used; see "System Clocks Configuration" on page 6 for details.

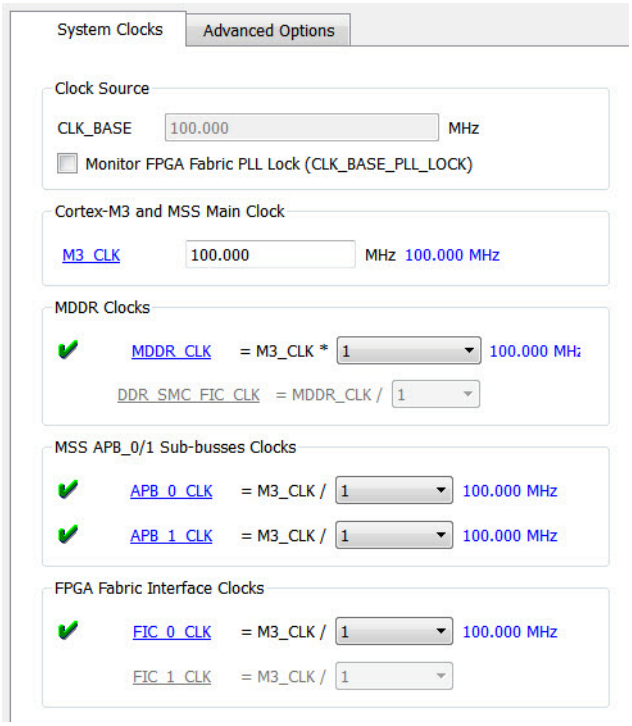

***Figure 2* • System Clocks Tab**

The System Clocks tab displays a high level block diagram of your design displayed based on what you have enabled/disabled/configured in the MSS configurator. The block diagram shows the different clock domains (each clock domain is a different color) within the MSS as well as the clock domains that cross into the FPGA fabric. If you click any of the clocks (blue labels) you will see that particular clock domain

highlighted on the block diagram Figure 3 shows the M3_CLK clock domain highlighted. It shows what components this clock is driving.

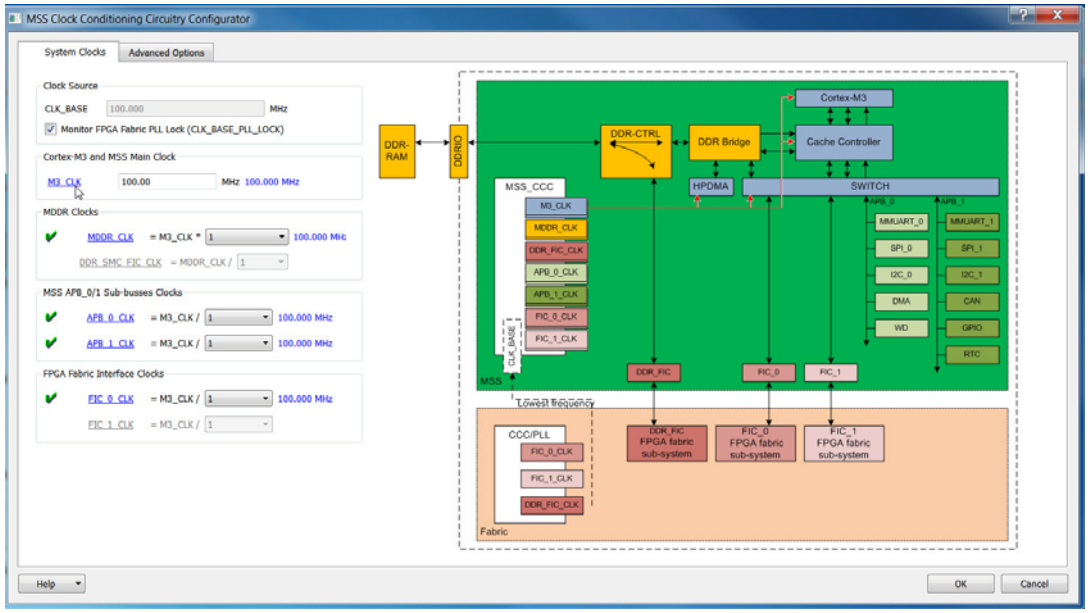

***Figure 3* • M3_CLK Domain Highlighted**

Advanced Options

You can also configure more advanced options related to the PLL LOCKs using the Advanced tab. See "Advanced Options" on page 9 for a summary.

1 – System Clocks Configuration

The System Clocks tab (Figure 1-1) enables you to configure:

- The MSS CCC clock source CLK_BASE
- The main MSS clock M3_CLK
- The MDDR related clocks (MDDR_CLK and DDR_SMC_FIC_CLK)
- The MSS APB_0 and APB_1 Peripheral clocks (APB_0_CLK and APB_1_CLK)
- The two Fabric Interface (FIC) clocks (FIC_0_CLK and FIC_1_CLK)

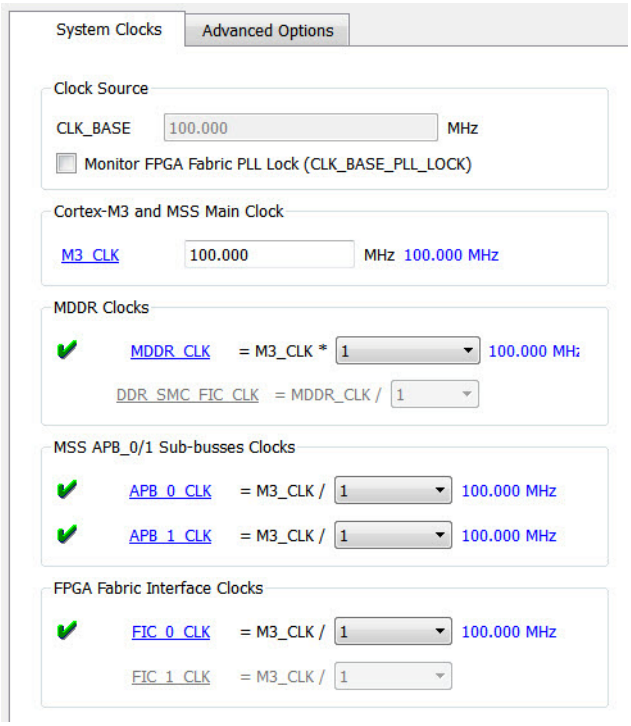

***Figure 1-1* • System Clocks Configuration Tab**

MSS CCC Clock Source

In normal operating mode (non Flash*Freeze) the MSS CCC is configured to be sourced from the FPGA fabric via the CLK_BASE port.

If you use any of the FIC clocks (DDR_SMC_FIC_CLK, FIC_0_CLK and FIC_1_CLK), CLK_BASE is automatically set at the lowest frequency of any of the used FIC clocks and is not editable. In this case, when MSS outputs and inputs are to/from the fabric, the MSS I/Os are synchronous to CLK_BASE. For a more comprehensive system level view of the clocking methodology for interfacing the MSS and the FPGA fabric through the MSS FICs, refer to the SmartFusion2 MSS Creating a Design using MSS Fabric Interfaces document.

If none of the FIC clocks are used, the CLK_BASE frequency is editable and you can select a clock frequency between 1 MHz and 200 MHz. In this case, the MSS I/Os are asynchronous.

If CLK_BASE is sourced by a PLL in the FPGA fabric, you should connect the PLL LOCK signal from that fabric CCC to the MSS CLK_BASE_PLL_LOCK. When the chip system controller boots the device (at

PoR or when the external pin DEVRST_N has been asserted/de-asserted) it monitors the external PLL LOCK as well as the internal MPLL LOCK and only switches to the clock configurations defined in this configurator when the PLL have a stable lock.

Cortex-M3 and MSS Main Clock (M3_CLK)

The main clock for the Cortex-M3 and the MSS is M3_CLK; you must define its frequency.

The following rules must be satisfied and are checked by the MSS_CCC configurator as you enter a frequency for M3_CLK:

1. The M3_CLK frequency must be less than or equal to 167 MHz.
2. The MDDR_CLK frequency must be less than or equal to 333 MHz.
3. If the CAN peripheral is used M3_CLK must be a multiple of 8 MHz.
4. If the USB peripheral is used M3_CLK must be greater than 30.1 MHZ.

MDDR Clocks (MDDR_CLK and DDR_SMC_FIC_CLK)

When the MDDR sub-block is configured as a DDR interface:

- The MDDR_CLK drives the DDR controller and the DDR Bridge in the MSS. You can select this clock to be a multiple - 1, 2, 3, 4, 6 or 8 - of the main MSS clock M3_CLK.
- The DDR_SMC_FIC_CLK drives the DDR FIC slave interface and defines the frequency at which the FPGA fabric sub-system connected to this interface is intended to run. You can select this clock to be a ratio - 1, 2, 3, 4, 6, 8, 12, or 16 - of MDDR_CLK. To enable this, you need to enable Fabric Interface Settings (i.e., FIC64) in the MDDR configurator.
- If MDDR_CLK ratio to M3_CLK is a multiple of 3, DDR_SMC_FIC_CLK's ratio to MDDR_CLK must also be a multiple of 3, and vice versa. The configurator issues an error if this requirement is not met. This limitation is imposed by the internal implementation of the MSS CCC.

When the MDDR sub-block is configured as a Soft Memory Controller (SMC) interface:

- The MDDR_CLK drives the DDR Bridge in the MSS. It is automatically set by the configurator to be equal to M3_CLK and is not editable.
- The DDR_SMC_FIC_CLK drives the SMC master fabric interface. It is automatically set by the configurator to be equal to M3_CLK and is not editable.

MSS APB_0 and APB_1 Sub-busses Clocks (APB_0_PCLK and APB_1_PCLK)

There are two internal APB sub-busses in the MSS: APB_0 and APB_1. Each of these sub-busses peripheral is clocked by APB_0_CLK and APB_1_CLK, respectively. These clocks are derived from the main MSS clock M3_CLK. Each APB clock can be programmed individually as M3_CLK divided by 1, 2, 4 or 8.

Note: Some peripherals may require a slower Peripheral clock (PCLK) to achieve certain configurations. Changing the APB sub-bus PCLK affects all peripherals present on that bus.

FPGA Fabric Interface Clocks (FIC_0_CLK and FIC_1_CLK)

For applications where the AMBA fabric Interface is used to connect to a soft AMBA sub-system (soft bus/bridge/peripheral cores), the FIC sub-system clocks (FIC_0_CLK and FIC_1_CLK) must be configured such that the generated frequencies meet the timing requirements of the FPGA logic implemented in the fabric for each FIC sub-system.

The FPGA fabric clocks, when used, can only be the MSS clock divided by 1, 2, 4, 8, 16 or 32. You must verify that the FPGA fabric timing for each FIC sub-system meets the selected fabric clock frequency by performing timing analysis of your design using SmartTime.

For a more comprehensive system level view of the clocking methodology for interfacing the MSS and the FPGA fabric through the MSS FICs, refer to the SmartFusion2 MSS Creating a Design Using MSS Fabric Interfaces document.

2 – Advanced Options

The Advanced Options tab enables you to configure Advanced PLL Lock Options:

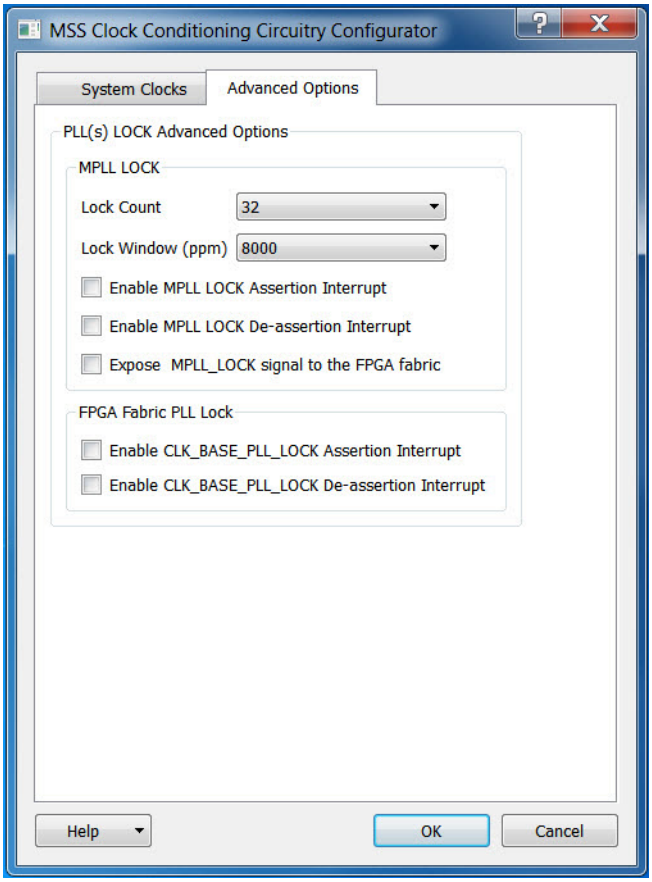

***Figure 2-1* • Advanced Options Configuration Tab**

PLL Lock(s) Advanced Options

Lock Count (Delay) - Sets the number of CLK_BASE (reference clock) clock cycles by which the lock is delayed after the MPLL has reached the lock condition. The default value is 32.

Lock Window (ppm) - Configures the maximum phase error allowed for the MPLL to indicate it has locked. The lock window is expressed as parts per million (ppm) of the reference frequency. The default value is 8,000.

You can enable interrupts to the Cortex-M3 to monitor assertions and de-assertions of the MPLL lock.

You can expose the MPLL LOCK signal to the FPGA fabric and use it as part of your design to monitor the health of the MPLL (loss or lock may require special handling by your application).

You can enable interrupts to the Cortex-M3 to monitor assertions and de-assertions of the CLK_BASE PLL lock if you are monitoring this signal by checking the Monitor FPGA Fabric PLL Lock (CLK_BASE_PLL_LOCK) checkbox (Figure 3).

A – Product Support

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Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call **800.262.1060**
From the rest of the world, call **650.318.4460**
Fax, from anywhere in the world, **650.318.8044**

Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

For Microsemi SoC Products Support, visit http://www.microsemi.com/products/fpga-soc/design-support/fpga-soc-support.

Website

You can browse a variety of technical and non-technical information on the Microsemi SoC Products Group home page, at www.microsemi.com/soc.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

My Cases

Microsemi SoC Products Group customers may submit and track technical cases online by going to My Cases.

Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office.

Visit About Us for sales office listings and corporate contacts.

Sales office listings can be found at www.microsemi.com/soc/company/contact/default.aspx.

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For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech_itar@microsemi.com. Alternatively, within My Cases, select **Yes** in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the ITAR web page.

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