UG0689
User Guide
Chip Planner

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA

Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
E-mail: sales.support@microsemi.com

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Contents

Introduction

The Chip Planner is a Graphical Interface Tool that provides a Chip View and a Netlist View.

The Chip View allows you to create regions, edit regions, and make logic assignments to regions. It is a floorplanning tool used to improve the timing performance and routability of your design by providing maximum control over your design object placement.

The Netlist Viewer provides a schematic view of the design that allows you to examine the routing of the nets and reveal any routing congestions.

You can also cross-probe from SmartTime into Chip Planner to browse your design and look into timing problems.

Use Chip Planner to:

- View macro assignments made during layout.
- Assign, unassign, or move macros.
- Lock macro assignments.
- View net connections using a ratsnest view.
- View architectural boundaries.
- View and edit silicon features, such as I/O banks.
- Create Regions and assign macros or nets to regions (floorplanning).
- View logic placement and net connections to investigate timing problems together with SmartTime's Cross-Probing feature.
- View the hierarchical netlist after Synthesis and the flattened netlist after Compile
- Create logical cones for debugging and detailed analysis.

You must run Synthesis and Compile Netlist on your design before invoking Chip Planner. If you do not, Libero runs Synthesis and Compile Netlist before opening Chip Planner. You can invoke Chip Planner for floorplanning after running Place and Route to improve routability and remove congestion.

When floorplanning, you analyze your design to see if certain logic can be grouped within regions. Placement regions are especially useful for hierarchical designs with plenty of local connectivity within a block. If your timing analysis indicates several paths with negative slack, try grouping the logic included in these paths into their own regions. This forces the placement of logic within the path closer together and may improve timing performance of the design.

Supported Families and Platforms

Chip Planner supports the SmartFusion2, IGLOO2, RTG4, and PolarFire devices and runs on Windows and Linux systems.

Invoking Chip Planner

When you first create a project in SmartFusion2, IGLOO2, or RTG4, the design flow option you select for the project determines the way Chip Planner is accessed. There are two design flows available in Libero SoC:

- Classic Constraint Flow option

  Note: This is only available for SmartFusion2, IGLOO2, and RTG4 devices.
- Enhanced Constraint Flow option, which has a single centralized Constraint Manager to manage all design constraints for the design.

When you first create a project in PolarFire, only one constraint flow is available. This is the default, and is the equivalent of the Enhanced Constraint Flow.

Invoking Chip Planner (Classic Constraint Flow)

Note: This section is applicable only for SmartFusion2, IGLOO2, and RTG4 projects created with the Classic Constraint Flow.

If you select the Classic Design Flow when you first create the project, invoke Chip Planner from the Design Flow window (**Design Flow window** > **Edit Constraints** > **Chip Planner** > **Open Interactively**) or double-click **Chip Planner** in the Design Flow window.

Note: You must have successfully completed the Synthesis step and the Compile step before Chip Planner can be opened. If you do not, Libero SoC executes these steps for you before it opens Chip Planner.

PDC Files in Classic Constraint Flow

When Chip Planner opens, only the PDC constraint file(s) marked “Use For Compile” are loaded into Chip Planner for reading. PDC constraint files in the project not marked as such are ignored by Chip Planner.

When you make an I/O or floorplanning change in Chip Planner, commit, and save, PDC files are created: a <root>_io.pdc file for I/O changes and a <root>_fp.pdc file for floorplanning changes.

The <root>_io.pdc file is located in the <proj>\constraints\io folder.

The <root>_fp.pdc file is located in the <proj>\constraints\fp folder.

Invoking Chip Planner (Enhanced Constraint Flow)

Note: This section is applicable for all PolarFire projects, and SmartFusion2, IGLOO2, and RTG4 projects using the Enhanced Constraint Flow.

If you have selected the Enhanced Constraint Flow option when your first create the project, invoke Chip Planner from the Constraint Manager (**Design Flow window** > **Manage Constraints** > **Open Manage Constraints View** > **Constraint Manager** > **Floor Planner > Edit with Chip Planner)** or double-click **Chip Planner** under Edit Constraints in the Design Flow window**.**

Note: You must complete the Synthesis or Compile step before invoking Chip Planner from the Constraint Manager. If you do not, a pop-up message appears telling you to run these steps first.

PDC Files in Enhanced Constraint Flow

When Chip Planner opens, only the PDC file(s) associated with Place and Route are loaded into Chip Planner for reading. PDC files in your project not associated with Place and Route are ignored.

When you make an I/O or floorplanning change in Chip Planner, commit, and save, the change is saved to a *.pdc file that you have set as target in the Constraint Manager. If no PDC constraint file is set as target, the change is written to a new user.pdc file. When the change is related to floorplanning, the user.pdc file is displayed in the Floor Planner tab. When the change is related to I/Os, the user.pdc file is displayed in the I/O Attributes tab.

The I/O PDC files are located in the <proj>\constraints\io folder.

The Floorplanning PDC files are located in the <proj>\constraints\fp folder.

Chip Planner Splash Screen

The Chip Planner splash screen appears when it is invoked.

***Figure 1* • Chip Planner Splash Screen**

Chip Planner and PDC Commands/Files

Chip Planner is an interactive tool for floorplanning. The floorplanning changes you make in Chip Planner are saved as PDC (Physical Design Constraints) commands in PDC file(s). Interactive floorplanning actions in Chip Planner have corresponding PDC commands which can be made part of a constraint file for Place and Route.

For details about SmartFusion2, IGLOO2, and RTG4 PDC commands, refer to the PDC Commands User Guide.

For details about PolarFire PDC commands, refer to the PolarFire PDC Commands User Guide

The Chip Planner and some other tools have access to and write to the same PDC file(s). When more than one of these tools are opened, making and saving changes (from any one tool) is not allowed. This is to prevent the user from inadvertently overwriting the constraints in the PDC file(s). A message pops up to alert you to the modification conflict and tells you what tool or tools are open and need to be closed.

To fix the modification conflict:

1. Close the tool or tools and leave only one tool open.
2. Make and save the changes in the tool.

1 – Chip Planner Views

When the ChipPanner Graphical Interface launches, it opens with the following windows:

- Design View window
- Canvas window
- Log window
- Display Options window
- Properties window
- World View window

All windows can be docked or undocked (floating), turned on or off, resized, or moved to the right, left, top, or bottom of the Chip Planner application. Docked windows can be stacked horizontally or vertically

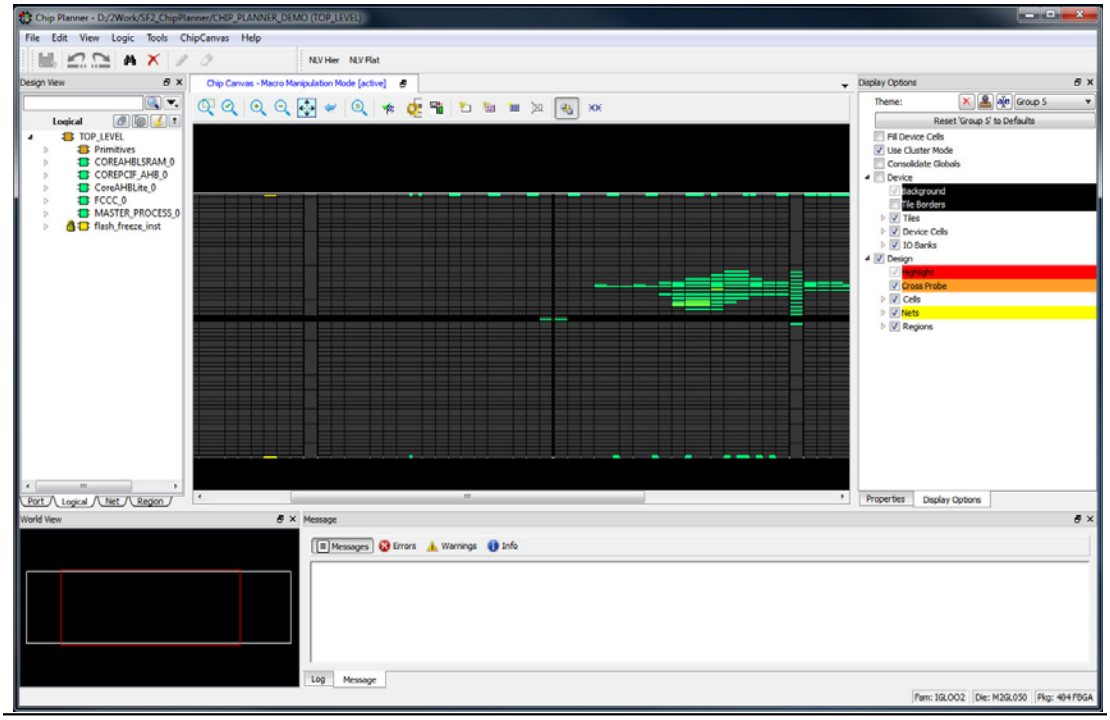


***Figure 1-1* • Chip Planner**

The Design View window provides the following view tabs for the design:

- Port
- Logical
- Net
- Region
- Block (only when the design instantiates a design block)

Table 1-1 lists the icons in the toolbar. Hover the mouse on the icon shown on Chip Canvas to see the tooltip.

***Table 1-1* • Chip Planner Toolbar Icons**

Icon	Name	Function
	Commit	Commit and Save will: • Run Chip Planner DRC before saving the changes. • Write/Update the PDC files.
	Undo	Reverse your last action.
	Redo	Reverse the action of your last Undo Command.
	Find /CTRL + F	Clone a Find window for a specific view (Logical/ Port/ Net,/Region/Block) depending on the view you are in when you click this icon or CTRL + F. Multiple Find windows may be cloned, each with a different set of filtering criteria, to give you multiple filtered views of design elements.
	Clear	Clear All Find Trees.
	Highlight	Highlight a net, macro or a port.
	Unhighlight All	Unhighlight all highlighted selections (macro, net or port).

In addition, there are special icons common to all the five views: Port, Logical, Net, Region, and Block. A tooltip is available for each icon.

Table 1-2 shows a list of special icons common to all the five views.

***Table 1-2* • Special Icons in the Design View Window**

Icon	Name	Function
	Reapply the Filter	Reapply the Filter and Sort (if any)
	Filter	Apply the Filter to design object display
	Collapse	Collapse the hierarchical display in the view.
	Expand	Expand the selected design object
	Clear	Clear the Filter and refresh the tree reflecting no filters applied.
	Change Sort Order and allow Additional Filtering	Change Sort Order (Ascending/ Descending) or Apply Additional Filtering. Sort and Filter criteria vary with the view.
	Rename Tree	Rename a cloned Find Window to a name different from the default name. Available only in the cloned Find Window.
	Delete Tree	Delete the cloned Find Window. Available only in the cloned Find Window.

All Chip Planner windows can be docked or undocked.

***Table 1-3* • Window Management Icons**

Icon	Name	Function
	Dock/Undock	Dock or Undock (Float) the window
	Close	Close the window

The Chip Planner provides the following special keys and hot keys.

***Table 1-4* • Special Keys/Hot Keys**

Hot Keys/Special Keys	Function
CTRL + F	Find/Search function. Creates a cloned Find Window.
CTRL + Z	Undo the last action/command.
CTRL + S	Save all changes.
CTRL + Y	Redo last action/command.
Home	Scroll to the first selected item in the view.
End	Scroll to the last selected item in the view.
Tab	Scroll to the next selected item in the view.
Shift + Tab	Scroll to the previous selected item.
CTRL + Q	Exit Chip Planner
CTRL + ++	Zoom In
CTRL + --	Zoom Out
CTRL + 0	Zoom to Fit
CTRL + H	Lock All Macros
SHIFT + CTRL + H	Unlock All Macros
Hold SHIFT + Left_Mouse Click	Select multiple elements in Design View Windows
Hold CTRL + Left Mouse click	Select multiple elements in Design View Windows
ESC	Unselect all selected items. Remove any pop-up windows
<Right Arrow key>	Select Element at next level of hierarchy in design flow window
<Left Arrow key>	Select element at previous level of hierarchy in design flow window.
<Down Arrow key>	Select next element at the same level of hierarchy in design flow window
<Up Arrow key>	Select previous element at the same level of hierarchy in the design flow window.

Design View Window and View Tabs

When Chip Planner opens, it presents a Design View Window with five view tabs:

- Port
- Logical
- Net
- Region
- Block - only if user blocks (*.cxz files) exist in the design

Each of the view tabs displays a design view. A selection of a design element in one view is reflected in other views. For example, when you click and select a bus port in the Port view, the Logical view shows the OUTBUF/INBUF primitives (for the bus) selected and the Net view shows the net (connected to the INBUF/OUTBUF of the port) selected.

Similarly, when a user region is selected in the Region view, the selection is reflected in the Chip Canvas as well.

The Design View Window can be docked and undocked.

Find Window

The Chip Planner provides a Find window for each of the five design views to search for design elements. To open the Find Window, click the **Edit** menu and choose **Clone for Find**. You can also use the **CTRL- F** Hot Key. Multiple Find windows can be created for the same design view (Port/Logical/Net/Region/Block).

When the Find window opens, it is associated with a specific design view. Only design elements specific to the particular view are displayed. The view name (Port/Logical/Net/Region/Block) is displayed across the top of the window.

You can create multiple cloned Find windows for each view. Cloned Find windows are floating when they are opened and can be resized, moved, docked or undocked (floating).

When the Find window is invoked in the Logical view, for example, the find window opens with the name Find (Logical) across the top of the window and the name Find # (Logical) across the top of the window when there are multiple cloned Find windows for the same View.

By default, each cloned Find window is named sequentially as Find 1 (<view_name>), Find 2 (<view_name>), Find 3 (<view_name>) and so on. The cloned Find Windows can be renamed to a name different from the default.

A cloned Find Window has the same features and functionality as the main view window. In addition, a cloned Find Window has two extra icons:

- Rename Tree - Renames the cloned Find Window to a name different from the default name.
- Delete Tree - Deletes the cloned Find Window.

You may find multiple find windows useful in floorplanning. For example, If your design has both a RAM and a MACC block and you want to filter and select both and display them in the Chip Canvas, you need two Find windows for the logical view, one with the filter based on Macro type > RAM and the other with the filter based on Macro type > MACC.

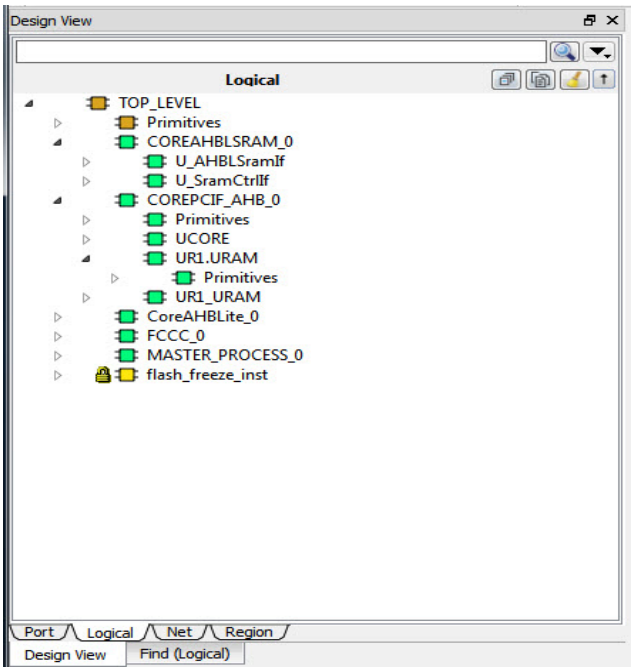


***Figure 1-2* • Find (Logical View)**

Search and Filter

For each of the five views (Port, Logical, Net, Region, and Block) the Search and Filter operations are available. Open first the Find windows and search for specific design elements. Click the Filter icon in the Design View window or any cloned Find windows to search and filter the display. Three types of searches are available:

- Wildcard Filter- such as “*” or “?” in the filter for wildcard matching. For example, when you enter FDDR* in the filter, the FDDR component and all its lower level primitives are displayed.
- Use Regular Match Filter
- Regular Expressions - posix case insensitive regular expression search. For details on the syntax, refer to http://www.boost.org/doc/libs/1_43_0/libs/regex/doc/html/boost_regex/syntax/basic_extended.html

Note: All Filtering is case-insensitive.

Port View

The Port View displays a hierarchical view all the Input, Output, and Inout ports of the design. Regular I/Os and Dedicated I/Os are displayed:

- Regular I/O ports - Input/Output/Inout ports that can be changed or reassigned by the user. These are shown under the **I/O Ports** tree.

- Dedicated I/Os - Special-purpose I/Os that cannot be changed or reassigned by the user. These are shown under **the Dedicated Ports** tree. Examples are SERDES I/Os and UJTAG dedicated ports

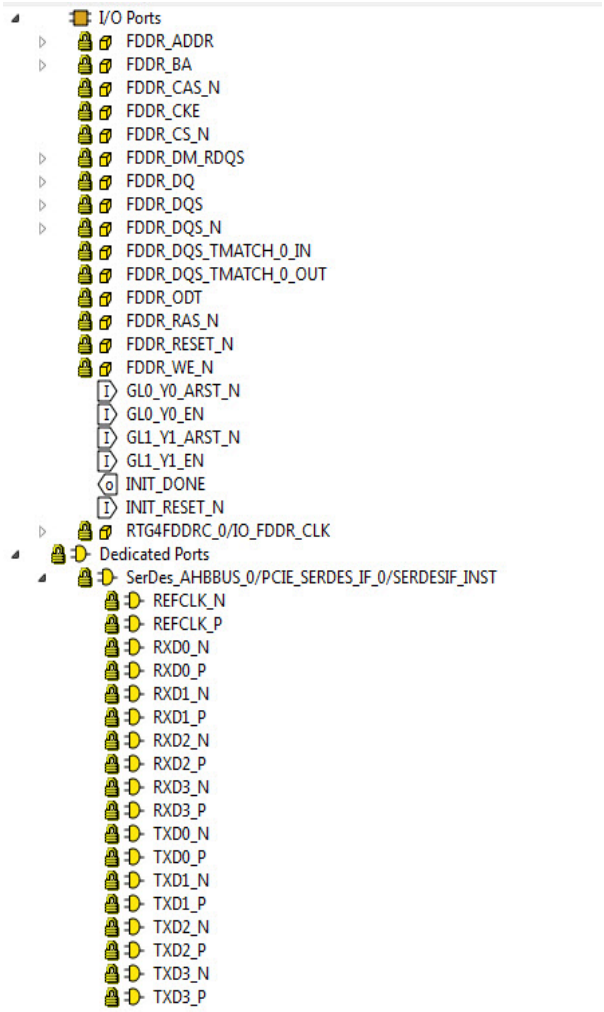


***Figure 1-3* • Port View**

Port Buses

Scalar members of a bus port are grouped under the bus. All bus ports can be collapsed or expanded.

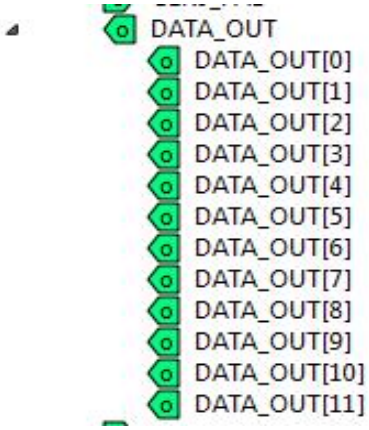


***Figure 1-4* • Bus Port DATA_OUT and its scalar members**

Port Properties

To see the properties of the port, click to select the port. The properties of the port you selected is displayed in the "Properties Window". The selected port is also highlighted in the Chip Canvas and the World View.

User Actions in Port View

In the Port View, you can:

- Assign ports to locations - Select a port and drag and drop the port into the Chip Canvas at a valid resource location to assign the element to that location. All valid port locations are highlighted when you drag the selected element into the Chip Canvas.
- Unassign ports from locations - Right-click the port and select **Unassign From Location** to unassign a port.
- Lock Port to location - Right-click the port and select **Lock Placement** to lock selected port to the assigned location. This option is enabled only when the port is already placed in a location.
- Unlock Port from location - Right-click the port and select **Unlock Placement** to unassign the port. This option is enabled only when the port is already locked to a location.
- Assign Port to Region - Right-click the port and select **Assign Macro to Region** to assign a port macro to a region. This option is enabled only if there is a valid region (inclusive or exclusive) created over the I/O port location.
- Unassign Port from Region - Right-click the port and select **Unassign Macro to Region** to un-assign a port macro from a region. This option is enabled only if the port is already assigned to a region.

Sorting

Click the sort icon  to sort the Ports in ascending or descending order, the type, and the state of the ports.

Port Filtering

Either the traditional match filter or Regular Expression match filter is available. Enter a port name in the Filter text box to filter Ports. Enable the **Use RegEx** checkbox to use Regular Expression match filtering.

Filter According to Port Types

The Port Filter list varies with the family and die. See “Family-specific Macros/Nets/Ports” on page 64 for details.

Filter According to Port States

Port States filtering includes:

- Placeable - All I/O that can be placed by the user.
- Unplaceable - All I/O that cannot be placed by the user, example: dedicated I/O.
- Assigned to location- All I/O that can be assigned to a location.
- Not assigned to location - All I/O that cannot be assigned to a location.
- Assigned to region - All I/O that can be assigned to a region.
- Not assigned to region - All I/O that cannot be assigned to a region.
- Locked - All I/O that are locked.
- Unlocked - All I/O that are not locked.

Table 1-5 lists the icons and the functions of the ports in the Port View.

Table 1-5 • **Ports and Icons**

Icon	Name	Function
	Input Port	Represents an Input Port.
	Output Port	Represents an Output port.
	Bidirectional Port	Represents a Bi-Directional port.
	White Background	Represents a port that is not placed.
	Green Background	Represents a port that is placed.
	Blue Tick Mark	Represents an I/O that has been assigned to a region.
	Lock Icon	Represent an I/O that is fixed/ locked to a location.

Logical View

The logical view is accessible from the Logical tab of the Design View window.

It displays a hierarchical view of all the logic inside the chip. The displayed Logic levels are:

- Component - Displays the logic at the component level, such as FDDR/CCC/Soft IP cores/ SERDES, etc. This represents the hierarchy in the design.
- Primitives - Displays the lowest level of the hierarchy (hard macro level).You can expand the hierarchy tree to see the lower level logic.

Logic Element Properties

Click the component/primitive to find out the properties of the logic element you have selected. The properties of the component/primitive are displayed in the "Properties Window". The selected design element is also highlighted in the Chip Canvas and in the World Vew.

User Action in Logical View

Select a design element to:

- Assign elements to locations - Right-click a design element and select **Assign to Location** to assign the element to that location. All valid resource locations are highlighted in the Chip Canvas when you drag the selected element into the Chip Canvas. Only a single element can be assigned at a time.
- Unassign element from location - Right-click a design element and select **Unassign from Location.** You can select multiple design elements/components and unassign them.
- Lock element to location - Right-click a design element and select **Lock Placement** to lock the selected element to an assigned location. This option is enabled only when the element is already placed in a location. You can select multiple design elements/components and lock them.
- Unlock element from location - Right-click a design element and select **Unlock Placement** to unlock or unfix a design element that is already locked to a location. This option is enabled when the element is already locked to a location. You can select multiple design elements/components and unlock them.
- Assign element to Region - Right-click a design element and select **Assign Macro to Region** to assign a macro to a region. This option is enabled only if there is a valid Region created over the required resource location. You can select multiple design elements/components and assign them to a region.
- You can also drag and drop the selected elements directly into a region in the Chip Canvas. If the selected elements are not compatible or over-booked for the desired region, the selection is not assigned to the region and invalid elements are shown in red in the Properties window.
- Unassign element from Region - Right-click a design element and select **Unassign Macro from Region** to unassign a design element/macro from a region. This option is enabled only if the element is already assigned to a region. You can select multiple design elements/components and unassign them from a region.

Filtering

Enter a macro name in the Filter text box to filter the design elements. From the pull-down menu of the Sort icon, choose either the traditional match filtering, wildcard filtering, or Regular Expression match filtering.

Sorting

Click the Sort Icon  to sort in ascending or descending order, the type (Filter by Macro Type), and state (Filter by State) of the logic element.

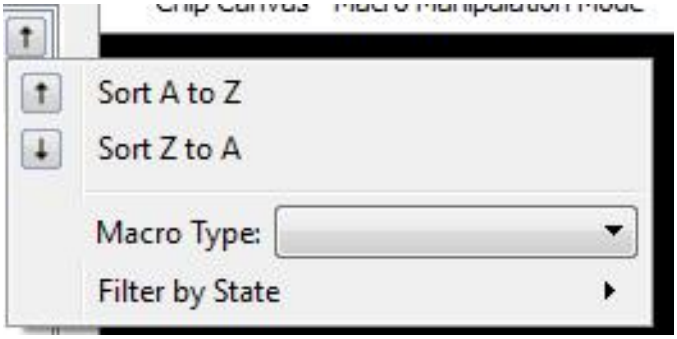


***Figure 1-5* • Macro Filter**

Filtering

Enter a macro name in the Filter text box to filter the design elements. From the pull-down menu of the Sort icon, choose either traditional match filtering, wildcard filtering, or Regular Expression match filtering.

According to Macro Types

Available Macro types are family/die-dependent. See Appendix A, "Cross-Probing from SmartTime to Chip View/Netlist View"for the list of Macro filters specific to the family/technology of your project.

According to Macro State

The Logical View displays the filter results based on the state of the Logical elements:

- Placeable - All Macro that can placed by the user. This option is mutually exclusive with the Unplaceable option.
- Unplaceable - All Macro that cannot be placed by the user. This option is mutually exclusive with the Placeable option.
- Assigned to Location - All Macro that can be assigned to a location. This option is mutually exclusive with the Not assigned to Location option.
- Not assigned to Location - All Macro that cannot be assigned to a location. This option is mutually exclusive with the Assigned to Location option.
- Assigned to Region - All Macro that can be assigned to a region. This option is mutually exclusive with the Not assigned to Region option.
- Not assigned to Region - All Macro that cannot be assigned to a region. This option is mutually exclusive with the Assigned to Region option.
- Locked - All Macro that are locked. This option is mutually exclusive with the Unlocked option.

- Unlocked - All Macro that are not locked. This option is mutually exclusive with the Locked option.

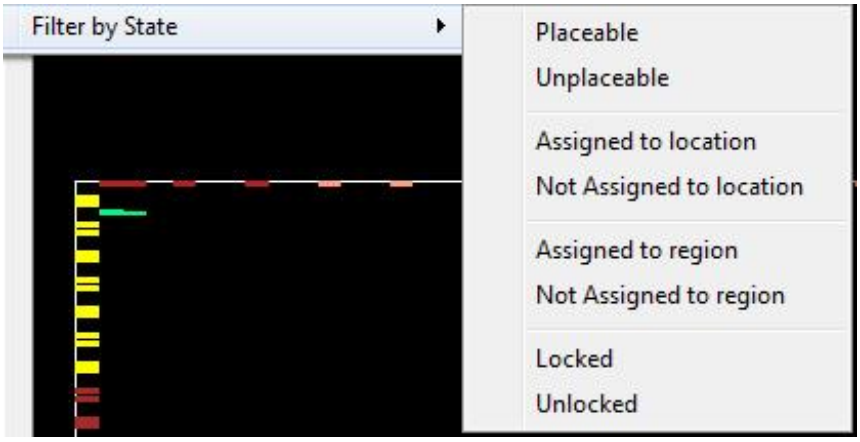


Figure 1-6 • **Macro State Filter**

Table 5 lists the Macros as displayed in the Logical View.

Table 1-6 • **Macros in Logical View**

Icon	Name	Function
	Component/Top Level Macro	Represents a Design Component or Top level macro that has a lower level macro.
	Comb/Seq Element	Represents the lowest level element associated with a fabric resource.
	Input Port Macro	Represents a macro associated with an Input port.
	Output port macro	Represents a macro associated with an output port.
	Bi-Directional port	Represents a macro associated with a Bi-Directional port.
	Global Resource	Represents a macro assigned to Global Resources/Row Global Resources.
	Block Element	Represents a design element associated with a block or an IP interface.
	White background	Represents a design element that is not placed.

***Table 1-6* • Macros in Logical View (continued)**

Icon	Name	Function
	Green background	Represents a design element that is placed.
	Blue tick mark	Represents a design element that has been assigned to a region.
	Lock Icon	Represents a design element that is fixed/locked to a location.

Net View

The Net View displays a flattened net view of the design and all the nets associated with the design. Shown with each net are the pins connected to the net.

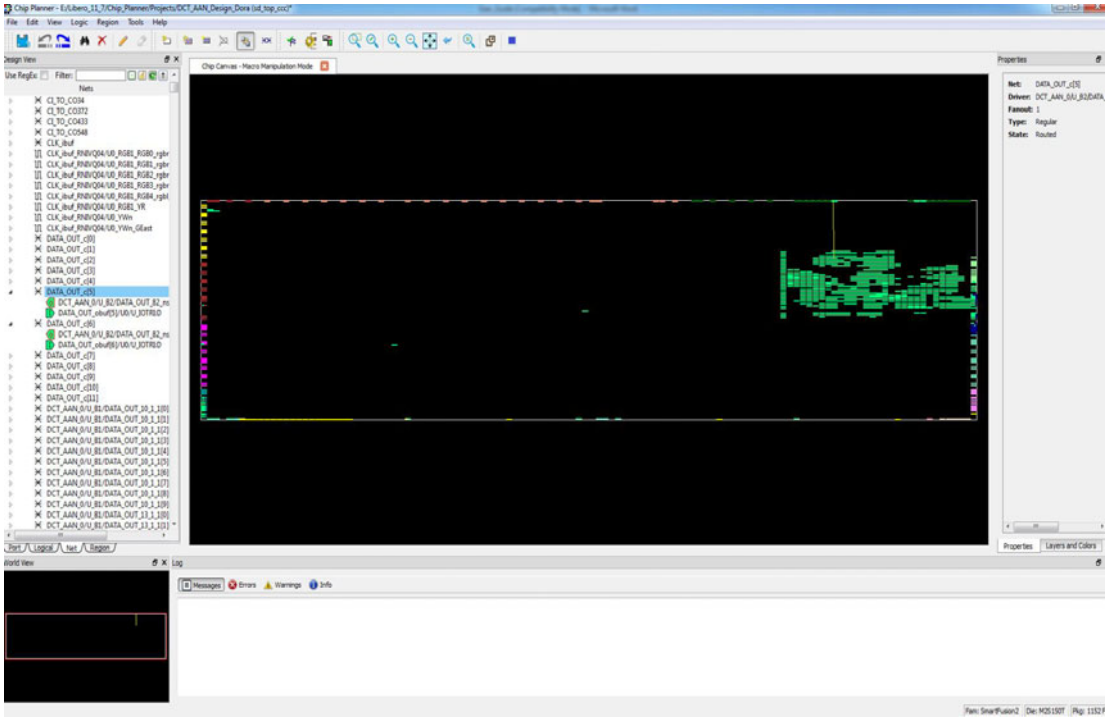


***Figure 1-7* • Net View**

Net Properties

Click to select the net and the net properties are displayed in the "Properties Window". The selected net is also highlighted in the Chip Canvas and the World View.

User Actions in Net View

From the Net view, you can:

- Change Net Color - Right-click a net and select **Net Color** to change the net color. This opens a color palette from which you can assign the desired color to the selected net.
- Assign net to Region - Right-click a net and select **Assign net to Region** to assign the driven macros associated to the net to the desired region. This option is enabled only if there is a valid Region created over the required resources. You can select multiple nets and assign them to a region.
- Assign net (with driver) to Region - Right-click a net and select **Assign net (with Driver) to Region** to assign all net macros including driver macros to a region. This option is enabled if there is a valid Region created over the required resources. You can select multiple nets and assign them to a region.
- Unassign net from Region - Right-click a net and select **Unassign net from Region** to unassign net macros from a region. This option is enabled only if the net is already assigned to a region. You can select multiple nets to unassign from a region.

Sorting

Sort the nets in ascending or descending order.

Filtering

Enter a net name in the Filter text box to filter net names. From the pull-down menu of the Sort icon, choose either traditional match filtering, wildcard filtering, or Regular Expression match filtering. You can also filter with criteria specific to nets, such as fanout values, net types, and routing status (routed or unrouted).

Filter Criteria based on fanout value

- Max Fanout - Enter a value to display nets with a maximum fanout value.
- Min Fanout - Enter a value to display nets with a minimum fanout value.

Note: Max Fanout and Min Fanout are logical ANDed together. If the Max Fanout has a value of 10 and the Min Fanout has a value of 2, the Net view displays only nets which meet both conditions. In this case, only nets with a fanout range of 2 to 10 are displayed.

Filter Criteria based on net type

The net type and the filter list is family/die-specific. See Appendix A, "Cross-Probing from SmartTime to Chip View/Netlist View" for the list of net filters specific to the family/technology of your project.

Filter Criteria based on routing status

- Routed - Displays all routed nets
- Unrouted - Displays all unrouted nets

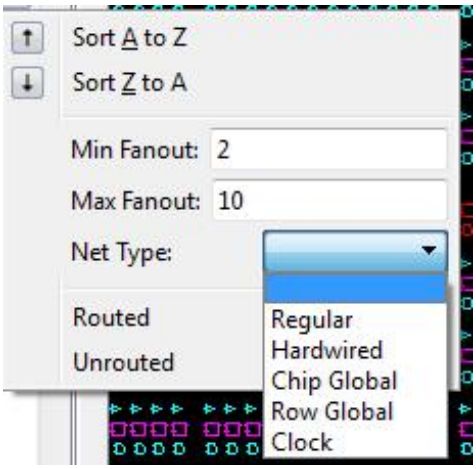


***Figure 1-8* • Net Filter Options**

Table 1-7 lists the icons specific to the net view.

***Table 1-7* • List of Net Icons**

Icon	Name	Function
	Regular/Hardwired Net	Represents a regular or hardwired net.
	Global Net	Represents a net that is routed through Chip Global/ Row global resources.
	Driven Macros	Represents a list of macros that are driven by this net.
	Driver macros	Represents a macro that is driving this net.
	Blue tick mark	Represents a net that has been assigned to a region.

Global Nets

A global net is a net that uses Global routing resources for routing a signal from source to destination logic clusters. These include Chip Globals Resources/Global Buffers (GB), Row global resources/row global buffers (RGB), and Half-Chip Globals (HGB for RTG4). Clocks, Async Reset, and nets with high fanout are typically routed through these global routing resources. Global signals (G[n:0]) reach the logic clusters through row global signals (RG[7:0]) generated by an associated row global buffer (RGB). RGB are inferred by the layout tool and depending on the placement of the design elements, it distributes the fanout of the global nets across multiple RGBs. The Net View shows this break-up for such global nets.

An example of a Global Net routed through GB[0] with a fanout of 2968 is shown in the Properties window below.

Global Nets Information

	From	GB Location	Net Name	Fanout
1	GB[0]	(290, 72)	CLK_ibuf_RNIVQ04/U0_YWn	2968
2	GB[12]	(306, 72)	RST_ibuf_RNIUR47/U0_YWn	512

***Figure 1-9* • Global Net Information in Properties Window**

The Chip Canvas View of the Global Net is shown in Figure 1-10.

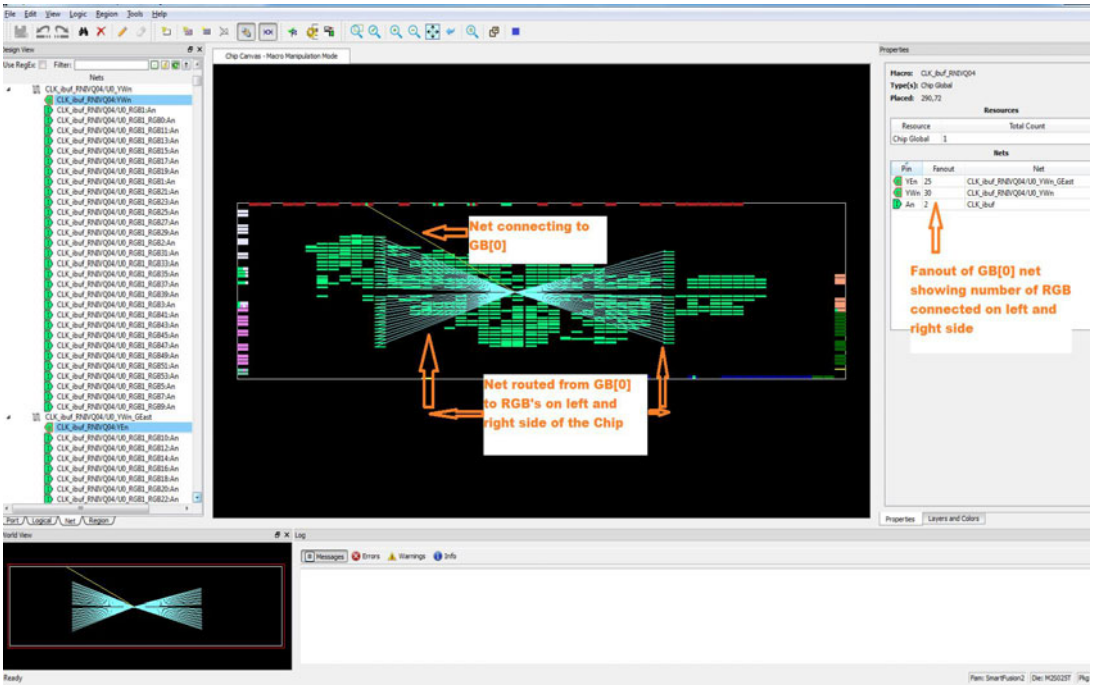


***Figure 1-10* • Chip Planner View of Global Net Routed Through GB[0]**

Region View

The Region View displays the regions you have created and all Components, Macros, and Nets assigned to the region. When you create a region, by default the region is named UserRegion1, UserRegion2, and so on. When you make a selection in the Region View, the properties of the Region you select are displayed in the "Properties Window". When you select an item in the hierarchical tree display, all sub-items are selected.

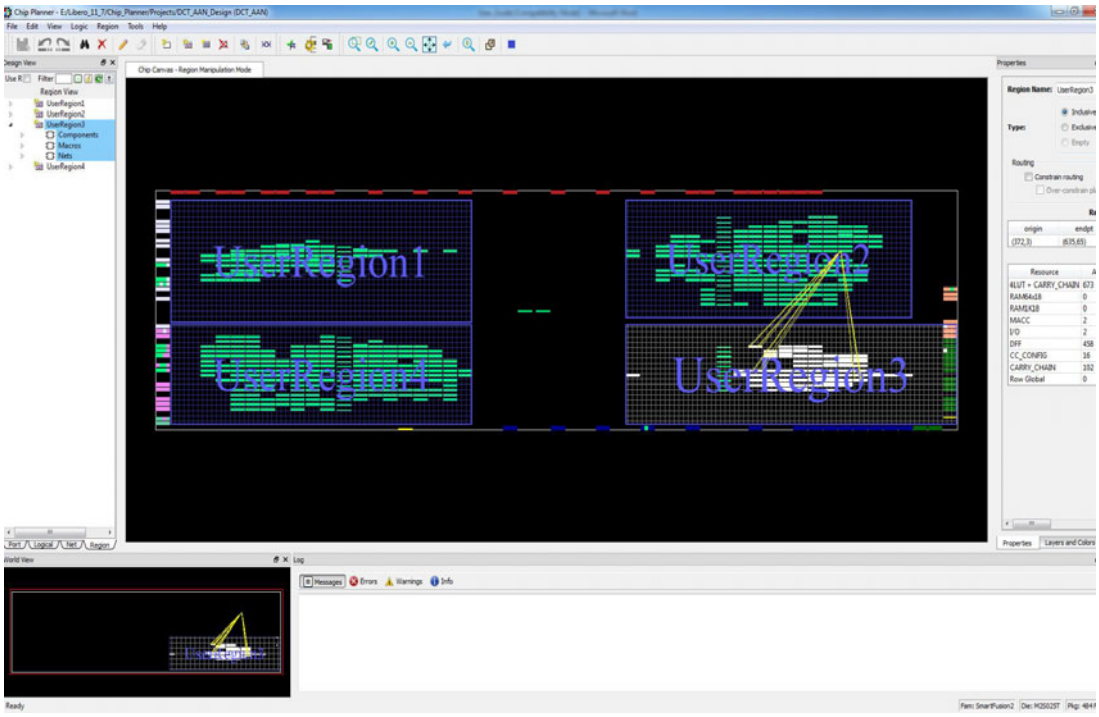


***Figure 1-11* • Region View**

User Regions and Region Types

Three types of regions are available for creation:

- "Inclusive Region"
- "Exclusive Region"
- "Empty Region"

User Actions on Regions in Chip Canvas

You can select a region in the Regions View to:

- Delete - Deletes a selected region.
- Clone - Clones a selected region.
- Rename - Renames a selected region.
- Merge - Merges two or more regions. This option is enabled if there are more than two regions selected.
- Assign macros inside Region - Assigns macros that are part of a region area assigned to the selected region.
- Unassign From location - Unassigns all design elements that are part of a selected region from their placed locations.
- Lock Placement - Locks all macros that are part of a selected region.
- Unlock Placement - Unlocks all macros that are part of a selected region.
- Unassign macros from Region - Unassigns assigned macros from a selected region.
- Unassign Component from Region - Unassigns assigned components from a selected region.
- Unassign Net from Region - Unassigns assigned nets from a selected region.

Region Properties

Click the region in the Region View and the properties of the region you have selected are displayed in the "Properties Window". The selected region is also highlighted in the Chip Canvas and the World View.

Region Filtering

Enter a region name in the Filter text box. From the pull-down menu of the Sort icon, choose traditional match filtering, wildcard filtering, or Regular Expression match filtering.

Region Sorting

In addition to ascending or descending order display, a filter is available for the Region View to display user regions based on region types:

- Inclusive - shows all inclusive regions
- Exclusive - shows all exclusive regions
- Empty - shows all empty regions

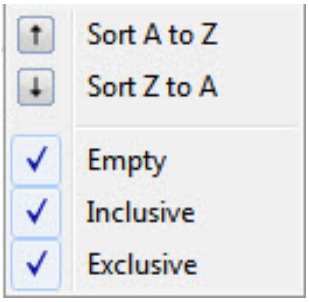


***Figure 1-12* • Region Filter**

The table below lists Region View icons.

***Table 1-8* • Region View Icons**

Icon	Name	Function
	Inclusive	Represents an inclusive region.
	Exclusive Region	Represents an exclusive region.
	Empty Region	Represents an Empty region.
	Nets	Represents a net associated with a region.

Table 1-8 • **Region View Icons (continued)**

Icon	Name	Function
	Component / Top Level Macro	Represents a Design Component or Top level macro that have lower level macros.
	Comb / Seq Element	Represents the lowest level element associated with a fabric resource.
	Output port macro	Represents a macro associated with an output port.
	Input Port Macro	Represents a macro associated with an Input port.
	Green background	Represents a design element that is placed.
	Blue tick mark	Represents a design element that has been assigned to a region.
	Lock Icon	Represents a design element that is fixed/locked to a location.

Block View

The block view displays the low-level design blocks (*.cxz files) you have imported into the Libero SoC project. This tab appears only if and when design blocks exist in the project. These low-level design blocks may have completed the place-and-route step and met the timing and power requirements of the design block. For details, refer to the Block Flow User Guide (**Help > Reference Manuals**).

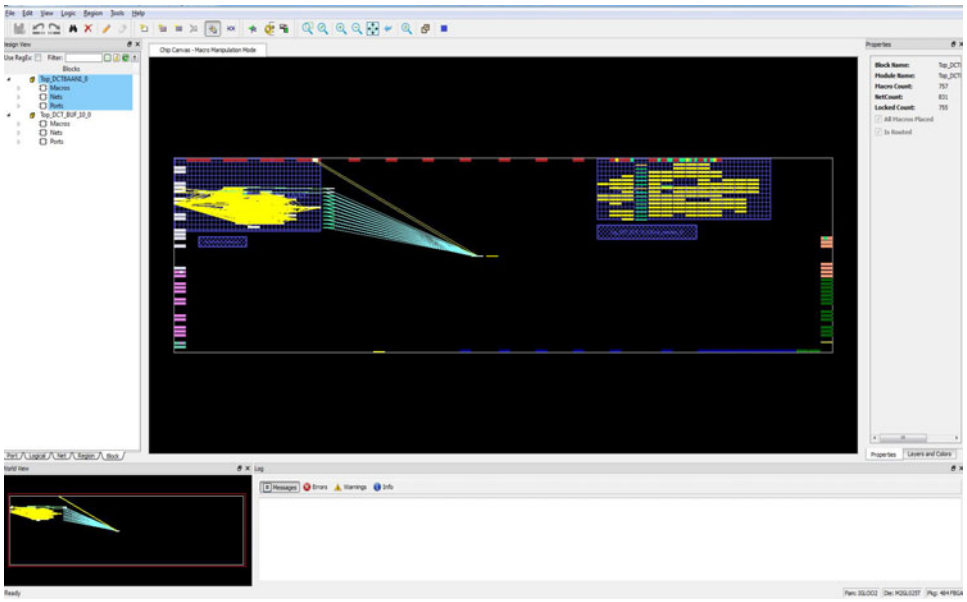


***Figure 1-13* • Block View Example – SmartFusion2, IGLOO2, RTG4**

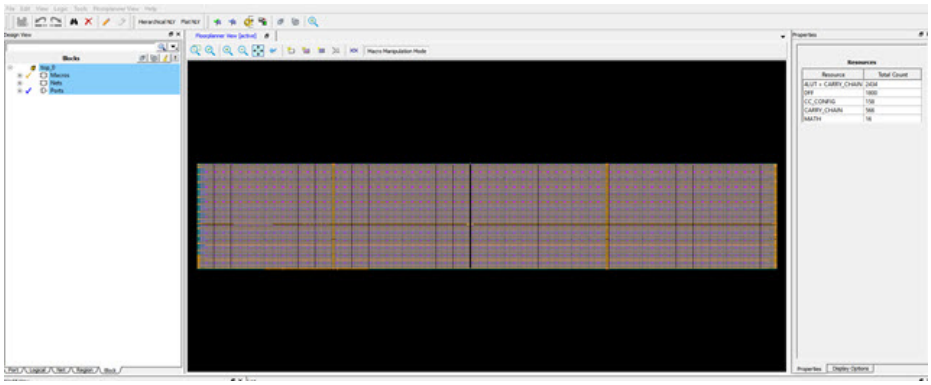


***Figure 1-14* • Block View Example – PolarFire**

The Block View displays all the design blocks in the project and displays the following design elements for each design block:

- Macros
- Nets
- Ports

Block Properties

Click to select the block in the Block View and the properties of the block are displayed in the "Properties Window". The selected block is also highlighted in Chip Canvas and the World View.

Block Filtering

Enter a block name in the Filter text box to filter blocks. From the pull-down menu of the Sort icon, choose traditional regular match filtering, wildcard filtering or regular expression match filtering.

You can sort the blocks in ascending or descending order.

Properties Window

The Properties window displays the properties of the design elements. What is displayed in the Properties window is dependent on what is selected in the design view.

Properties of Logical View Elements

The Properties window displays the properties of a component or macro when it is selected in the Logical View. Properties displayed may include the following, depending on the type of design elements:

- Macro/Component Name - Full Macro or component name based on selection in logical view.
- Cell Type - Resource type based on design element selection.
- Placed (Location) - X-Y coordinates where device element is placed.
- Resource Usage Table - A table showing resources based on component and macro selection.
- Region Attached Table - A table showing region to which selected macro/component is assigned.
- User region (if any) it is attached to.
- Nets Table - A table showing pins and nets which is associated with the selected macro along with fanout value.
- Locked/Unlocked (Placement) - The selected port is locked or unlocked.
- Port - Port name to which the I/O macro is assigned (only shown for I/O port macros).
- I/O Technology Standard - I/O Technology which is associated with the selected I/O macro (only shown for I/O port macros).
- I/O Bank- I/O bank to which the selected I/O macro is assigned (only shown for I/O port macros).
- Pin (Package Pin) - Pin to which the macro is assigned (only shown for I/O port macros).

Note: Not all properties in the list are displayed. The list of displayed properties varies with the type of design element selected in the Logical View.

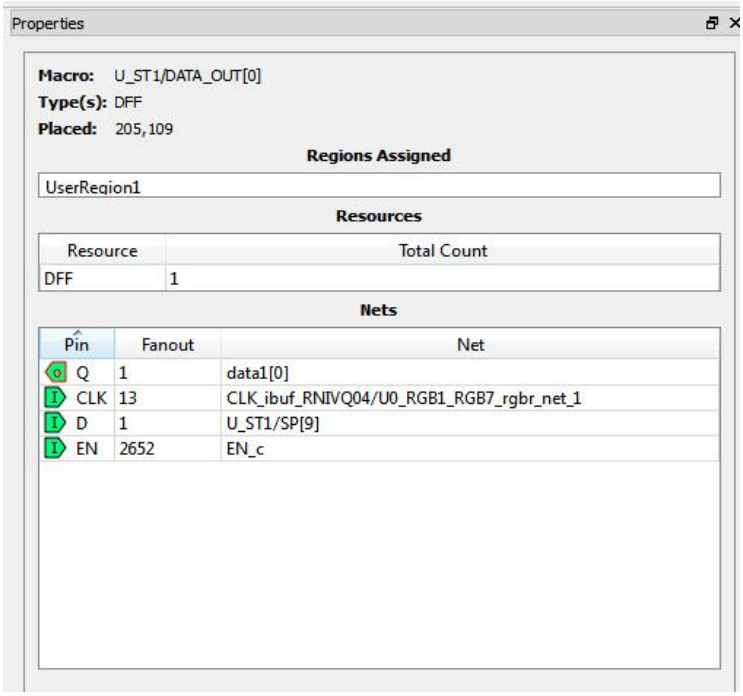


***Figure 1-15* • Example of Properties Window (Logical View)**

Properties of Port View Elements

When a design element (I/O Bus or Scalar I/O) is selected in the Port View, the Properties window displays the properties of a bus (for I/O bus) or a macro (for scalar I/Os)

For an I/O bus, the Properties window displays:

- Resource Usage Table - Shows all resources associated with the selection.
- Ports Table: Displays a table with I/O Bank, I/O Technology Standard, Package Pin, and Port Names of each individual member of the bus.

For scalar I/O ports, the Properties window displays the Macro information:

- Port Name - Full Name of the selected port.
- Macro - Name of the macro associated with the selected port.
- Port Type of selected I/O.
- Locked/Unlocked (Placement) - Selected port is locked or unlocked.
- Pin (Package Pin name) - Pin name to which selected port is assigned.
- I/O Technology Standard - I/O standard that is associated with the port.
- I/O Bank - I/O Bank associated with the selected port.
- Resource Usage table.

- Nets Table - A table showing pins and nets associated with the selected port along with fanout value.

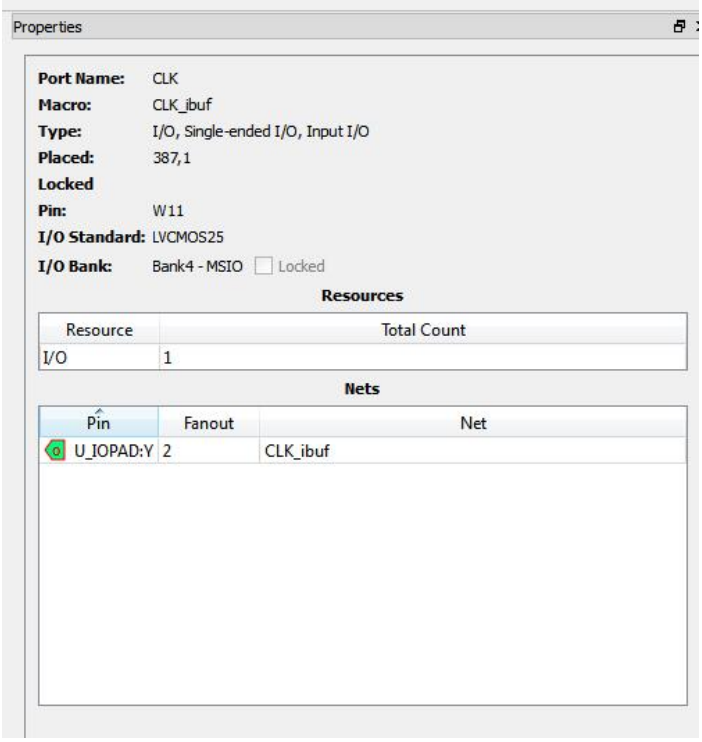


***Figure 1-16* • Example of Properties Window (Ports View)**

Properties of Nets

For nets selected in the Net view, the Properties window displays the following:

- Net Name - Full name of the selected net.
- Driver Name - Macro that is driving the selected net.
- Fanout - Fanout value of the selected net.
- Type of Net: Regular/Hardwired/Global for the selected net.
- State: Routed or Unrouted net

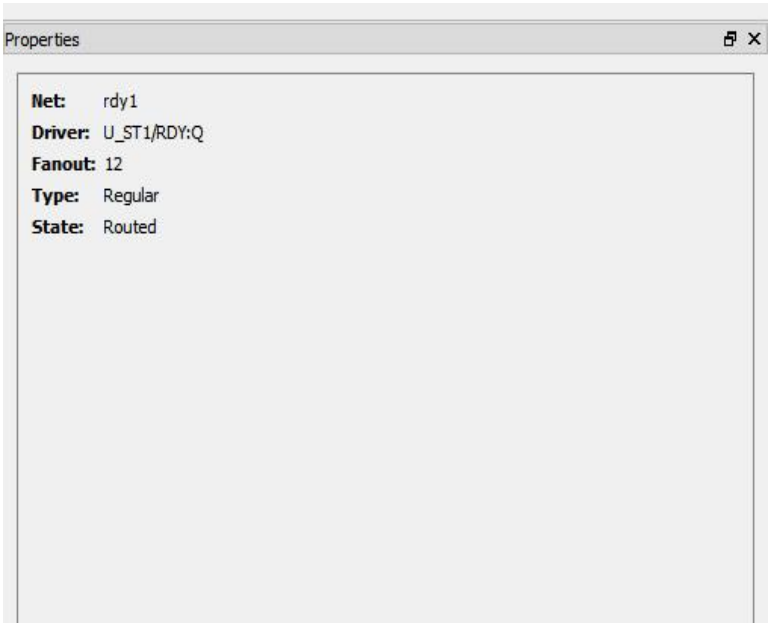


***Figure 1-17* • Example of Properties Window (Net)**

Properties of Region

Region properties are displayed in the Properties window when a user region is selected in the Chip Canvas or in the Region View.

The properties window for a region displays the following:

- Region Name - By default, the regions are named UserRegion1, UserRegion2, and so on when first created. You can change the region name by editing the Region name text box in the Properties window.
- Type of Region (Inclusive/Exclusive/Empty)
- Routing Requirements
  - Constrain routing - Instructs the Place and Route tool to apply routing restrictions (in addition to Placement restrictions) to the user regions. Refer to Figure 1-18 • Example of Properties Window (Region) for details.
- Region Extents - Displays the X-Y coordinates of the origin (lower left corner) and the endpoint (upper right corner) and the width and height of the region.
- Resources in the Region - Displays the logic resources in the region, including used (Assigned) resources and total available resources (Capacity) and a percentage of used resources (Assigned) relative to the total resources (Capacity). A percentage greater than 100 indicates resource overbooking, which is not allowed. The overbooked resource is highlighted in red.

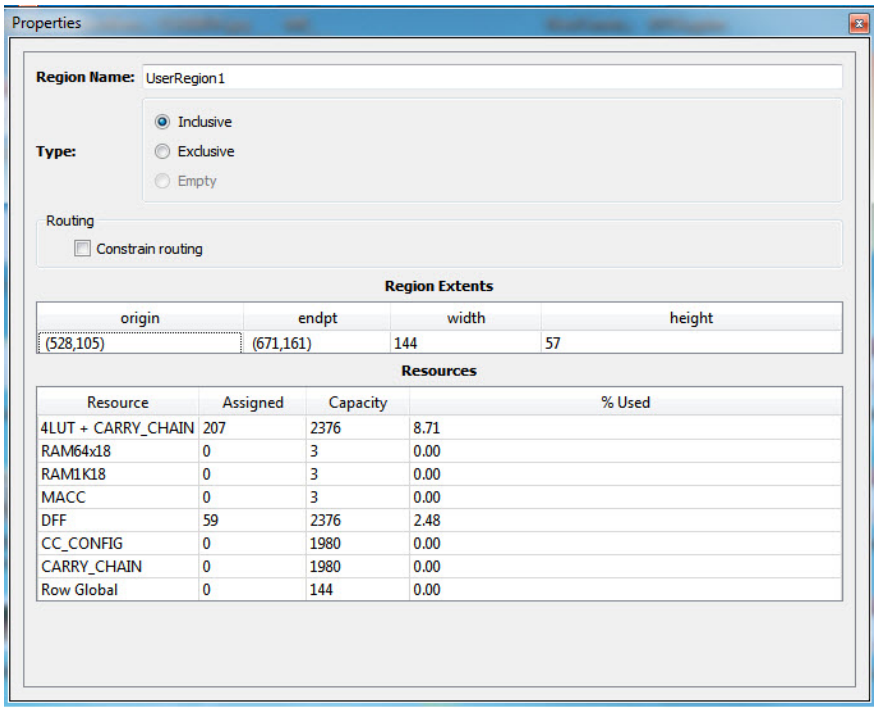


***Figure 1-18* • Example of Properties Window (Region)**

Properties of Blocks

When a block is selected in the Block View, the Properties window displays:

- Block Name - Name of the selected block.
- Module Name - Name of the block module.
- Macro Count - Total number of macros in the block.
- Net Count - Total number of nets in the block.
- Locked Count - Total number of locked macros.

In addition, it specifies whether all the macros are placed and/or routed.

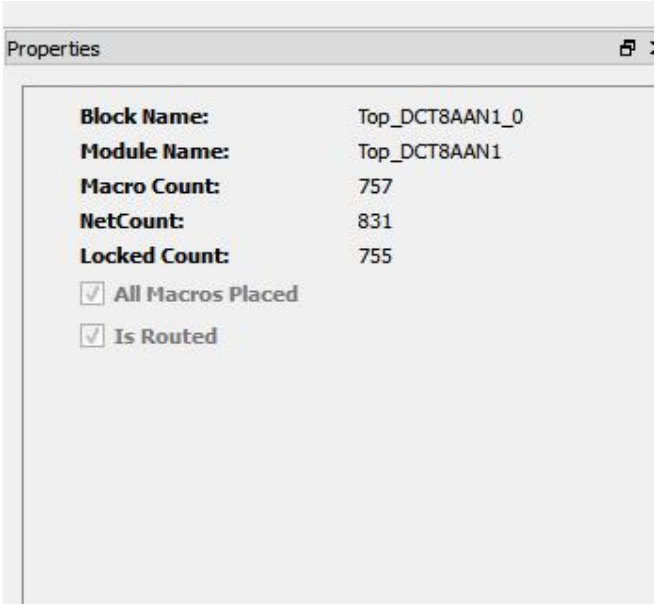


Figure 1-19 **• Properties of Block**

2 – Display Options Window

The Display Options Window allows you to customize the layout and the color settings for design elements on the Chip Canvas to meet your personal preferences.

There are two default layers and colors settings group that are provided with Chip Planner:

- System
- Pin_Planner (PolarFire only)
- Grey_Scale

By default, Chip Planner launches with “System” layers and colors settings group for the Device (Silicon feature) and the Design Elements. These are the System Default Settings.

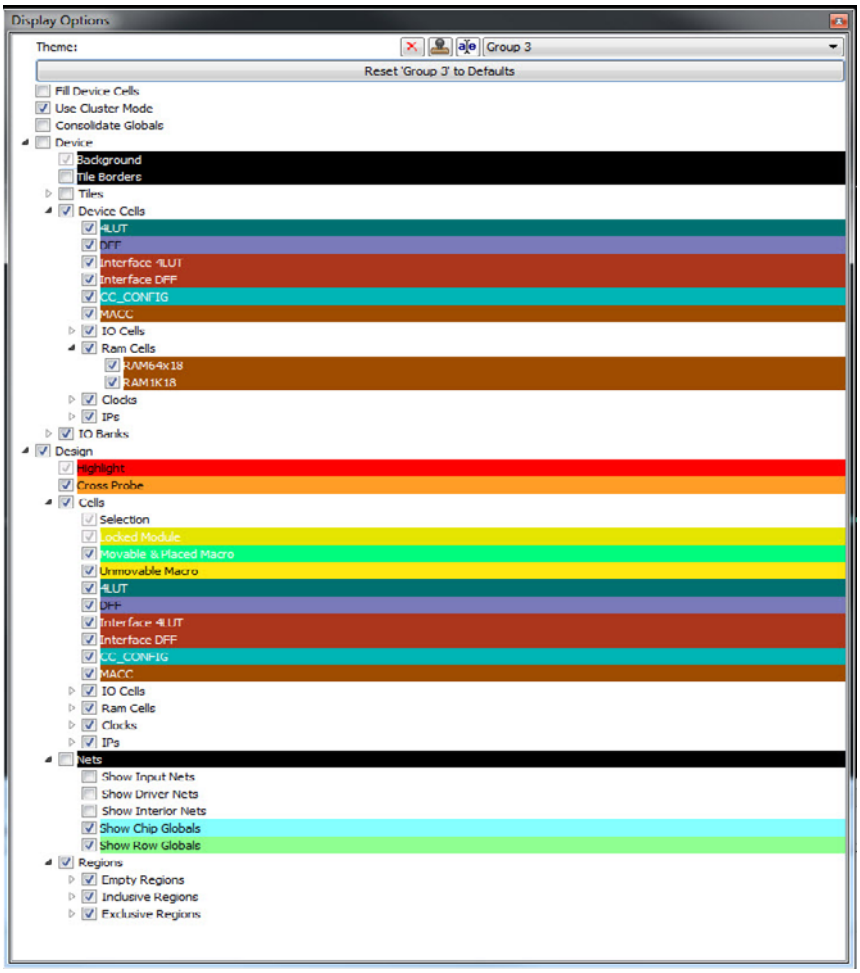


***Figure 2-1* • Default Color Setting for Device (Silicon Hardware) - Settings shown are for M2GL050 die**

.

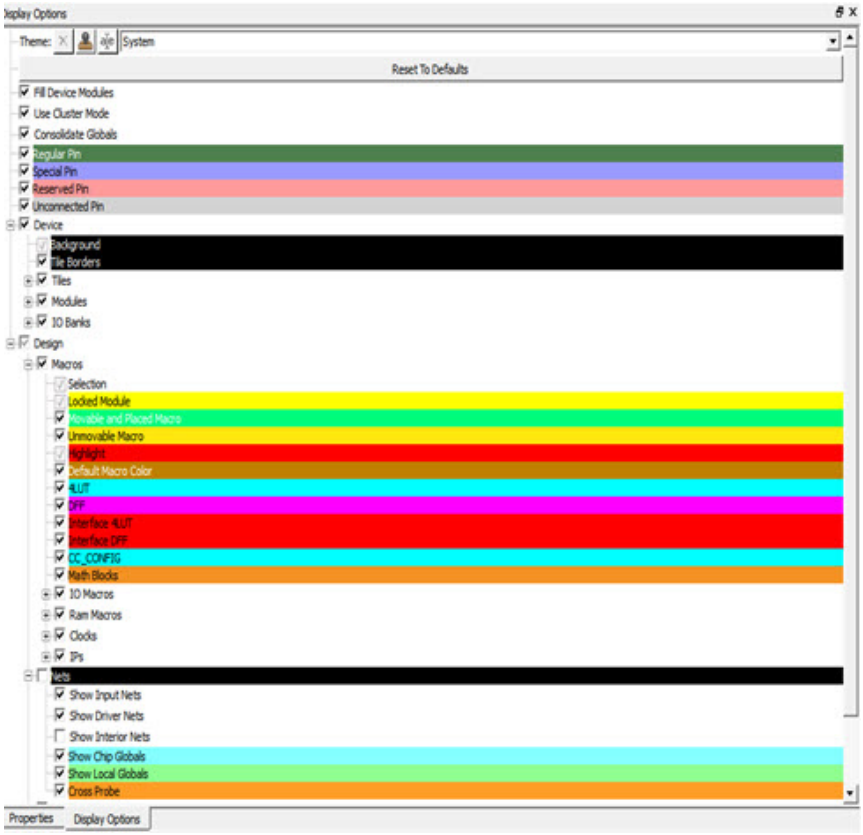


***Figure 2-2* • Default Color Setting for Device (Silicon Hardware) - Settings shown are for MPF300TS die (PolarFire)**

The device color setting is a hierarchical view. You may expand each group to see the lower level items and see the default color setting for each. The device cell types, IO banks are die-dependent and reflects the available hardware components for the selected die.

Similarly the color setting for the Design Elements are displayed in a hierarchical view. Expand the group to see the default color setting for each lower level design element.

Changing Color Settings

To change the color setting for a device or design element from the default setting:

1. Right-click the color for the element.
2. In the Set Color Dialog Box, move the Cross across the color spectrum to the color you prefer.

3. Click **OK**.

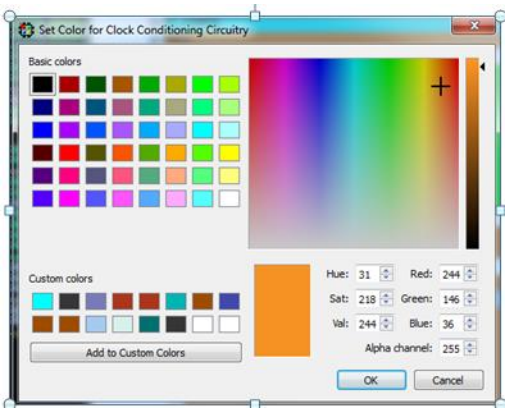


***Figure 2-3* • Set Color Dialog Box to Change Color**

Displaying an Instance on the Chip Canvas using the Display Options Window

You can use the checkbox provided against each menu item.to select the elements you want to see in Chip Canvas.

Some of the options in Display Options window cannot be unchecked, as these options are fixed for any design. Such options have checkboxes grayed-out and are always enabled. However you can still change the colors settings of these options

Design Option in Display Options windows can be grouped according to Macro Type and State of Macro. The display of design elements in Chip Canvas depends on both conditions met: the Macro Type and the State of macro. For example if you want to see 4LUT elements of your design, you need to select both Movable & Placed Macro and 4LUT options.

The table below lists the icons specific to the Display Options window.

***Table 2-1* • Display Options Icons**

Icon	Name	Function
	Rename Settings	Rename user created layers and colors settings from the default name to a name you specify
	Remove Settings	Remove the user defined Layers and colors settings.
	Clone Settings	Create a clone of current Layers and Colors Settings

Creating Personal Settings

You can create your display settings according to your preferences.

1. Create a clone from one of the selected settings (Grey Scale, Pin Planner – PolarFire only, System) using **Clone Setting** icon in the Layers and Colors/Display Options window.

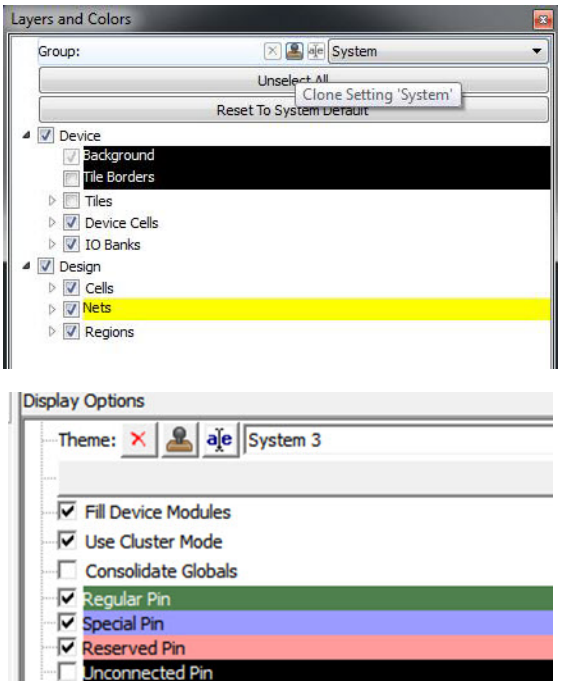


Figure 2-4 • **Clone Settings in Layers and Colors/Display Options Window**

2. Accept the default name “Group #” for the settings name or rename it from the Layers and Colors/Display Options window.
3. Change color settings and/or select items to be displayed from the Layers and Colors/Display Options window.

The customized settings can be created and preserved on your system and will always be available in the drop-down group list in the Layers and Colors/Display Options window. The customized settings are available to you across different projects on the same machine.

Removing Custom Setting Group

To delete the custom setting group, select the custom setting group and click **Remove Setting icon** in Display Options Window.

Note: The System setting is the default group and it cannot be removed. Only user-set custom settings can be removed.

Reset to System Default

Click **Reset <group_name> to Default** to reset the group’s settings to the system default settings.

Chip Display Options

The following options are available in the Display Options Window. They control the display in the Chip Canvas window:

Fill Device Cells

When this box is checked, the entire chip canvas is filled with all device modules at all view levels. Use this mode to see the display of all device resources on the chip. When this mode is not enabled (the default), only the devices used by the design are displayed.
Device cells which are shown are dependent on the Display Options settings for Device cells.

Use Cluster Mode

When this box is checked, the clusters (rather than the modules and macros inside the clusters) of the chip are displayed. This mode is useful when the Chip Canvas is zoomed out far enough to make the modules and macros too small to be visible. This mode significantly improves runtime performance, especially when displaying large device.The cluster will be displayed as used in the Chip Canvas if any module inside it is used.
When this mode is not enabled (the default), the Chip Canvas displays down to the macro and module level. This mode may incur runtime penalty, particularly on large devices.

Consolidate Globals

When this box is checked, the Row Globals (RGB) are hidden from the Chip Canvas view. Row globals (RGB) do not exist in the user netlist. They are buffers inserted by Libero SoC after layout. When this option is turned on, the Row Globals are removed from the display and the Chip Globals are shown as directly driving the macros and cells. This view makes it easier to determine the load of the Chip Globals. To do so, there is no need to track the load from the Chip Globals to the Row Globals and then to the macros and cells.

Design Elements in Display Options Window

The design elements displayed in the Display Options Window are family and die-dependent.

3 – Chip Canvas/Floorplanner View Window

The Chip Canvas/Floorplanner View window displays all design elements in one window. The selections you make in the views are reflected in the Chip Canvas window. The color scheme used in the canvas is dependent on the Layers and Colors you have selected in the Display Options window.

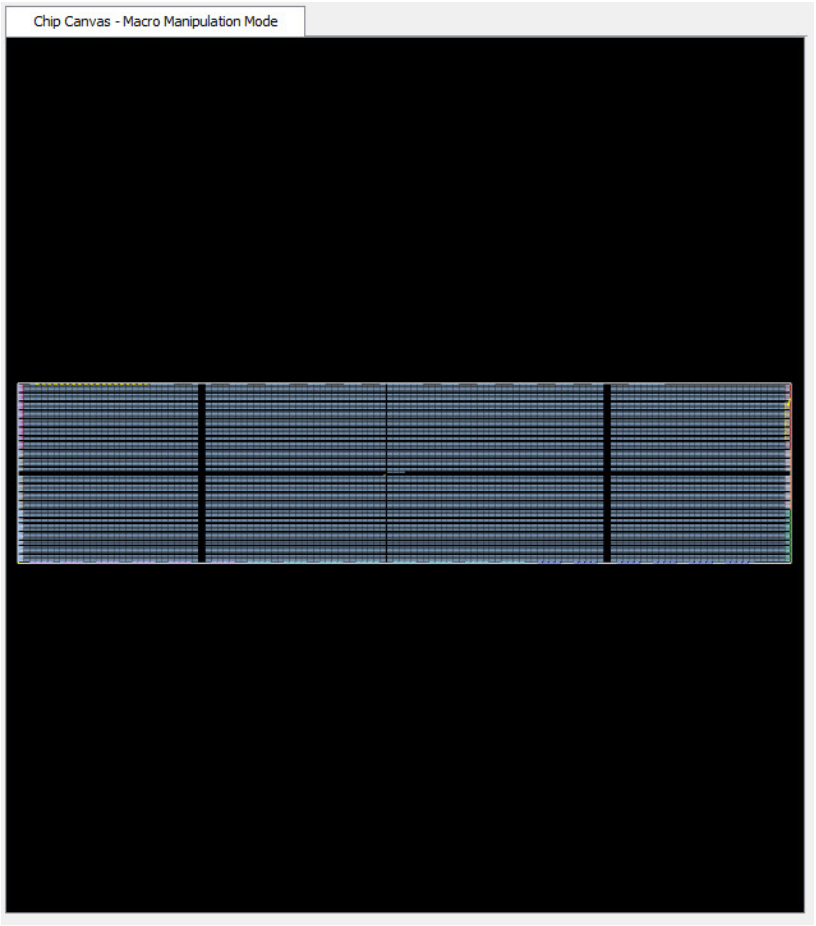


Figure 3-1 **• Chip Canvas**

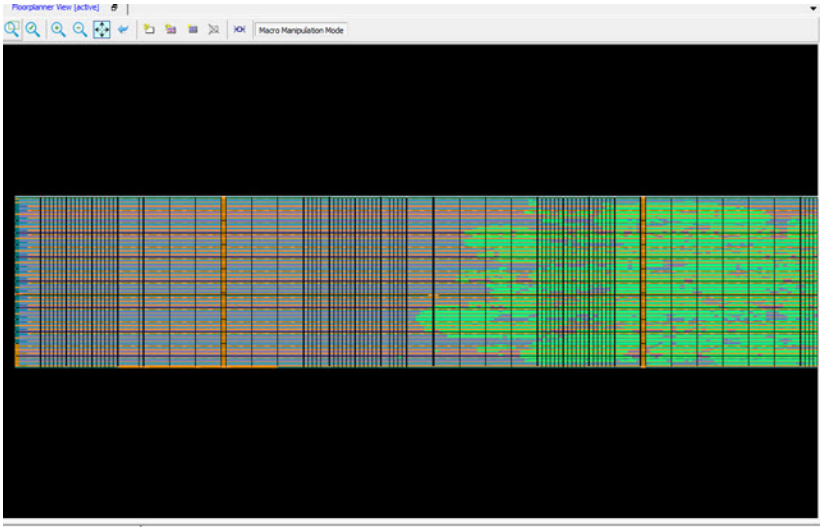


***Figure 3-2* • Floorplanner View (PolarFire)**

Operation Modes

The Chip Canvas has two modes of operation. Toggle the  button to switch between modes:

- Macro Manipulation Mode

  Use this mode to work with macros, such as assigning macros to location or unassigning placed macros from locations. You can also view properties of selected macros in the Chip Canvas from the properties window. You can select multiple macros from the Chip Canvas by pressing the <CTRL> key and selecting required macros in the Chip Canvas.

- Region Manipulation Mode

  Use this mode to work on regions such as resizing, renaming, or deleting regions, or assigning and unassigning macros or nets to regions.

Note: For PolarFire, click the Macro Manipu;lation Mode or Region Manipulation Mode button to switch modes.

Display Modes

The Display Options window configures the display of the window. Three display options are available.

- Fill Device Cells
- Use Cluster Mode
- Consolidate Globals

Icons

The icons available across the top of the Chip Canvas/Floorplanner View window allows you to zoom in, zoom out, assign I/O banks, runs DRC checks, create regions for placement.

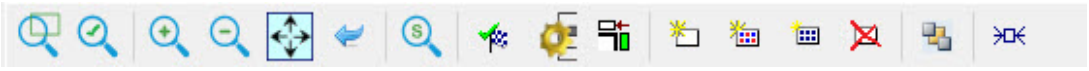


***Figure 3-3* • Chip Canvas/Floorplanner View Icons Across the Top of the Window**

These icons are also available as menu items under the ChipCanvas/Floorplanner Viesw menu

Table 3-1 lists the functions of the each icon.

Table 3-1 • **Icons**

Icon	Name	Function
	Rubber Band Zoom	Rubber Band Zoom - Drags out an area to enlarge/ zoom into.
	Rubber Band Select	Rubber Band Select an area to Zoom into. Click in the Chip Canvas/Floorplanner View and drag the mouse to delineate an area. Release the mouse and all macros inside the delineated area are selected. Works in the Macro Manipulation Mode.
	Zoom In	Zoom In to Chip Canvas/Floorplanner View.
	Zoom Out	Zoom Out of Chip Canvas/Floorplanner View.
	Zoom to Fit	Zoom to fit the Chip Canvas/Floorplanner View.
	Zoom to Location	Zoom to a Location Specified by X-Y co-ordinates.
	Zoom to fit Selection	Zoom to fit selected macros and ports. When enabled, the view attempts to center the view on the selected and placed ports.
	Check Design Rules	Run the Prelayout Checker, a preliminary check of the netlist for possible Place and Route issues.
	Check DRC Rules for Selected Interfaces Note: This option is available only for PolarFire.	Run the Prelayout Checker for the selected interface, a preliminary check of the netlist for possible Place and Route issues.
	I/O Bank Settings	Set the I/O bank to specific I/O Technology.

Icon	Name	Function
	Auto Assign I/O Bank	Run the Auto I/O Bank and Globals Assigner. Assigns a voltage to every I/O Bank that does not have a voltage assigned to it and if required, a VREF pin.
	Create Empty	Create an empty user region.
	Create Inclusive	Create an inclusive user region.
	Create Exclusive	Create an Exclusive user region.
	Delete Region	Delete user-created region you have selected.
	Region/Macro Toggle Switch – SmartFusion2, IGLOO2, and RTG4 only For PolarFire, use the Macro Manipulation Mode and Region Manipulation Mode buttons	Toggle this switch to select the Macro or the Region in the Chip Canvas. Use this switch when you are switching back and forth between Macro Manipulation Mode and Region Manipulation Mode. For PolarFire, click the Macro Manipulation Mode and Region Manipulation Mode buttons to switch modes.
	Show Nets For Macros	Show all nets connected to the Macro. There are usually too many nets attached to the macro. It is off by default.

Netlist Viewer in Chip Canvas Window

In addition to the chip view, the Chip Canvas window displays the netlist views. See “Netlist Views” on page 53 for details.

The Chip View (Floorplanner View in PolarFire) and the Netlist View each features a different set of icons specific to that view. There is also a ChipCanvas (Floorplanner View)/Netlist Viewer menu which toggles between Chip Canvas and Netlist View based on the view that is active at the time.See the following figures.

***Figure 3-4* • Chip Canvas Menu and Icons (SmartFusion2, IGLOO2, and RTG4)**

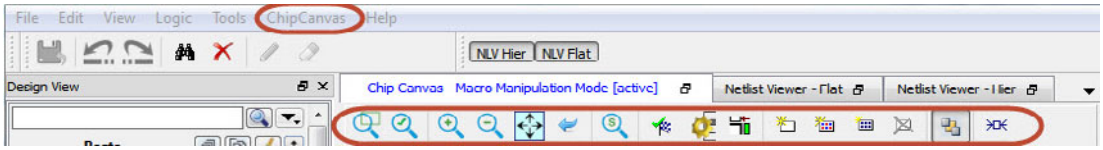
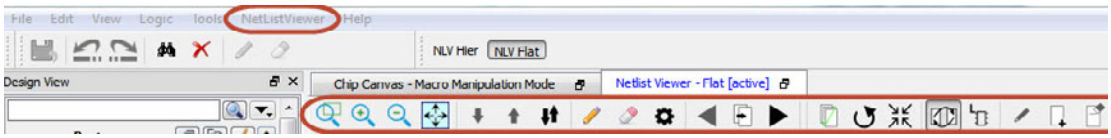


***Figure 3-5* • Netlist Viewer Menu and Icons (SmartFusion2, IGLOO2, and RTG4)**



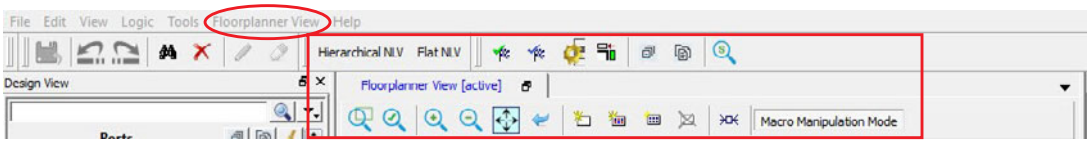


***Figure 3-6* • Floorplanner Menu and Icons (PolarFire)**

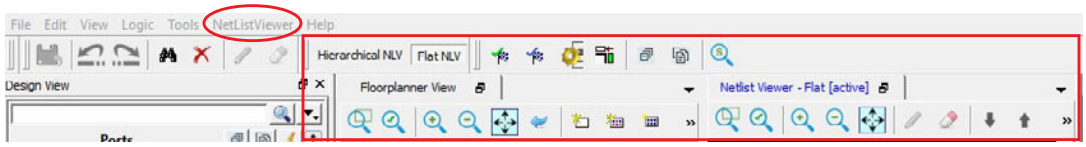


***Figure 3-7* • Netlist Viewer Menu and Icons (PolarFire)**

4 – Other Chip Planner Windows

World View Window

The World View shows a red rectangle which reflects what is visible in the Chip Canvas view in the context of the Chip. Changing what is visible in the canvas also changes the red rectangle. Changing the size or position of the red rectangle changes what is seen in the Chip Canvas.

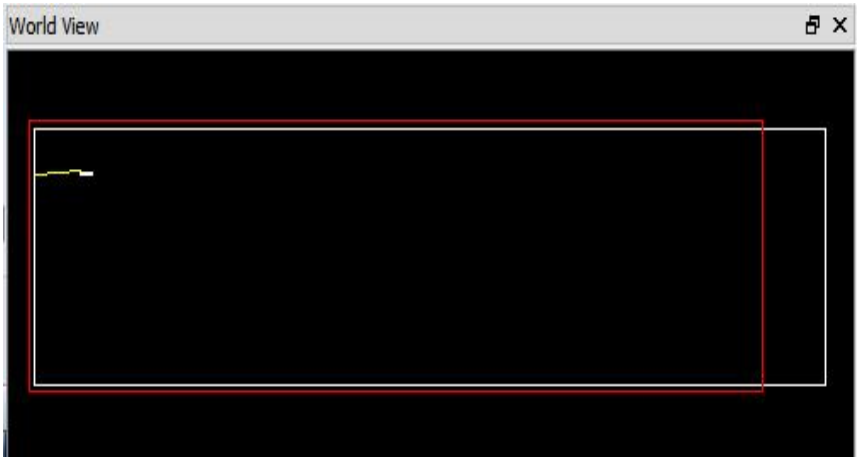


***Figure 4-1* • World View Window**

Log Window

The Log window displays all messages generated by Chip Planner. You can filter the messages according to the type of message: Error, Warning, and Info. If you have made and saved changes in Chip Planner, the Log Window displays the name and location of the PDC file(s) which have been edited/ updated to reflect the changes.

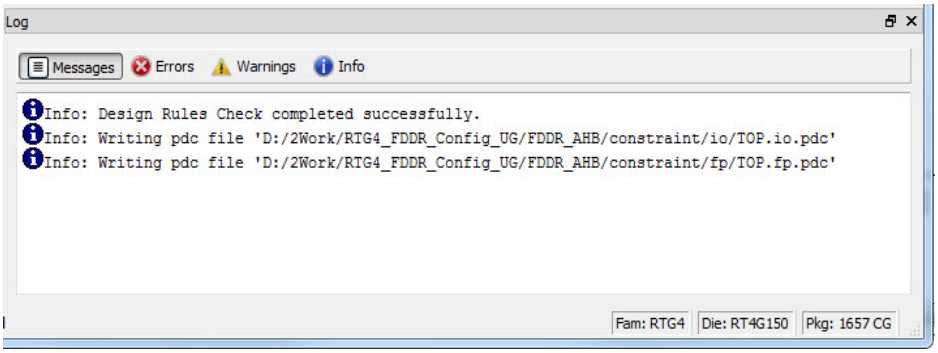


***Figure 4-2* • Log Window**

5 – Floorplanning Using Chip Planner

Floorplanning includes creating regions and making logic assignments to those regions. It is an optional methodology to improve the performance and routability of your design. The objective in floorplanning is to assign logic to specific regions on the chip to enhance performance and routability.

When floorplanning, you analyze your design to see if certain logic can be grouped within regions. Placement regions are especially useful for hierarchical designs with plenty of local connectivity within a block. If your timing analysis indicates several paths with negative slack, try grouping the logic included in these paths into their own regions. This forces the placement of logic within the path closer together and may improve timing performance of the design.

Use floorplanning to create Design Separation Regions for security-critical designs. For Microsemi's Design Separation Methodology, all logic should be contained in a logic placement region with dedicated place and route resources. Refer to Microsemi Design Separation Methodology for details.

Use Chip Planner before and after running layout to help you floorplan. You can:

- Create Regions
- Move, resize, merge, or delete regions
- Assign logic to region
- Assign nets to regions

Types of Regions

Three region types can be created for floorplanning purposes:

- Inclusive region
- Exclusive region
- Empty region

Inclusive Region

In an inclusive region, the Place-and-Route tool places unassigned logic within its boundary. It can contain macros, both assigned and unassigned to region. Routing resources within an inclusive region are also not restricted. Logic already placed there before region creation is not unplaced from the region.

Use the **create Inclusive Region** icon  to create an Inclusive region.

When a region rectangle is created, you can assign logic macros / net macros / port macros to it from the design view window.

You can also draw a region rectangle over placed macros and assign these macros to the region using the **Assign macros inside region** option by selecting the region rectangle in the Chip Canvas.

***Figure 5-1* • Inclusive Region Example**

Exclusive Region

In an exclusive region, the Place-and-Route tool does not place unassigned logic within its boundary. It can contain only macros already assigned to the region before the region is created. However, routing resources within an exclusive region are not restricted.

Use the **Create Exclusive Region** icon  to create an exclusive region.

When a region rectangle is created, you can assign logic macros / net macros / port macros to it from the design view window.

If an exclusive region rectangle is created over placed macros, the locked macros already inside the exclusive region will not be unplaced. They are automatically assigned to the region. If the macro is placed but not locked, the macros will be unplaced from the locations and will not be assigned to the exclusive region.

***Figure 5-2* • Exclusive Region Example**

Empty Region

In an empty region, neither the user nor the Place-and-Route tool can place any logic within its boundary. However, routing resources within an empty region can be used by the Place and Route tool.

Use the **Create Empty Region icon**  to create an empty region.

You cannot assign logic macros / net macros / port macros to an empty region.

If an empty region rectangle is created over placed macros which are not locked, the macros will be unplaced from the locations. The creation of an empty region over locked macros is not allowed.

***Figure 5-3* • Empty Region Example (SmartFusion2, IGLOO2, RTG4)**

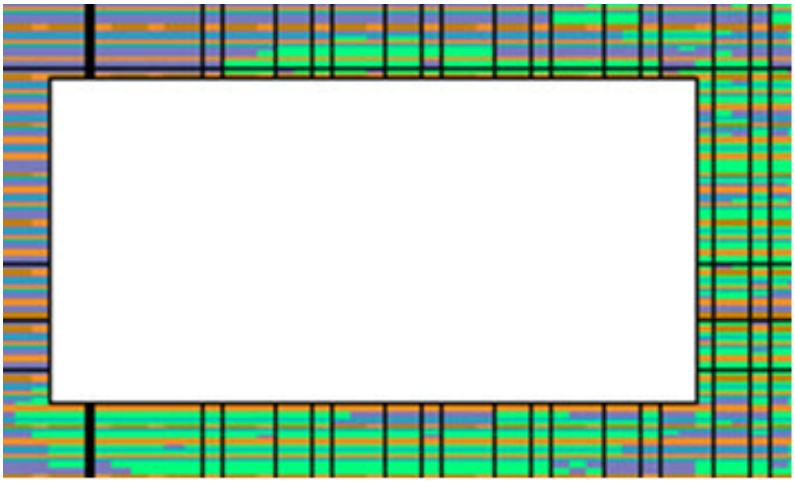


***Figure 5-4* • Empty Region Example (PolarFire)**

Creating Rectilinear Regions

To create a rectilinear region for floorplanning:

1. Click the region icon: Empty/Inclusive/Exclusive.
2. Go to the Chip Canvas and click at the location where you want to create a region.
3. Drag the mouse diagonally to draw a rectilinear shape for the size of the region you want. The region is named UserRegion1, 2, 3, and so on by default for Inclusive and Exclusive Regions, and EmptyRegion1, 2, 3, and so on by default for Empty Regions.

4. (Optional) Right-click and select **Rename** to rename the region from the default name to a different name.
5. Click **Commit** to save the changes.

Note: When a user region and its boundary falls on top of a cluster boundary, the tool extends the region to include the cluster in the region.

The Log window prints the message that PDC files are updated/written to reflect the changes you have made in Chip Planner.

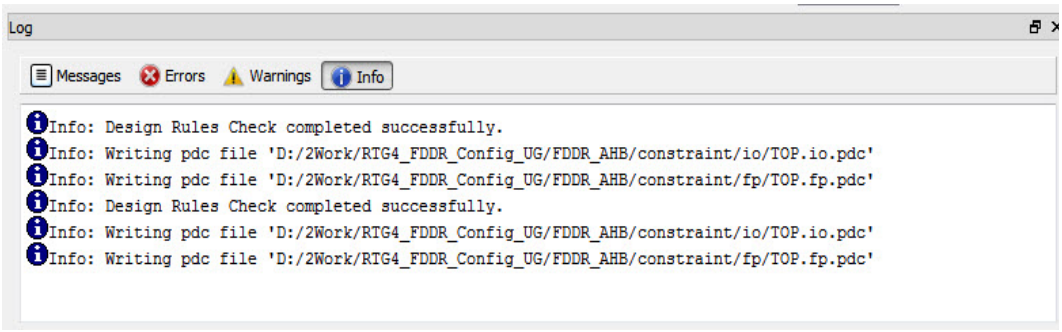


Figure 5-5 • **Log Window Messages**

The <proj_location>\constraint\<root>.fp.pdc is updated with the “define_region” PDC command to reflect the new user region you create.

```
define_region -name EmptyRegion3 -type empty -color 2143322112 648 225 659 227
define_region -name UserRegion1 -type inclusive -color 2147442270 552 300 731 311
```

For details about PDC commands, refer to the PDC Commands User’s Guide.

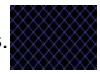
The "Properties Window" displays the properties of the region you have created.

Creating Non-Rectilinear Regions

By default, a region is created with a rectangular area. However, you can also create a non-rectilinear regions by merging two or more rectangular regions.

Note: Use inclusive or exclusive region constraints if you intend to assign logic to a region. An inclusive region constraint with no macros assigned to it has no effect. An exclusive region constraint with no macros assigned to it is equivalent to an empty region.

Note: A user region in which there are macros assigned to it is identified by a vertical and horizontal checkered-board pattern 

Note: A user region without any logic assigned to it is identified by a diagonal hash lines.  pattern.

Assigning Components/Macros to Regions

To assign Components or Macros to a user region:

1. Right-click the Component/Macro in the Logical View and select Assign Component/Macro to a UserRegion.
2. Click **Commit** to save the changes.

Alternatively, you can drag-drop the component/macro from the logical view onto a user region in the Chip Canvas.

The component/macro that has been assigned to the region is identified by a blue check mark  .

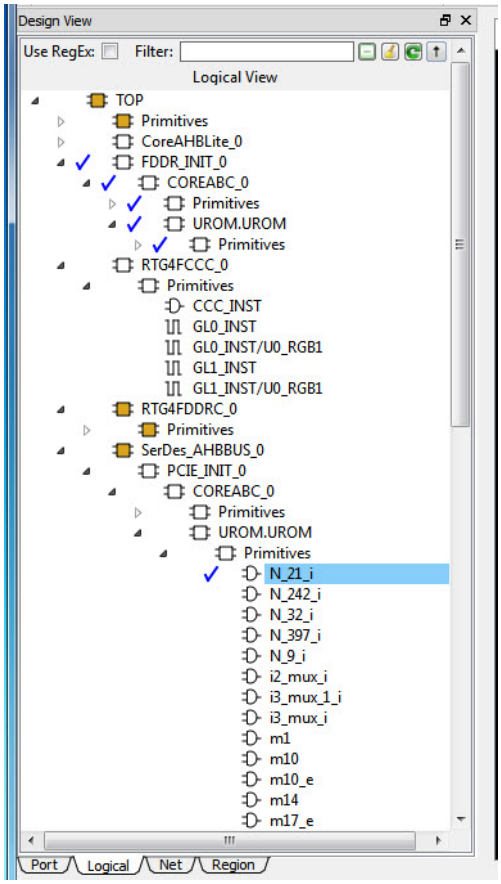


***Figure 5-6* • Macro Assigned to a User Region**

The Log window prints the message that PDC files are updated/written to reflect the changes you have made in Chip Planner.

The <proj_location>\constraint\<root>.fp.pdc is updated with the assign_region PDC command:

```
define_region -name UserRegion1 -type inclusive -color 2147442270 552 300 731 311
assign_region UserRegion1 FDDR_INIT_0
```

For details about PDC commands, refer to the PDC Commands User's Guide.

Routing Inside a Constrained Region

By default, when a region is first created, the region properties (Inclusive/Exclusive/Empty) apply to design resources (Placement) only. The Place and Route tool is free to use the routing resources inside the region. To further constrain the Place and Route tool on routing resources usage inside the region, click the **Constrain Routing** checkbox in the Properties window.

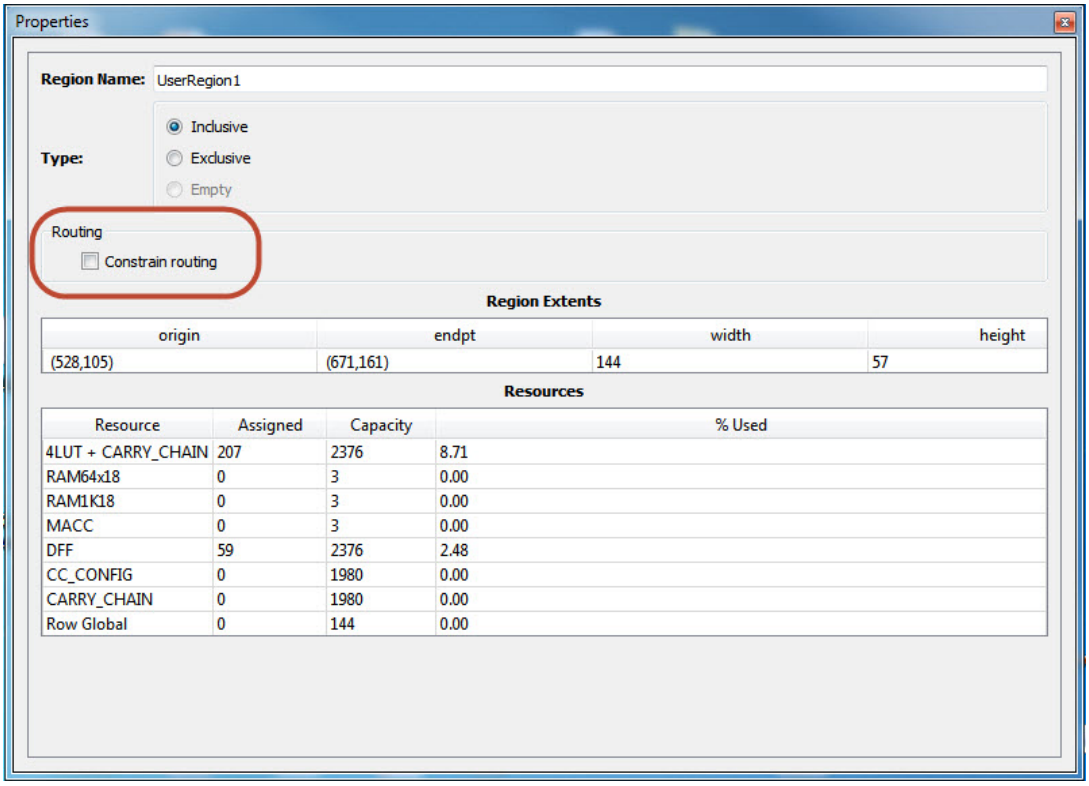


Figure 5-7 • **Constrain Routing Checkbox inside Property Window**

Constrain Routing

This option applies to all types of regions: inclusive, exclusive, and empty.

When this checkbox is checked, the region constraints are applied to routing, in addition to placement. The routing behavior is summarized in Table 5-1 for each type of user region.

Table 5-1 • **Routing Behavior Inside User Regions with Constrain Routing Enabled**

Region Type	Routing Behavior
Inclusive	• For all nets internal to the region (the source and all destinations belong to the region), routing must be inside the region (that is, such nets cannot be assigned any routing resources that are outside the region or cross the region boundaries). • Nets not internal to the region can use routing resources within the region.
Exclusive	• For all nets internal to the region (the source and all destinations belong to the region), routing must be inside the region (that is, such nets cannot be assigned any routing resources that are outside the region or cross the region boundaries). • Nets without pins inside the region cannot be assigned any routing resources that are outside the region or cross region boundaries).
Empty	• No routing is allowed inside the Empty Region. • However, local clocks and globals can cross empty regions.

Empty Region General Guidelines

Empty regions allow you to create exclusive areas on the device where no logic placement can occur. Empty regions help guide the placer to pack your logic closer together and thereby use more local routing resources to connect it. You cannot create empty regions in areas that contain locked macros. Use the following guidelines for empty regions.

Use Empty Regions to Guide the Place-and-Route Process

If your design does not completely use up your target device (for example, 60% utilization or lower), use empty regions to cluster your logic placement into specific subareas of the chip. This helps when you have originally placed-and-routed the design into a smaller device but want to fit it to a larger part while still preserving the performance you have achieved in the smaller device.

Use Empty Regions to Reduce Routing Congestion

Creating empty regions next to the congested area(s) of your design helps reduce congestion. When you place an empty region next to congested logic blocks or regions, the placer cannot place any logic next to your region or logic block. Logic which would normally be placed there is forced to be placed somewhere else. Routing resources next to the congested area are freed up and provide the router more options to route signals into the congested block.

Before deciding to place empty region(s), analyze your design for congestion areas. Use the **Ratsnest** view in Chip Planner to see dense areas of connectivity into and out of your logic blocks or regions. Create empty regions in these congested areas and see it if improves the routability of your logic.

Use Empty Regions to Reserve Device Resources

If you want to preserve the placement of your existing design but plan additional modifications in the future, create empty regions in the areas of the chip where you plan to add additional logic. As you add new logic, remove or resize your empty regions accordingly to fit your new logic. Empty regions placed over I/O pins reserve them for future use as the I/O needs of your design changes. There are some restrictions for using empty regions in this manner.

Overbooking of Regions

Overbooking of regions (assigning resources over 100% utilization) is not allowed. When you try to overbook a region, Chip Planner shows the overbooked resource type in the "Properties Window"of the Region and the resources are not assigned to the region. The overbooked resource is highlighted in red in the Region Properties window.

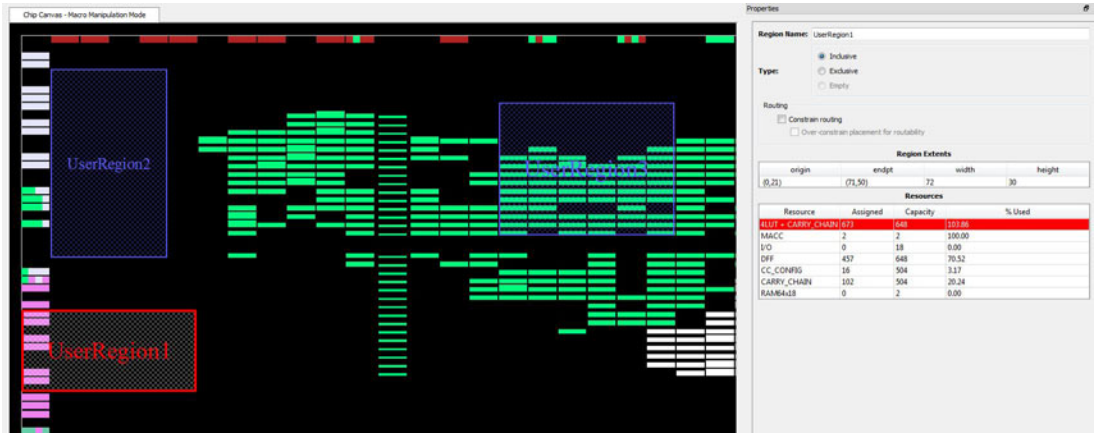


***Figure 5-8* • Overbooking of Region**

User Action in Regions in the Chip Canvas/Floorplanner View

When you select a region on the Chip Canvas, you may see some of the options below:

- Rename Regions
- Delete Regions
- Merge Regions
- Unassign macros from Regions
- Assign Macros inside Region
- Clone Region

Note: The Chip Canvas has two modes of operation: Macro Manipulation Mode and Region Manipulation Mode. If the Chip Canvas is in the Macro Manipulation Mode, before any region operations (Resizing/Renaming/Deleting/Merging), you must first click the Region/Macro Toggle Switch icon (Macro Manipulation Mode and Region Manipulation Mode buttons for PolarFire) to enter the Region Manipulation Mode.

Note: Any side-effects, such as unplacing or unassigning of a macro due to region creation or region resizing, are shown in the Log window.

6 – Netlist Views

In addition to the chip view for floorplanning purposes, the Chip Planner displays (in the same Chip Canvas window) a schematic view of the design to make it easier to trace nets and debug the design.

Two netlist types can be displayed in the Chip Canvas Window:

- Post-Synthesis Hierarchical View (NLV Hier/Hierarchical NLV)
- Post-compile flattened Netlist View (NLV Flat/Flat NLV)

The Chip view (Floorplanner View in PolarFire) and the Netlist Views are identified by tabs across the top of the window after they are loaded into memory. This makes it easy to switch between the different views.

NLV Hier View

The Post-Synthesis Hierarchical View (NLV Hier/Hierarchical NLV) is a hierarchical view of the netlist after synthesis and after technology mapping to the Microsemi FPGA technology. Click the **NLV Hier/ Hierarchical NLV** button to display this view. The Chip Planner loads the netlist into the system memory and displays it in the Canvas Window.

When the netlist is loaded for the first time into memory, a pop-up progress bar indicates the progress of the loading process, which may incur some runtime penalty for a large netlist.

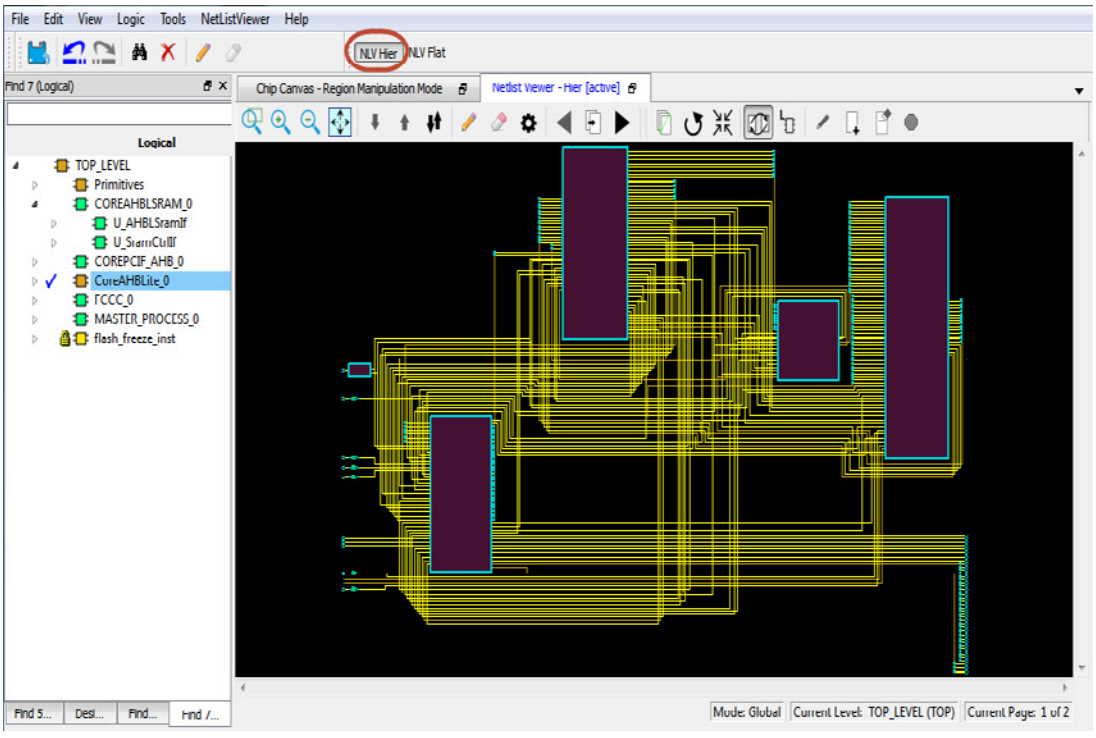


***Figure 6-1* • NLV Hierarchical View**

NLV - Flat View

This is the flattened (non-hierarchical) netlist generated after synthesis, technology mapping and further optimization based on the DRC rules of the device family and/or die. Click the **NLV Flat /Flat NLV** button to display this view. The Chip Planner loads the netlist into the system memory and displays it in the Canvas Window.

When the netlist is loaded for the first time into memory, a pop-up progress bar indicates the progress of the loading process, which may incur some runtime penalty for a large flattened netlist.

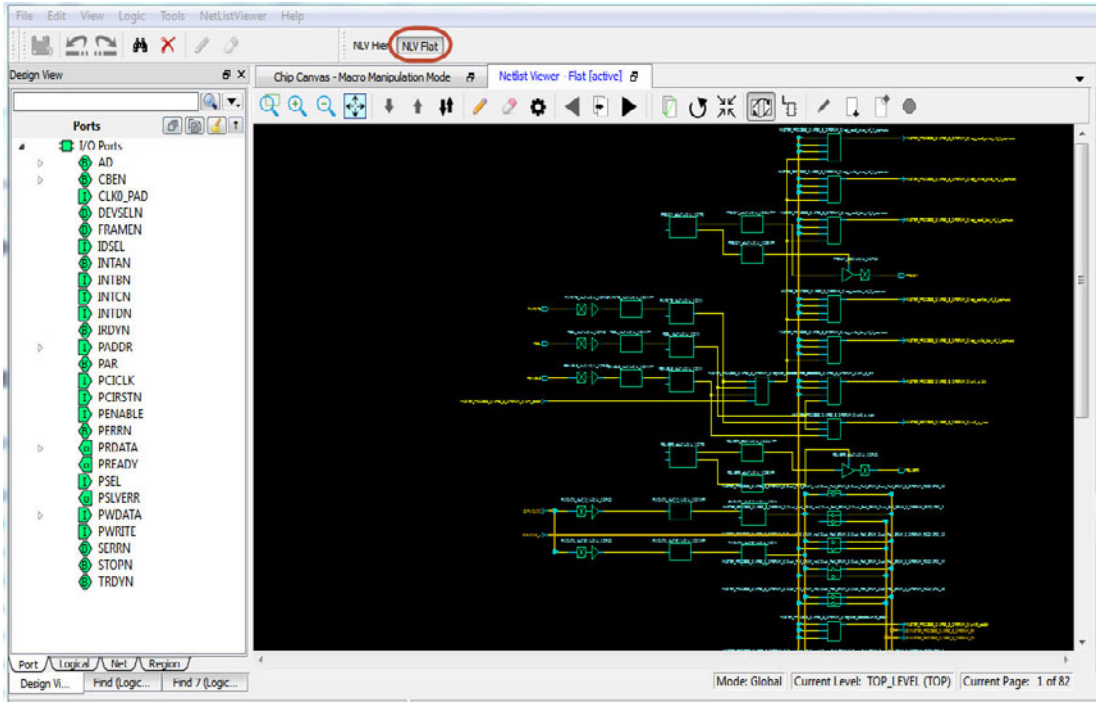


***Figure 6-2* • NLV - Flattened Netlist**

Display Across Multiple Pages

Hierarchical or flattened netlist may span across multiple pages, in which case the first page is displayed when it opens.

The current page number and the total number of pages are displayed in the status bar at the lower right corner of the window.

***Figure 6-3* • Status Bar**

To go to different pages of the Netlist view, use the left-pointing arrow  or right-pointing arrow  .

Netlist Viewer Features

See the Netlist Viewer Interface User Guide for details on the Netlist Viewer features.

7 – Cross-Probing from SmartTime to Chip View/ Netlist View

Cross-probing allows you to select a design object in one application and see the selection reflected in another application. When you cross-probe a design object from SmartTime to the Chip View /Netlist View, you will understand better how the two applications interact with each other.

Cross-probing from SmartTime to Chip View

With cross-probing, a timing path not meeting timing requirements may be fixed with relative ease when you see the less-than-optimal placement of the design object (in terms of timing requirement) in Chip Planner. Cross-probing from SmartTime to Chip Planner is available for the following design objects:

- Macros
- Ports
- Nets/Paths

Note: Cross-probing of design objects is available from SmartTime to Chip Planner but not vice versa.

Before you can cross-probe from SmartTime to Chip Planner, you must:

1. Complete Place and Route on the design.
2. Open both SmartTime and Chip Planner.

Cross-Probing Examples

To cross-probe from SmartTime to Chip Planner, a design macro in the SmartTime is used as an example.

Design Macro Example

1. Make sure that the design has successfully completed the Place and Route step.
2. Open SmartTime Maximum/Minimum Analysis view.
3. Open Chip Planner.
4. In the SmartTime Maximum Analysis view, right-click the instance Q[2] in the Timing Path Graph and choose **Show in Chip Planner**. With cross-probing, the Q[2] macro is selected in Chip Planner's Logical view and highlighted (white) in the Chip Canvas. The Properties window in Chip Planner displays the properties of Q[2].

Note: The menu item **Show in Chip Planner** is grayed out if Chip Planner is not already open.

Note: You may need to zoom in to view the highlighted Q[2] Macro in the Chip Canvas.

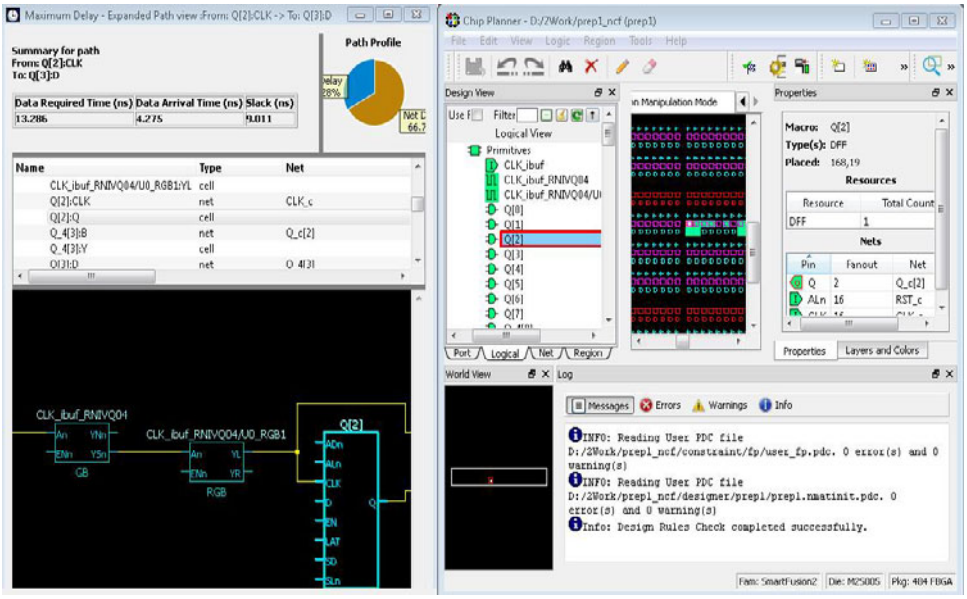


Figure 7-1 • **Cross-Probing the Q[2] Macro**

Timing Path Example

1. Make sure that the design has successfully completed the Place and Route step.
2. Open SmartTime Maximum/Minimum Analysis view.
3. Open Chip Planner.
4. In the SmartTime Maximum/Minimum Analysis view, right-click the net **Cliburn/U0/U_IOPAD:PAD** in the Table and choose **Show Path in Chip Planner**. Note that the net is selected (highlighted in red) in the Chip Canvas view and the three macros connected to the net are also highlighted (white) in the Chip Canvas view.

Note: The menu item **Show Path in Chip Planner** is grayed out if Chip Planner is not already open.

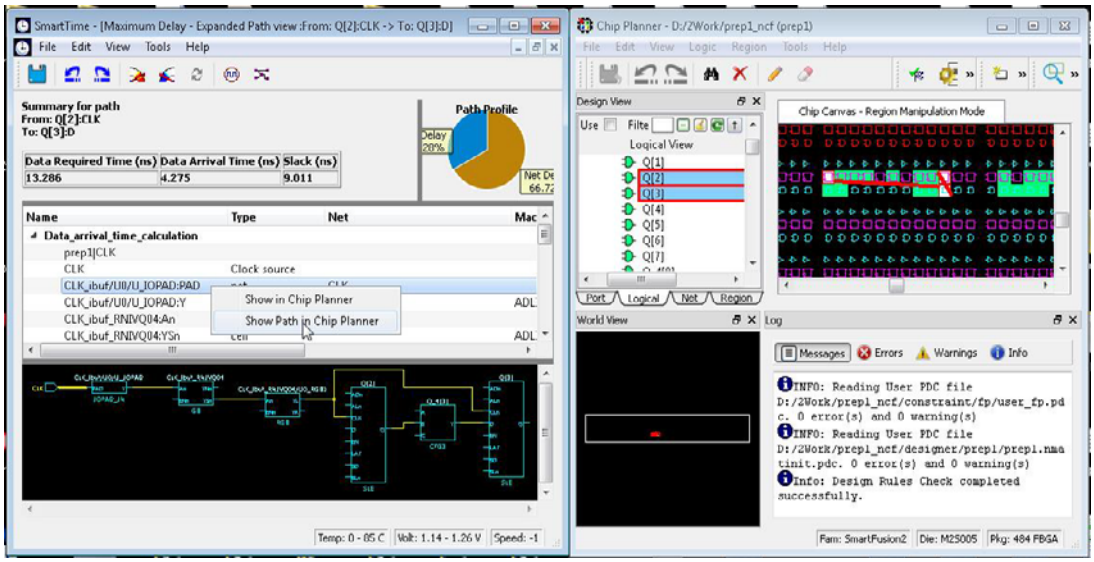


***Figure 7-2* • Cross-Probing - Timing Path**

Alternatively, right-click from SmartTime's Max/Min Delay Analysis Table view to cross-probe into Chip Planner.

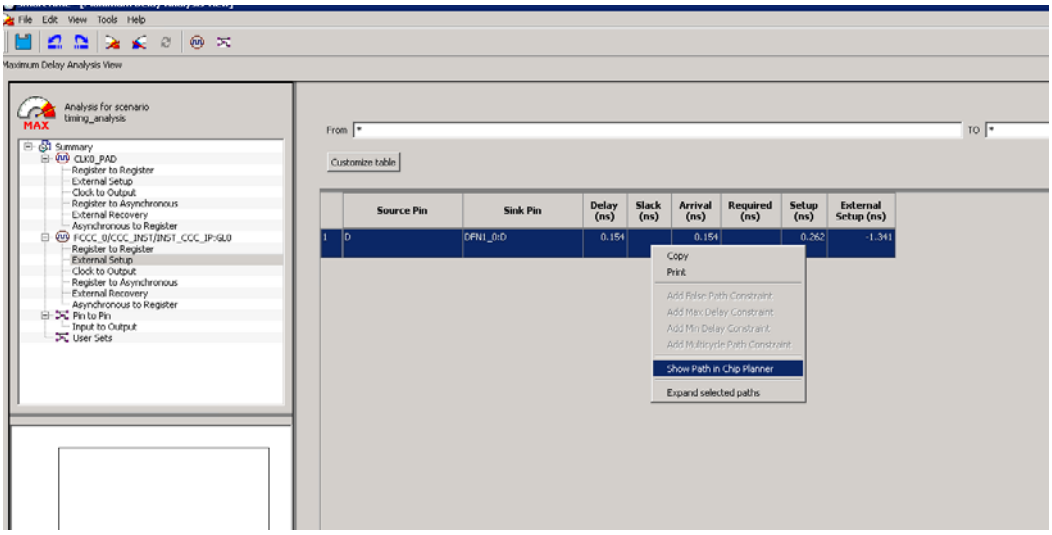


***Figure 7-3* • Cross-Probing from Max/Min Delay Analysis View Table**

Port Example

1. Make sure that the design has successfully completed the Place and Route step.
2. Open the SmartTime Maximum/Minimum Analysis view.
3. Open Chip Planner.
4. In the SmartTime Maximum/Minimum Analysis view, right-click the port **CLK** in the Path and choose **Show in Chip Planner**. Note that the port "CLK" is selected and highlighted in Chip Planner's Port view.

Note: The menu item Show in Chip Planner is grayed out if Chip Planner is not already open.

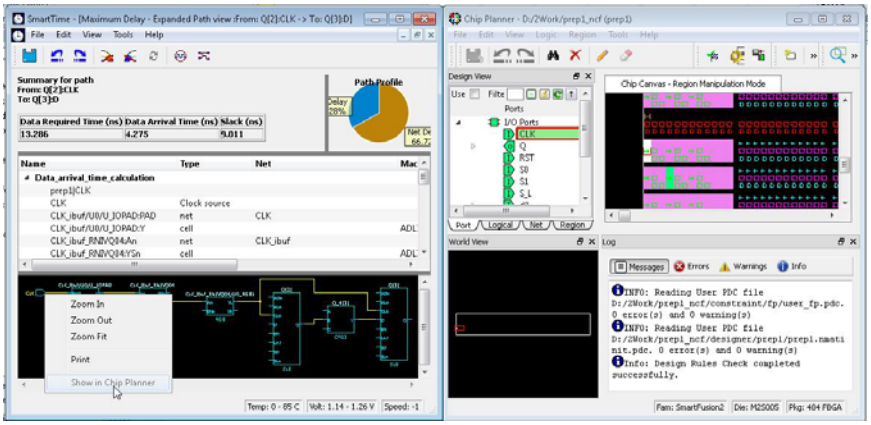


***Figure 7-4* • Cross-Probing - Port**

From the Properties view inside Chip Planner, you will find useful information about the Port “CLK” you are cross-probing:

- Port Type
- Port Placement Location (X-Y Coordinates)
- I/O Bank Number
- I/O Standard
- Pin Assignment

Cross-probing from Chip Planner to Netlist Viewer

To cross-probe from Chip Planner to the Netlist Viewer (Flattened AFL View only):

1. Open Chip Planner and Load the Flattened AFL Netlist into Netlist Viewer.
2. Select the design object in Chip Planner: Ports in Port Tab, Macros in Logical Tab and Nets in Net Tab.

Figure 7-5 shows the Port PRDATA[22] selected in the Logical tab and highlighted in the etlist Viewer.

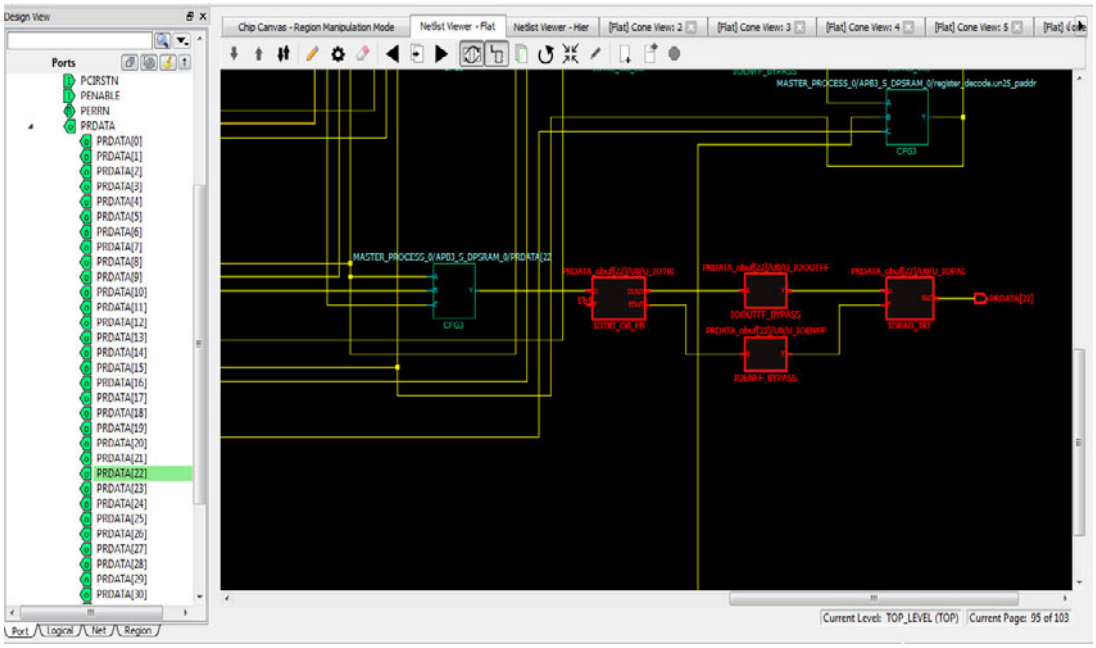


Figure 7-5 • **Cross-probe from Chip Planner to Netlist Viewer**

Cross-probing from SmartTime to Netlist Viewer

Cross-probing from SmartTime to Netlist Viewer allows you to examine and debug timing-critical paths as the first step towards timing closure. Timing paths with setup or hold time violations can be selected and cross-probed from SmartTime to Netlist Viewer to examine how the net is routed. Cross-probing may reveal and identify routing congestions.

To cross-probe a net from SmartTime to Netlist Viewer:

1. Complete the Place-and-Route step.
2. Open Chip Planner.
3. Load the Flattened AFL Netlist into Netlist Viewer.
4. Open SmartTime in the Design Flow window.
5. Open the Maximum/Minimum Delay Analysis View.
6. Click on a timing path to open the Timing Path display in SmartTime.
7. Right-click a net in the timing path display or a timing path in the SmartTime table and select **Show in Chip Planner**.

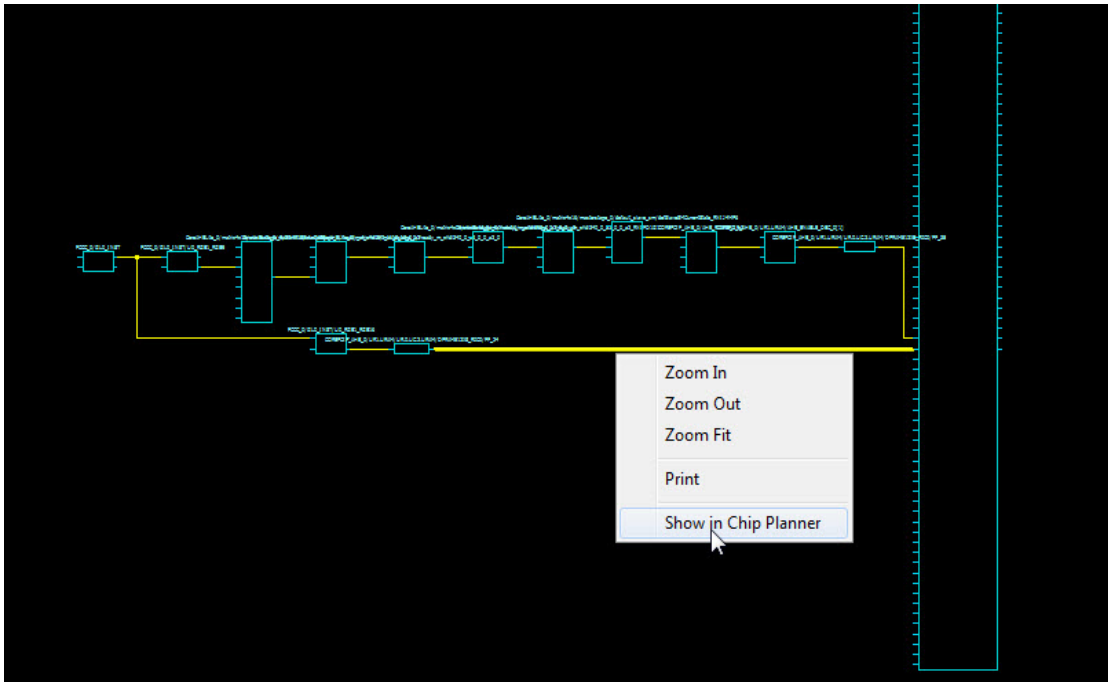


***Figure 7-6* • Cross-Probe From SmarTime to NelistViewer**

Netlist Viewer opens a Logical Cone View to display the selected path and highlight it (Figure 7-7).

***Figure 7-7* • Cross-Probed Net in Netlist Viewer Logical Cone View**

8. If desirable, add Drivers or Loads to the net in the Netlist Active Cone view for debugging.

Note: The cone view may not show the path's input IO or some extra macros along the path added by the Flattened View(but not shown in the SmartTime Path). To get a complete path in the Logical Cone View, double click the dashed net or right-click > add driver/load to cone.

A - Limitations

This appendix lists Chip Planner limitations:

I/O Register Support

Every I/O has several embedded registers that you can use for faster clock-to-out timing, and to meet external hold and setup timing requirements. This feature uses input, output, or enable registers available in the I/O block.

However, a register (if combined with an I/O register) is not shown in the Logical view as a separate element, and is shown as part of a port.

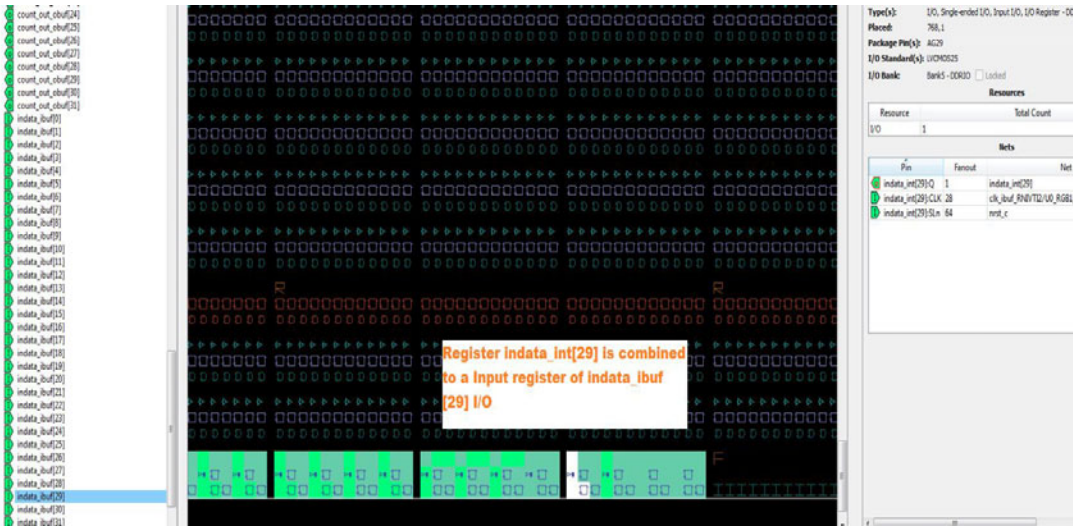


***Figure B-1* • Register Combined with Input Register of an I/O**

Internal Elements of External IP Macros Displayed in a Single Connection

Some external IP, such as SERDES and FDDR, span across multiple clusters and have their own dedicated ports. However, the net connected to these macro I/Os are shown to be connected from a single location. Figure B-2 is an example of a SERDES macro which shows all the associated nets connected to a single macro.

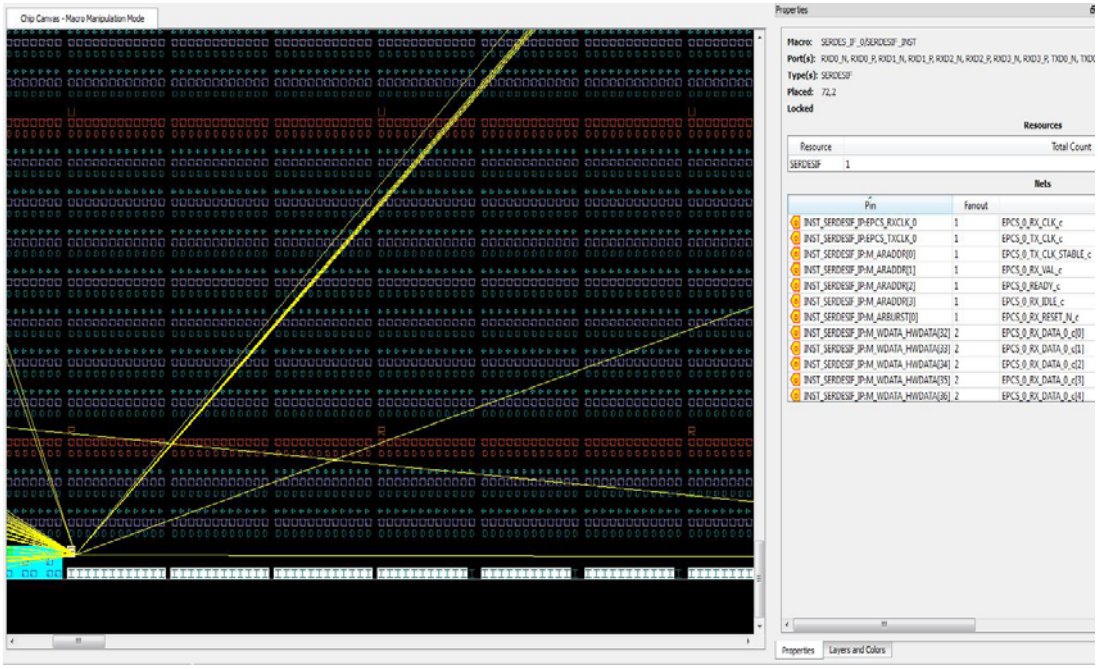


Figure B-2 **• SERDES Macro with Associated Nets in a Single Connection**

Cross-probing into SmartTime Unavailable

Cross-probing from the Chip View /Netlist View into SmartTime is not available. Cross-probing is supported for SmartTime to Chip View/Netlist View but not vice versa.

B – Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call **800.262.1060**
From the rest of the world, call **650.318.4460**
Fax, from anywhere in the world, **650.318.8044**

Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

For Microsemi SoC Products Support, visit http://www.microsemi.com/products/fpga-soc/design-support/fpga-soc-support.

Website

You can browse a variety of technical and non-technical information on the Microsemi SoC Products Group home page, at www.microsemi.com/soc.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

My Cases

Microsemi SoC Products Group customers may submit and track technical cases online by going to My Cases.

Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office.

Visit About Us for sales office listings and corporate contacts.

Sales office listings can be found at www.microsemi.com/soc/company/contact/default.aspx.

ITAR Technical Support

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech_itar@microsemi.com. Alternatively, within My Cases, select **Yes** in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the ITAR web page.