Libero SoC PolarFire v2.2

Release Notes

7/2018

Microsemi
Power Matters.™

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Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision 1.3

Revision 1.3 includes the following changes (07/11/2018):

- Added Known Issue 5.12 IOD CDR

Revision 1.2

Revision 1.2 includes the following changes (06/29/2018):

- Known Issue 5.21 I/O Register Combining – revised text to improve clarity

Revision 1.1

Revision 1.1 includes the following changes (06/05/2018):

- Added Known Issue 5.26 sNVM write fails due to ROM client created by previous design
- Additional updates to expand information and improve clarity

Revision 1.0

Revision 1.0 was the first publication of this document (06/01/2018).

Reference Documents

PO0137: Product Overview PolarFire FPGA

DS0141: PolarFire FPGA Datasheet

UG0722: PolarFire FPGA Packaging and Pin Descriptions User Guide

Pin package Assignment Tables:

- MPF300T/MPF300TS-FCG484 Package Pin Assignment Table
- MPF300T/MPF300TS-FCVG484 Package Pin Assignment Table
- MPF300T/MPF300TS-FCSG536 Package Pin Assignment Table
- MPF300T/MPF300TS-FCG784 Package Pin Assignment Table
- MPF300T/MPF300TS-FCG1152 Package Pin Assignment Table

UG0752: PolarFire FPGA Power Estimator User Guide

UG0680: PolarFire FPGA Fabric User Guide

UG0684: PolarFire FPGA Clocking Resources User Guide

UG0686: PolarFire FPGA User I/O User Guide

UG0677: PolarFire FPGA Transceiver User Guide

UG0685: PolarFire FPGA PCI Express User Guide

UG0687: PolarFire FPGA 1G Ethernet Solutions User Guide

UG0727: PolarFire FPGA 10G Ethernet Solutions User Guide

UG0676: PolarFire FPGA DDR Memory Controller User Guide

UG0748: PolarFire FPGA Low Power User Guide

Athena TeraFire Cryptographic Algorithm Library (CAL) Users Guide

UG0743: PolarFire FPGA Debugging User Guide

UG0714: PolarFire FPGA Programming User Guide

UG0725: PolarFire FPGA Device Power-Up and Resets User Guide

UG0726: PolarFire FPGA Board Design User Guide

UG0753: PolarFire FPGA Security User Guide

UG0786: PolarFire FPGA Splash Kit User Guide

DG0755: PolarFire FPGA JESD204B Interface Demo Guide

DG0756: PolarFire FPGA PCIe Endpoint Demo Guide

DG0757: PolarFire FPGA 10GBASE-R Ethernet Loopback Demo Guide

DG0759: PolarFire FPGA Multi-Rate Transceiver Demo Guide

DG0762: PolarFire FPGA DSP FIR Filter Demo Guide

Verilog Simulation Guide

VHDL Simulation Guide

PolarFire FPGA Design Flow User Guide

PolarFire FPGA Macro Library Guide

PolarFire FPGA Design Constraints User Guide

PolarFire FPGA PDC Commands User Guide

PolarFire FPGA Timing Constraints User Guide

PolarFire FPGA Tcl Commands User Guide

PolarFire FPGA I/O Editor User Guide

Chip Planner User Guide

Netlist Viewer Interface User Guide

PolarFire FPGA Netlist Viewer User Guide

SmartPower User Guide

Timing Constraints Editor User Guide

SmartTime Static Timing Analyzer User Guide

PolarFire FPGA SmartDebug User Guide

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1 Libero SoC PolarFire™ v2.2 Software Release Notes

The Libero® system on chip (SoC) PolarFire™ v2.2 release is software for designing with Microsemi PolarFire FPGAs. PolarFire FPGAs are the fifth generation nonvolatile FPGA devices from Microsemi, built on 28-nm flash technology. The PolarFire cost-optimized FPGAs deliver lowest power at mid-range densities.

For more information about PolarFire devices, see the Microsemi website.

1.1 Software Enhancements in Libero SoC PolarFire v2.2

The Libero SoC PolarFire v2.2 release includes the following new features and enhancements.

1.1.1 Runtime improvements

- Place-and-route runtime improved by ~15% on average
- Programming File Generation runtime improved by 2.5x
- Device Programming runtime improved by 2x
- Responsiveness enhancements added in this release:
    - Opening a Libero Project
    - Opening I/O Editor, Chip Planner, SmartDebug, and Programming Tools
    - Freeze/Unfreeze calculations while interacting with the SmartPower UI

1.1.2 Libero Project Management

- Compile Point Flow: Fully supported in Libero SoC PolarFire v2.2
- Libero Vault Management: Libero now supports read-only IP vaults, removing the need for users to have write permissions to the folder where the IP vault resides

1.1.3 Synthesis

The following enhancements for PolarFire are included in SynplifyPro N-2017.09M-SP1-1 release:

- DSP: Shift Chain inference using MACC_PA_BC_ROM blocks. Packing is supported for Direct Form FIR filters with pre-cascaded adder structures and Systolic FIR filters.
- SRAM initialization: Initial value packing is supported for RAM1K20 and RAM64x12 blocks. It is also supported for ECC mode of RAM1K20.
- RAM inference with initialization: RTL RAM descriptions with initialization statements will automatically be initialized at powerup, with the specified content
    - RAM Initialization Clients will automatically be created, and shown in the RAM Initialization Tab of the Design and Memory Initialization tool; use this tool to select whether RAM Initialization content is to be stored in sNVM, uPROM, or in external SPI Flash Memory.
    - Ensure that the logic connected to the inferred RAM starts after the RAM has been initialized, as indicated by assertion of the relevant PF_INIT_MONITOR outputs below:
        - USRAM_INIT_FROM_SNVM_DONE
        - USRAM_INIT_FROM_UPROM_DONE
        - USRAM_INIT_FROM_SPI_DONE
        - SRAM_INIT_FROM_SNVM_DONE
        - SRAM_INIT_FROM_UPROM_DONE

- SRAM_INIT_FROM_SPI_DONE

Note: For VHDL designs containing RAMs initialized with the statement *"others => '0'"*, an initialization client will be created for each such RAM.

- The next-generation HDL Analysis tool is enabled by default. This version contains many new and improved features, such as:
  - Multi-threaded Find improvements
  - New schematic preferences
  - Dissolving of ports
  - Handling of partially dissolved nets
  - Cross-probing to objects in a source file from the HDL Analyst schematic
  - HDL Analyst tool also supports new and updated Tcl and find commands

Note: Application Notes describing the enhancements above will be available at a later date.

1.1.4 Simulation support

- Simulation is now supported for the following cores:
  - Crypto
  - Tamper
  - TVS (Temperature and Voltage Sensors)
  - System Services
- Simulation support has been added for PCIE *PERST_N and SECDED for the following devices: MPF100/200/300/500 T/TS/TL/TLS.
- Fabric RAMs' ECC behavior can now be simulated. You will be able to add two additional options in the vsim commands under Simulation options of Libero SoC PolarFire v2.2 to stimulate the ECC flags of all LSRAM blocks in a PolarFire design:
  - -gERROR_PROBABILITY=<value>, where 0 <= value <= 1
  - -gCORRECTION_PROBABILITY=<value>, where 0 <= value <= 1

  During simulation, the SB_CORRECT and DB_DETECT flags on each LSRAM block will be asserted randomly with an occurrence rate depending on the probability set in the options above.

Note: Post-Synthesis File Generation/Simulation is in Beta phase for this release. Post-Synthesis simulation for IOD interfaces and DDR/QDR Memories is not supported.

1.1.5 Automatic placement of PLL, DLL, CLKINT, NGMUX, and CLK_DIV macros

Libero SoC PolarFire v2.2 now automatically places the PLL, DLL, CLKINT, NGMUX, and CLK_DIV macros, as part of the Place and Route step. You may remove existing PDC commands targeting these macros.

Note: You must still place Memory, Transceiver (XCVR, TXPLL, XCVR_REF_CLK), and IOD Interfaces using PDC or I/O Editor.

1.1.6 Timing

- Added '-add_delay', '-rise', and '-fall' options for set_input_delay and set_output_delay SDC commands
- Added '-add' option for create_clock and create_generated_clock SDC commands

1.1.7 Design Initialization

Libero SoC PolarFire v2.2 includes updates to the Design Initialization flow:

- The design can be securely initialized from SPI Flash with encrypted initialization bitstream and design binding
- RAM Initialization Enhancements
    - Each logical RAM in the design can be initialized from a different source – sNVM, uPROM, or SPI-Flash.
    - RAM Initialization for inferred RAMs with initialization statements in RTL.

Note: Application Notes describing these enhancements will be available at a later date.

- The PolarFire Initialization Monitor (PF_INIT_MONITOR) core has been updated for better coordination with power up events:
    - A new signal, XCVR_INIT_DONE, is exposed to indicate when the Transceiver blocks have been initialized.
    - The following USRAM and LSRAM initialization signals have also been added:
        - USRAM_INIT_FROM_SNVM_DONE
        - USRAM_INIT_FROM_UPROM_DONE
        - USRAM_INIT_FROM_SPI_DONE
        - SRAM_INIT_FROM_SNVM_DONE
        - SRAM_INIT_FROM_UPROM_DONE
        - SRAM_INIT_FROM_SPI_DONE
    - The AUTOCALIB_DONE port has been added, indicating when I/O calibration is complete. This port is not to be used on the MPF300XT or MPF300_ES device variants.

1.1.8 SmartDebug

- sNVM and uPROM view enhancements
- New Programming Connectivity and Interface TCL commands have been added to Standalone SmartDebug
- Optimize DFE flow enhancements
- Power ON eye monitor option in Plot Eye
- Generate SmartDebug FPGA Array Data tool in Libero Design Flow

1.2 Silicon Features

Libero SoC PolarFire v2.2 includes enhancements targeting Silicon Support.

1.2.1 I/O's

Input/Output static I/O delays

With this release, you can set static input and output delays on a per-I/O basis, through PDC, or using the I/O Editor tool. These delays will also be propagated to SmartTime and timing reports.

I/O Register Combining is turned OFF

I/O Register Combining is disabled for all I/O's in this release. The I/O Register Combining feature will be re-enabled in a subsequent release.

I/O Standards removed

The following I/O standards are no longer supported by PolarFire devices, and are not available in Libero SoC PolarFire v2.2:

- LVSTL11I
- LVSTL11II
- LVPECL25
- MIPI25 (ES/XT only)

If your pre-Libero SoC PolarFire v2.2 design contains these standards, it will be invalidated to pre-Synthesis.

1.2.2 Memories

Libero SoC PolarFire v2.2 supports QDRII+ memories; you can instantiate and configure them from the Libero Catalog.

Libero SoC PolarFire v2.2 also includes the following enhancements for DDR3, DDR4, and LPDDR3:

- The Lookahead pre-charge feature is now available
- Command queue depth can be adjusted
- Timing performance (i.e. max fabric clock frequency) has been improved

1.2.3 IOD Interfaces

In this release, all IOD Interfaces have updated configuration DRCs. As a result, all IOD components will be invalidated. You must upgrade your IOD RX components. IOD receive interfaces are supported with timing adjustments statically set by Libero. There is no autonomous support for dynamically trained interfaces. In addition, all IOD TX and RX interfaces may now be used on Silicon.

2 Device Support

2.1 MPF300XT

With Libero SoC PolarFire v2.2, Production Power support is added for the MPF300XT device, the first production device in the PolarFire FPGA family. This release includes the following support for this device:

- Full Libero flow
- Production Timing Data
- Production Power Data
- Programming support
- SmartDebug support
- Design-specific IBIS generation support
- Simultaneous Switching Noise (SSN) Analysis support (for the FCG1152 package only)

2.2 Pre-production devices

Programming support for the MPF300T/TS and MPF200T/TS pre-production devices has been enabled in the Libero SoC PolarFire 2.2 release.

2.3 Low-static power devices

This release introduces the “L” series of PolarFire devices, featuring a reduction in static power.

2.4 PolarFire Devices supported in Libero SoC PolarFire v2.2

Note: Devices and packages in bold are new in v2.2

Device	Package	Speed Grade	Core Voltage	Range	License Required
MPF100T	FCSG325	-1, STD	1.0/1.05V	EXT/IND	Eval/Silver/Gold/Platinum
	FCVG484	-1, STD	1.0/1.05V	EXT/IND	Eval/Silver/Gold/Platinum
	FCG484	-1, STD	1.0/1.05V	EXT/IND	Eval/Silver/Gold/Platinum
MPF100TL	**FCSG325**	**STD**	**1.0/1.05V**	**EXT/IND**	**Eval/Silver/Gold/Platinum**
	FCVG484	**STD**	**1.0/1.05V**	**EXT/IND**	**Eval/Silver/Gold/Platinum**
	FCG484	**STD**	**1.0/1.05V**	**EXT/IND**	**Eval/Silver/Gold/Platinum**
MPF100TLS	**FCSG325**	**STD**	**1.0/1.05V**	**IND**	**Eval/Platinum**
	FCVG484	**STD**	**1.0/1.05V**	**IND**	**Eval/Platinum**
	FCG484	**STD**	**1.0/1.05V**	**IND**	**Eval/Platinum**
MPF100TS	FCSG325	-1, STD	1.0/1.05V	IND	Eval/Platinum
	FCVG484	-1, STD	1.0/1.05V	IND	Eval/Platinum
	FCG484	-1, STD	1.0/1.05V	IND	Eval/Platinum
MPF200T	FCSG325	-1, STD	1.0 /1.05V	EXT/IND	Eval/Gold/Platinum
	FCSG536	-1, STD	1.0 /1.05V	EXT/IND	Eval/Gold/Platinum

	FCVG484	-1, STD	1.0 /1.05V	EXT/IND	Eval/Gold/Platinum
	FCG484	-1, STD	1.0 /1.05V	EXT/IND	Eval/Gold/Platinum
	FCG784	-1, STD	1.0 /1.05V	EXT/IND	Eval/Gold/Platinum
MPF200TL	**FCSG325**	**STD**	**1.0 /1.05V**	**EXT/IND**	**Eval/Gold/Platinum**
	FCSG536	**STD**	**1.0 /1.05V**	**EXT/IND**	**Eval/Gold/Platinum**
	FCVG484	**STD**	**1.0 /1.05V**	**EXT/IND**	**Eval/Gold/Platinum**
	FCG484	**STD**	**1.0 /1.05V**	**EXT/IND**	**Eval/vGold/Platinum**
	FCG784	**STD**	**1.0 /1.05V**	**EXT/IND**	**Eval/Gold/Platinum**
MPF200TLS	**FCSG325**	**STD**	**1.0 /1.05V**	**IND**	**Eval/Platinum**
	FCSG536	**STD**	**1.0 /1.05V**	**IND**	**Eval/Platinum**
	FCVG484	**STD**	**1.0 /1.05V**	**IND**	**Eval/Platinum**
	FCG484	**STD**	**1.0 /1.05V**	**IND**	**Eval/Platinum**
	FCG784	**STD**	**1.0 /1.05V**	**IND**	**Eval/Platinum**
MPF200TS	FCSG325	-1, STD	1.0/1.05V	IND	Eval/Platinum
	FCSG536	-1, STD	1.0/1.05V	IND	Eval/Platinum
	FCVG484	-1, STD	1.0/1.05V	IND	Eval/Platinum
	FCG484	-1, STD	1.0/1.05V	IND	Eval/Platinum
	FCG784	-1, STD	1.0/1.05V	IND	Eval/Platinum
MPF300T_ES	FCG484	-1, STD	1.0 /1.05V	EXT/IND	Eval/Platinum
	FCG1152	-1, STD	1.0 /1.05V	EXT/IND	Eval/Platinum
	FCSG536	-1, STD	1.0 /1.05V	EXT/IND	Eval/Platinum
	FCVG484	-1, STD	1.0 /1.05V	EXT/IND	Eval/Platinum
	FCG784	-1, STD	1.0/1.05V	EXT/IND	Eval/Platinum
MPF300TS_ES	FCG484	-1, STD	1.0 /1.05V	EXT/IND	Eval/Gold/Platinum
	FCG 1152	STD	1.0 /1.05V	EXT/IND	Eval/Platinum
		-1	1.0 /1.05V	EXT/IND	Eval/Gold/Platinum
	FCSG536	-1, STD	1.0 /1.05V	EXT/IND	Eval/Platinum
	FCVG484	-1, STD	1.0 /1.05V	EXT/IND	Eval/Platinum
	FCG784	-1, STD	1.0 /1.05V	EXT/IND	Eval/Platinum
MPF300XT	FCG1152	-1, STD	1.0 /1.05V	EXT/IND	Eval/Platinum
	FCG484	-1, STD	1.0 /1.05V	EXT/IND	Eval/Platinum
	FCG784	-1, STD	1.0 /1.05V	EXT/IND	Eval/Platinum
MPF300T	FCG484	-1, STD	1.0 /1.05V	EXT/IND	Eval/Platinum
	FCG1152	-1, STD	1.0 /1.05V	EXT/IND	Eval/Platinum
	FCSG536	-1, STD	1.0 /1.05V	EXT/IND	Eval/Platinum
	FCVG484	-1, STD	1.0 /1.05V	EXT/IND	Eval/Platinum
	FCG784	-1, STD	1.0/1.05V	EXT/IND	Eval/Platinum
MPF300TL	**FCG484**	**STD**	**1.0 /1.05V**	**EXT/IND**	**Eval/Platinum**
	FCG1152	**STD**	**1.0 /1.05V**	**EXT/IND**	**Eval/Platinum**
	FCSG536	**STD**	**1.0 /1.05V**	**EXT/IND**	**Eval/Platinum**
	FCVG484	**STD**	**1.0 /1.05V**	**EXT/IND**	**Eval/Platinum**
	FCG784	**STD**	**1.0/1.05V**	**EXT/IND**	**Eval/Platinum**

MPF300TLS	**FCG484**	**STD**	**1.0 /1.05V**	**IND**	**Eval/Platinum**
	FCG1152	**STD**	**1.0 /1.05V**	**IND**	**Eval/Platinum**
	FCSG536	**STD**	**1.0 /1.05V**	**IND**	**Eval/Platinum**
	FCVG484	**STD**	**1.0 /1.05V**	**IND**	**Eval/Platinum**
	FCG784	**STD**	**1.0/1.05V**	**IND**	**Eval/Platinum**
MPF300TS	FCG484	-1, STD	1.0/1.05V	IND	Eval/Gold/Platinum
	FCG1152	STD	1.0 /1.05V	IND	Eval/Platinum
		-1	1.0 /1.05V	IND	Eval/Gold/Platinum
	FCSG536	-1, STD	1.0/1.05V	IND	Eval/Platinum
	FCVG484	-1, STD	1.0/1.05V	IND	Eval/Platinum
	FCG784	-1, STD	1.0/1.05V	IND	Eval/Platinum
MPF500T	FCG784	-1, STD	1.0/1.05V	EXT/IND	Eval/Platinum
	FCG1152	-1, STD	1.0/1.05V	EXT/IND	Eval/Platinum
MPF500TL	**FCG784**	**STD**	**1.0/1.05V**	**EXT/IND**	**Eval/Platinum**
	FCG1152	**STD**	**1.0/1.05V**	**EXT/IND**	**Eval/Platinum**
MPF500TLS	**FCG784**	**STD**	**1.0/1.05V**	**IND**	**Eval/Platinum**
	FCG1152	**STD**	**1.0/1.05V**	**IND**	**Eval/Platinum**
MPF500TS	FCG784	-1, STD	1.0 /1.05V	IND	Eval/Platinum
	FCG1152	-1, STD	1.0 /1.05V	IND	Eval/Platinum

See the Licensing web page for licensing details.

2.5 PolarFire Devices' Timing and Power Data State in Libero SoC PolarFire v2.2

Device	Timing Data State	Power Data State
MPF100T/TS/TL/TLS	Advance	Advance
MPF200T/TS/TL/TLS	Advance	Advance
MPF300TS_ES	Advance	Advance
MPF300XT	Production	Production
MPF300T/TS/TL/TLS	Preliminary	Preliminary
MPF500T/TS/TL/TLS	Advance	Advance

3 Design Migration

3.1 General Notes on Design Migration

3.1.1 Design Invalidation

Libero SoC PolarFire v2.2 is a major release milestone in the Microsemi® PolarFire FPGA program. Bug fixes and enhancements to some silicon features may require core upgrades for users migrating from Libero SoC PolarFire v2.1.

1. After opening your project in this release, you must rerun Verify Power to regenerate the power report.
2. You must upgrade to the latest version, or regenerate cores that have been invalidated and re-generate existing designs through full implementation and timing verification flow.
    a. You must also rerun the Derive Constraints step before running Synthesis or Place-and-Route to get the most up-to-date configured core-related timing constraints.

The following is the list of cores that have been invalidated in Libero SoC PolarFire v2.2:

Core	User Action
DDR3	Upgrade to latest version in Catalog
DDR4	Upgrade to latest version in Catalog
LPDDR3	Upgrade to latest version in Catalog
PolarFire IOD Generic Receive Interfaces	Upgrade to latest version in Catalog

3.2 Cores Supported in Libero SoC PolarFire v2.2

Microsemi recommends upgrading to the latest versions of all cores.

Display Name	Libero SoC PolarFire v2.2	Changes from Libero SoC PolarFire v2.1
Clock Conditioning Circuitry (CCC)	1.0.113	PLL. Changed default value for Bandwidth option to Medium-Low – This provides the best combination of jitter and reference clock jitter tolerance in most systems.
Clock divider	1.0.102	None
CoreSmartBERT	2.1.102	Support for latest XCVR version
Crypto	1.0.105	Added support for AXI clock < 100MHz Added DRC to comply with datasheet Fmax
DDR3	2.3.108	See Section 1.2.2
DDR4	2.3.108	See Section 1.2.2
Glitchless clock mux	1.0.101	None
LPDDR3	2.2.103	See Section 1.2.2

PCI Express	1.0.242	Added support for AXI clock < 100MHz Enhanced presentation for BAR configuration
PF Dual-Port Large SRAM	1.1.110	None
PF Micro SRAM	1.1.107	None
PF Two-Port Large SRAM	1.1.108	None
PF uPROM	1.0.108	None
PolarFire 7:1 LVDS Receive Interface	1.0.104	None
PolarFire 7:1 LVDS Transmit Interface	1.0.104	None
PolarFire Dynamic Reconfiguration Interface	1.0.101	None
PolarFire IOD CDR	1.0.210	None
PolarFire IOD Generic Receive Interfaces	1.0.242	See Section 1.2.3
PolarFire IOD Generic Transmit Interfaces	1.0.236	See Section 1.2.3
PolarFire Initialization Monitor	2.0.103	See Section 1.1.4
PolarFire RC Oscillators	1.0.102	None
PolarFire RGMII TO GMII	1.0.208	None
PolarFire SRAM (AHBLite and AXI)	1.1.125	Added support for AXI data widths of 128, 256, 512
Tamper	1.0.105	UI Enhancements
Temperature and Voltage Sensor Interface	1.0.105	New in this release
Transceiver Interface	1.0.231	Jitter Attenuation support for 10GbE Fixed fabric PMA reset signals' configuration Fixed constraint generation for duty cycle
Transceiver Reference Clock	1.0.103	None
Transmit PLL	1.0.112	Jitter Attenuation support for 10GbE
PolarFire System Services	2.2.103	New in this release, replaces CORESYSSERVICES_PF Integrates sNVM configurator

4 Resolved Issues

The following table lists the customer-reported SARs resolved in Libero SoC PolarFire v2.2. Resolution of previously reported “Known Issues and Limitations” is also noted in this table.

4.1 List of Resolved Issues

Case Number	Description
493642-2454603495	PRPF_012: Failed to find a legal placement solution for instance 'RECGEN_i0/HS_IO_CLK_RX (HS_IO_CLK)'
493642-2353309721	SmartPower: Add missing calculation after domain frequencies are changed
493642-2447196563	Placer fails with Error: PRPF-002 for a design with IOD_GENERIC
493642-2446667986	Running DG0807 design (using PolarFire v2.1) gives a PRPF_012 error
493642-2436508862	PolarFire Bidirectional design with IO REG combining is not working
493642-2391276145	Libero crashes in Classic Constraint Flow
493642-2390373562	G5_IO: Support for programmable IO delay feature
493642-2390373562	Request for automatic placement of 3 PLLs feeding 2 NGMUX
493642-2351704505	Synthesis option must be turned off when the user imports a VM file
493642-2353309721	Add calculation freeze capability to SmartPower
493642-2347929747	Adding a *.sdc file, via link or import, causes the place and route checkbox to no longer function properly
493642-2347929747	SDC: create_clock - add feature support
493642-2338802602	Power on Reset "Delay" Setting in Libero
493642-2437199462	DDR3/4: Look ahead Precharge and Look ahead Activate controller features should be enabled
493642-2287287333, 493642-2323565379	HDL_PLUS: Core Definition is losing modified parameters
493642-2268812377	DDR: Constraints coverage report indicates numerous missing DDR constraints and violations
493642-2177605080	With an error in the PDC file, the Libero tool shows all stages completed successfully
493642-2178299344, 493642-2184951525, 493642-221619580	SDC: add_delay support (especially for constraining with regard to DDR rise and fall edges)
493642-2349601283, 493642-2396162779	Batch Mode: Remove X-Server Dependency for Libero
493642-2376357299	Synplify Pro error triggered by set_clock_groups constraint
	Block Flow must not be used for designs intended to be programmed onto silicon

5 Known Issues and Limitations

5.1 SPI Flash Programming

This release includes the following limitations:

- Only the Micron SPI Flash is currently supported with the Evaluation Kit.
- This tool erases the SPI Flash prior to programming. It is recommended to program the SPI Flash with Libero SoC PolarFire v2.2 prior to programming other data on the SPI Flash using non-Libero programming solutions.
- Partial update of the SPI Flash is currently not supported.
- It is not recommended to have huge gaps between clients in the SPI Flash, since gaps are currently programmed with 1's and will increase programming times.

  The following table lists the ERASE, PROGRAM, and VERIFY/READ times for different client sizes. All times are in hh:mm:ss.

  Note: Depending on the SPI-Flash memory silicon version, you may observe a shorter erase time.

SPI Size	ERASE	PROGRAM	VERIFY/READ	TCK	Programmer
1 MB	00:03:55	00:00:45	00:10:46	4MHz	FP5
1 MB	00:03:55	00:00:28	00:10:05	15MHz	FP5
9 MB	00:03:55	00:06:38	01:19:15	4MHz	FP5
9 MB	00:03:55	00:04:26	01:08:49	10MHz	FP5
18 MB	00:03:55	00:09:04	02:32:43	10MHz	FP5
128 MB	00:03:55	00:58:38	22:07:55	15MHz	FP5

5.2 SPI-Slave Programming

Programming Libero SoC PolarFire v2.2 via SPI instead of JTAG is currently not supported. Support for this use model will be added in a future release.

5.3 FlashPro Express - MPF300T_ES or MPF300TS_ES Programming File Fails to Program a MPF300XT Device

In FlashPro Express PolarFire v2.2, the MPF300T_ES or MPF300TS_ES programming file cannot program a MPF300XT device, and vice versa.

Workarounds:

1. Export a STAPL file for the target device.
2. Export a STAPL file from Libero and use standalone FlashPro on Windows in single mode to program.

5.4 Zeroization is Not Supported for ES and XT Devices

In Libero SoC PolarFire v2.2, zeroization is not supported for ES and XT devices. For more information, see the following documents:

ER0207 Errata: PolarFire FPGAs: Engineering Samples (ES) Devices

ER0215 Errata: PolarFire FPGAs: MPF300XT Devices

5.5 SmartDebug

This release includes the following limitations:

- General Limitations
  - Standalone SmartDebug: Non Microsemi Devices in chain: Microsemi devices present in chain along with non-Microsemi devices cannot be debugged using standalone SmartDebug. **Workaround**: Users should use SmartDebug through the Libero flow to debug Microsemi Devices.
  - Standalone SmartDebug: ID Code of Microsemi device cannot be read when non-Microsemi device is connected in chain when using standalone SmartDebug.

    Workaround: Users should use SmartDebug through the Libero flow to perform this operation.
  - Logical View: The logical view cannot be reconstructed for:
    - LSRAM/uSRAM for port widths of x1 inferred through RTL.
    - LSRAM/uSRAM configurations when a single net of output bus is used i.e. A_DOUT[0]/B_DOUT[0] for DPSRAM/uSRAM and RD[0] for TPSRAM and others are unused. The memories can be read/write using physical view.
    - LSRAM/uSRAM configurations inferred using IP Cores CoreAHBLtoAXI (Verilog flow), CoreFIFO (Verilog and VHDL flow).
    - HDL modules inferring RAM blocks that are instantiated in SmartDesign.

      Workaround: There are no workarounds for the issues above at this time.
  - Physical View: RAM content read using the Physical View of SmartDebug for LSRAM 1Kx18 configuration (which are inferred through RTL) is incorrect. This is due to improper pin assignments on A_DIN and A_DOUT ports. This will be fixed in upcoming PolarFire releases.
  - The new Libero Design Flow tool 'Generate SmartDebug FPGA Array Data' under Debug Design must be run before invoking SmartDebug. This tool runs automatically when a DDC file is exported in Libero.
- Transceiver Limitations
  - Plot Eye introduces a burst of errors in data traffic on XCVR lanes when started. This will be fixed in an upcoming PolarFire release.

    Workaround: Enable Eye Monitor using the PowerOn Eye Monitor option before starting the traffic. This will power on the DFE and EM receivers in CDR mode and no errors will be seen during eye plot.
  - For MPF200T/TS/TLS devices, Plot Eye does not work for Quad0 lanes if they are configured in CDR mode.

    Workaround: There is no workaround at this time.
  - The Custom DFE solution (using the Optimize DFE option in the Eye Monitor tab) does not work when the transceiver is configured in 8B10B PCS-PMA mode and the receiver is DFE.

    Workaround: Perform the following steps to obtain the expected eye output with PLOT_EYE.

    1. Assert PCS RX RESET
    2. Optimize DFE
    3. Plot Eye
    4. De-Assert PCS RX RESET
  - After running Optimize DFE on a lane in CDR mode, users will see data errors when doing eye plot. This will be fixed in upcoming PolarFire releases.

- Optimize DFE on lanes configured in CDR mode does not work for SmartBERT IP patterns (this is specific to the MPF200T device). This will be fixed in upcoming PolarFire releases.
- Optimize DFE on lanes configured in DFE mode does not work reliably (this is specific to the MPF200T device). This will be fixed in upcoming PolarFire releases.
- SmartBERT IP does not work when lanes are configured at 250Mbps data rate.
- SmartBERT IP PRBS tests take more time to start/stop/inject error on RHEL 7.x and Cent OS 7.x platforms as compared to RHEL 6.x and Windows OS. This issue is seen only with PRBS patterns from SmartBERT IP, and will be fixed in upcoming PolarFire releases.
- The Power ON eye monitor TCL command (eye_monitor_power) does not work correctly in PolarFire v2.2. RX PLL does not lock to the incoming data after this TCL command is run. This will be fixed in upcoming PolarFire releases.

  Workaround: There are no workarounds for the issues above at this time.

- Signal Integrity Limitation
  - The RX Polarity Signal Integrity parameter (Polarity P/N reversal) has no effect when a PDC file is imported using the Import option in SmartDebug. This flow works fine in GUI mode. This will be fixed in upcoming PolarFire releases.

5.6 DDR3 and DDR4 and LPDDR3 Memories

- The Constraints Coverage report indicates some missing constraints; this can be ignored.
- Dual rank is not supported for DDR3/DDR4.
- Data Bus Inversion is not supported for DDR4.

5.7 DLL

- **Secondary Phase Restrictions Missing:** Although the user can specify values for Primary and Secondary phase with no restrictions, the Secondary Phase value cannot be lower than the Primary Phase value.
  Workaround: Do not set the Secondary Phase value lower than the Primary Phase value.
- In DLL Phase Generation Mode, the secondary output clocks are not producing the correct phase in pre-synth HDL simulations.
  Workaround: There is no workaround at this time.

5.8 PLL

- Only the post-VCO feedback mode is available in this release.
- Bypass option on output clocks is not available in this release.

5.9 PCIe

- For BFM simulation of AXI master or slave, the simulator may print out a warning message about AHB signals, such as “HRESP”. The warning message can be ignored.

5.10 Transceiver

- MPF300XT: Soft DFE Solution does not work when transceiver is configured in 8B10B PCS Mode
  Workaround: There is no workaround at this time.

- The CDR lock mode “lock to reference” is not supported in Libero SoC PolarFire v2.2. It will be supported in an upcoming PolarFire release.
- The CDR lock mode “Burst Mode Receiver” (BMR) is not supported in Libero SoC PolarFire v2.2. It will be supported in an upcoming PolarFire release.

5.11 IOD Receive Interfaces

The External PLL option is not supported while using a Regional Clock for the IOD RX Interface. This option should not be used, and will be removed in a future release.

5.12 IOD CDR

Add false path constraints in designs with IOD CDR core:

```
set_false_path -to { */DELAY_CODE_TIP_*/lock_sync[1]/D }
set_false_path -to { */DELAY_CODE_TIP_*/diff_sync[1]/D }
set_false_path -to { */dll_inst_0/CODE_UPDATE }
```

5.13 Synthesis

The Synplify Pro software that is bundled with Libero SoC PolarFire v2.2 is intended to be used only with PolarFire devices.

Inferred MathBlocks: Libero SoC PolarFire v2.2 does not support the B2 pin of the MACC_PA_BC_ROM. The B2 pin going to fabric will not be routed. If this pin has been used in a SynplifyPro-inferred MACC_PA_BC_ROM or in HDL, Compile will error out with the message: “Using 'B2' pins is not supported in this release of software on instance”. This will be supported in the upcoming Libero SoC PolarFire v2.2 SP1 release.

5.14 Standalone Synthesis Flow

Libero SoC PolarFire v2.2 users may synthesize their design outside the PolarFire tool by using Synopsys SynplifyPro directly. When using this flow, the following additional steps are necessary to successfully synthesize and implement a design:

- Ensure that the <install location>/Designer/data/aPA5M/polarfire_syn_comps.v is passed to SynplifyPro. This file contains module declarations with timing information for PolarFire primitives not known to Synopsys.
- Many configured cores generate timing constraints. You must ensure that these constraint files are passed to synthesis for optimal results. These constraint files must also be imported into Libero along with the synthesis gate level netlist to get optimal place and route and timing analysis results. Core generate constraint files must be modified so that constraints are expressed using the proper hierarchical name of the configured cores in the top-level design.

5.15 SynplifyPro crash if PAD pins of BIBUF drive internal logic

Correct your design so that PAD pins of I/O macros can only be connected to top level ports of the design.

5.16 SynplifyPro mapping of sequential-shift to uSRAM does not support initial

values

PolarFire does not support initial values on registers (SLE) or Sequential-shift constructs mapped to uSRAM. If an initial value is specified for a register in the RTL code, the tool ignores the value and issues a warning.

5.17 Identify Debugger invoked through Libero opens an extra dialog box

Invoking Identify Debugger through Libero opens a dialog box about the Open View.

Workaround: Ignore the dialog box and click No. This will open the correct project in Identify Debugger through Libero. Another option is to open SynplifyPro interactively, configure Identify Debugger, and open it through SynplifyPro.

5.18 SynplifyPro version gives an error message for the Linux 7.4 platform

Checking the SynplifyPro version with following command returns an error message:

```
synplify_pro -version -batch
Error creating '"Internal Error: unsupported format used in message: '
Error creating '"Internal Error: unsupported format used in message: '
N-2017.09M-SP1-1
```

Note: In Libero, Add Profile -> Synthesis -> Version Name will display the same error message.

RHEL7.4 is supported and this message can be ignored.

5.19 RAM Initialization: SRAM_INIT_FROM_*_DONE and USRAM_INIT_FROM_*_DONE do not assert in specific scenarios

In the scenario where all LSRAM and USRAM instances that are initialized, are set to be initialized with zeroes, the PF_INIT_MONITOR signals SRAM_INIT_FROM_*_DONE and USRAM_INIT_FROM_*_DONE do not assert on powerup. Note that the initialization to zeroes was successful in this scenario. Rely on DEVICE_INIT_DONE to indicate completion of the initialization process. This issue will be fixed in the upcoming Libero SoC PolarFire v2.2 SP1 release.

5.20 PolarFire Core Generation Language

With Libero SoC PolarFire v2.2, some PolarFire cores generate only Verilog files, regardless of the preferred HDL language selected. Affected cores include:

- Cores in the PolarFire Features list
- Clocking: CCC, RC Oscillators, No-Glitch Mux
- Memories: DDR3, DDR4, LPDDR3, Large SRAM, Micro SRAM

VHDL users desiring to simulate designs containing affected cores must use mixed-language simulation (available with ModelSim ME Pro, which is bundled with Libero SoC PolarFire releases, and requires a Gold, Platinum, or Eval license).

5.21 SSTL15 ODT Values

In XT and ES devices, 20 Ohm and 30 Ohm terminations do not currently output the correct ODT value in SSTL15.

Workaround: Set 20 Ohm and 30 Ohm termination to the 40 Ohm termination value.

5.22 I/O Register Combining

Timing-driven I/O Register Combining is not supported in the PolarFire v2.2 release. If your pre-v2.2 PolarFire design uses BIBUF I/O's combined to a register, there is a risk of a functional failure on silicon in certain I/O register combining scenarios. For such designs, you must rerun Place and Route (that disables existing I/O register combining in the design) and generate an updated bitstream.

5.23 SDC set_false_path with [get_clocks] qualifiers is ignored by the placer

The SDC constraint set_false_path with [get_clocks] qualifiers is ignored by the placer; however, Verify Timing interprets it correctly.

Recommendation: Use set_clock_groups -asynchronous for clock domain crossing constraints.

5.24 SmartPower - Theta JA value is incorrectly reported in SmartPower reports

In SmartPower reports, the Theta JA value is always reported as "8" and is incorrect. Users should always use the value shown in the GUI, which is correct.

5.25 Hold Violations in Clock Domain implemented on Global Network

Your design may result in hold time violations in some register-to-register, register-to-MATH block or register-to-uSRAM paths. Enable Repair Minimum Delay Violations in Place and Route Options to have the Place and Route tool mitigate hold time violations.

5.26 Post-layout simulation is not supported

The Libero SoC PolarFire v2.2 release does not support post-layout simulation.

5.27 sNVM write fails due to ROM client created by previous design

In the scenario where a PolarFire device is first programmed with a design with an sNVM client, and then reprogrammed with a (different) design without an sNVM client, upon completion of programming with the second design, the sNVM client will not be erased. In such a case, if there are sNVM pages that are locked, writes to those pages will fail.

There is no programming action to erase SNVM completely.

Workaround: Create a dummy SNVM client (filled with 0's) in the second design.

5.28 Installation on Local Drive Only

This release is intended for installation only on a local drive. The Installer might report permission rights problems if the release is installed across a networked drive.

5.29 Installation

C++ installation error can be ignored. Required files will install successfully.

On some machines, the InstallShield Wizard displays a message stating:

The installation of Microsoft Visual C++ Redistributable Package (x86) appears to have failed. Do you want to continue the installation?

Click Yes and the software is installed successfully.

5.30 64-bit Linux package containing libpng12.so 64-bit library may be missing

In addition to the steps outlined in the Libero SoC Linux Environment Setup User Guide, Libero SoC PolarFire 2.2 (Linux) users must check to see if the 64-bit package containing the libpng12.so 64-bit library is installed. Follow the steps below to check/install the package on RHEL/CentOS 6 and RHEL/CentOS 7 systems.

RHEL/CentOS 6

1. Run the following command:

   ```
   yum provides libpng
   ```

2. Check the output and verify that libpng.*.el6_*.x86_64 is shown as installed.
3. If not installed, run the following command under root/sudo:

   ```
   yum install libpng.x86_64
   ```

RHEL/CentOS 7

1. Run the following command:

   ```
   yum list installed | grep png12
   ```

2. Check the output and verify that libpng12.x86_64 is shown as installed.
3. If not installed, run the following command under rtoot/sudo:

   ```
   yum install libpng12.x86_64
   ```

5.31 Installation on Windows 7

During Libero SoC PolarFire v2.2 installation on Windows 7 machines, you may see pop-up warning messages about shortcuts toward the end of installation process.

These messages can be safely ignored. Click OK to close the pop-up windows and the installation will proceed and complete as expected. All Windows shortcuts will appear correctly.

5.32 Antivirus Software Interaction

Many antivirus and HIPS (Host-based Intrusion Prevention System) tools will flag executables and prevent them from running. To eliminate this problem, users must modify their security setting by adding exceptions for specific executables. This is configured in the antivirus tool. Contact the tool provider for assistance.

Many users are running PolarFire successfully with no modification to their antivirus software. Microsemi is aware of issues for some antivirus tool settings that occur when using Symantec, McAfee, Avira, Sophos, and Avast tools. The combination of operating system, antivirus tool version, and security settings all contribute to the end result. Depending on the environment, the operation of Libero SoC PolarFire v2.2, ModelSim ME and/or Synplify Pro ME may or may not be affected.

All public releases of Libero software are tested with several antivirus tools before they are released to ensure that they are not infected. In addition, Microsemi's software development and testing environment is also protected by antivirus tools and other security measures.

6 System Requirements

The Libero SoC PolarFire v2.2 release has the following system requirements:

- 64-bit OS
  - Windows 7, Windows 8.1, or Windows 10 OS
  - RHEL 6.6 or later, RHEL 7, CentOS 6.6 or later, or CentOS 7
- A minimum of 32 GB RAM

Note: Setup instructions for using Libero SoC PolarFire v2.2 on Red Hat Enterprise Linux OS or CentOS are available here. As noted in that document, installation step 2 now includes running a shell script (bin/check_linux_req.sh) to confirm the presence of all required runtime packages.

7 Download Libero SoC PolarFire v2.2 Software

The following are available for download:

- Libero SoC PolarFire v2.2 for Linux
- Libero SoC PolarFire v2.2 for Windows
- Libero SoC PolarFire v2.2 MegaVault

Note: Installation requires administrative privileges.

After successful installation, clicking **Help-> About Libero** will show Version: 12.200.30.10