Programming and Debug Tools

PolarFire v2.2

Release Notes

6/2018

Microsemi

Power Matters.™

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Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision 1.0

Revision 1.0 is the first publication of this document (06/01/2018).

Reference Documents

PO0137: Product Overview PolarFire FPGA

DS0141: PolarFire FPGA Datasheet

UG0722: PolarFire FPGA Packaging and Pin Descriptions User Guide

Pin package Assignment Tables:

- MPF300T/MPF300TS-FCG484 Package Pin Assignment Table
- MPF300T/MPF300TS-FCVG484 Package Pin Assignment Table
- MPF300T/MPF300TS-FCSG536 Package Pin Assignment Table
- MPF300T/MPF300TS-FCG784 Package Pin Assignment Table
- MPF300T/MPF300TS-FCG1152 Package Pin Assignment Table

UG0752: PolarFire FPGA Power Estimator User Guide

UG0680: PolarFire FPGA Fabric User Guide

UG0684: PolarFire FPGA Clocking Resources User Guide

UG0686: PolarFire FPGA User I/O User Guide

UG0677: PolarFire FPGA Transceiver User Guide

UG0685: PolarFire FPGA PCI Express User Guide

UG0687: PolarFire FPGA 1G Ethernet Solutions User Guide

UG0727: PolarFire FPGA 10G Ethernet Solutions User Guide

UG0676: PolarFire FPGA DDR Memory Controller User Guide

UG0748: PolarFire FPGA Low Power User Guide

Athena TeraFire Cryptographic Algorithm Library (CAL) Users Guide

UG0743: PolarFire FPGA Debugging User Guide

UG0714: PolarFire FPGA Programming User Guide

UG0725: PolarFire FPGA Device Power-Up and Resets User Guide

UG0726: PolarFire FPGA Board Design User Guide

UG0753: PolarFire FPGA Security User Guide

UG0786: PolarFire FPGA Splash Kit User Guide

DG0755: PolarFire FPGA JESD204B Interface Demo Guide

DG0756: PolarFire FPGA PCIe Endpoint Demo Guide

DG0757: PolarFire FPGA 10GBASE-R Ethernet Loopback Demo Guide

DG0759: PolarFire FPGA Multi-Rate Transceiver Demo Guide

DG0762: PolarFire FPGA DSP FIR Filter Demo Guide

Verilog Simulation Guide

VHDL Simulation Guide

PolarFire FPGA Design Flow User Guide

PolarFire FPGA Macro Library Guide

PolarFire FPGA Design Constraints User Guide

PolarFire FPGA PDC Commands User Guide

PolarFire FPGA Timing Constraints User Guide

PolarFire FPGA Tcl Commands User Guide

PolarFire FPGA I/O Editor User Guide

Chip Planner User Guide

Netlist Viewer Interface User Guide

PolarFire FPGA Netlist Viewer User Guide

SmartPower User Guide

Timing Constraints Editor User Guide

SmartTime Static Timing Analyzer User Guide

PolarFire FPGA SmartDebug User Guide

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1 Programming and Debug PolarFire™ v2.2 Software Release Notes

The Programming and Debug Tools installer is intended for laboratory and production environments where Libero is not installed or needed. The installer installs the following tools:

- FlashPro (Available on Windows only)
- FlashPro Express
- SmartDebug

1.1 What's New in This Release

This release includes the following new features and enhancements.

1.1.1 FlashPro Express and FlashPro

Runtime improvements

- Runtime prior to device programming improved by 20%

1.1.2 SmartDebug

- sNVM and uPROM view enhancements
- New Programming Connectivity and Interface TCL commands have been added to Standalone SmartDebug
- Optimize DFE flow enhancements
- Power ON eye monitor option in Plot Eye
- Generate SmartDebug FPGA Array Data tool in Libero Design Flow

2   Design Migration – Cores

For information about design migration and cores for this release, see the [Libero SoC PolarFire v2.2 Release Notes](#).

3   Known Issues and Limitations

3.1   FlashPro Express - MPF300T_ES or MPF300TS_ES Programming File Fails to Program a MPF300XT Device

In FlashPro Express, the MPF300T_ES or MPF300TS_ES programming file cannot program a MPF300XT device, and vice versa.

Workarounds:

1. Export the programming file for the correct device name
2. Export a STAPL file from Libero and use standalone FlashPro on Windows in single mode to program.

3.2   Zeroization is Not Supported for ES and XT Devices

Zeroization is not supported for ES and XT devices. For more information, see the following documents:

ER0207 Errata: PolarFire FPGAs: Engineering Samples (ES) Devices

ER0215 Errata: PolarFire FPGAs: MPF300XT Devices

3.3   SmartDebug

This release includes the following limitations:

*   General Limitations
    *   Standalone SmartDebug: Non Microsemi Devices in chain: Microsemi devices present in chain along with non-Microsemi devices cannot be debugged using standalone SmartDebug. **Workaround**: Users should use SmartDebug through the Libero flow to debug Microsemi Devices.

    *   Standalone SmartDebug: ID Code of Microsemi device cannot be read when non-Microsemi device is connected in chain when using standalone SmartDebug.

        Workaround: Users should use SmartDebug through the Libero flow to perform this operation.
    *   Logical View: The logical view cannot be reconstructed for:

        *   LSRAM/uSRAM for port widths of x1 inferred through RTL.

        *   LSRAM/uSRAM configurations when a single net of output bus is used i.e. A_DOUT[0]/B_DOUT[0] for DPSRAM/uSRAM and RD[0] for TPSRAM and others are unused. The memories can be read/write using physical view.

        *   LSRAM/uSRAM configurations inferred using IP Cores CoreAHBLtoAXI (Verilog flow), CoreFIFO (Verilog and VHDL flow).

        *   HDL modules inferring RAM blocks that are instantiated in SmartDesign.

            Workaround: There are no workarounds for the issues above at this time.
    *   Physical View: RAM content read using the Physical View of SmartDebug for LSRAM 1Kx18 configuration (which are inferred through RTL) is incorrect. This is due to improper pin assignments on A_DIN and A_DOUT ports. This will be fixed in upcoming PolarFire releases.
*   Transceiver Limitations

- Plot eye introduces a burst of errors in data traffic on XCVR lanes when started. This will be fixed in an upcoming PolarFire release.

  Workaround: Enable Eye Monitor using the PowerOn Eye Monitor option before starting the traffic. This will poweron the DFE and EM receivers in CDR mode and no errors will be seen during eye plot.

- Plot eye on a lane configured in CDR mode does not work on a few lanes in Quad0 (this is specific to the MPF200T device).

  Workaround: There is no workaround at this time.

- The Custom DFE solution (using the Optimize DFE option in the Eye Monitor tab) does not work when the transceiver is configured in 8B10B PCS-PMA mode and the receiver is DFE.

  Workaround: Perform the following steps to obtain the expected eye output with PLOT_EYE.

  1. Assert PCS RX RESET
  2. Optimize DFE
  3. Plot Eye
  4. De-Assert PCS RX RESET

- After running Optimize DFE on a lane in CDR mode, users will see data errors when doing eye plot. This will be fixed in upcoming PolarFire releases.

- Optimize DFE on lanes configured in CDR mode does not work for SmartBERT IP patterns (this is specific to the MPF200T device). This will be fixed in upcoming PolarFire releases.

- Optimize DFE on lanes configured in DFE mode does not work reliably (this is specific to the MPF200T device). This will be fixed in upcoming PolarFire releases.

- SmartBERT IP does not work when lanes are configured at 250Mbps data rate.

- SmartBERT IP PRBS tests take more time to start/stop/inject error on RHEL 7.x and Cent OS 7.x platforms as compared to RHEL 6.x and Windows OS. This issue is seen only with PRBS patterns from SmartBERT IP, and will be fixed in upcoming PolarFire releases.

- The Power ON eye monitor TCL command (eye_monitor_power) does not work correctly in PolarFire v2.2. RX PLL does not lock to the incoming data after this TCL command is run. This will be fixed in upcoming PolarFire releases.

  Workaround: There are no workarounds for the issues above at this time.

- Signal Integrity Limitation

  - The RX Polarity Signal Integrity parameter (Polarity P/N reversal) has no effect when a PDC file is imported using the Import option in SmartDebug. This flow works fine in GUI mode. This will be fixed in upcoming PolarFire releases.

3.4 Installation on Local Drive Only

This release is intended for installation only on a local drive. The Installer might report permission rights problems if the release is installed across a networked drive.

3.5 Installation

C++ installation error can be ignored. Required files will install successfully.

On some machines, the InstallShield Wizard displays a message stating:

The installation of Microsoft Visual C++ Redistributable Package (x86) appears to have failed. Do you want to continue the installation?

Click Yes and the software is installed successfully.

3.6   Installation on Windows 7

During Libero SoC PolarFire v2.2 installation on Windows 7 machines, you may see pop-up warning messages about shortcuts toward the end of installation process.

These messages can be safely ignored. Click OK to close the pop-up windows and the installation will proceed and complete as expected. All Windows shortcuts will appear correctly.

3.7   Antivirus Software Interaction

Many antivirus and HIPS (Host-based Intrusion Prevention System) tools will flag executables and prevent them from running. To eliminate this problem, users must modify their security setting by adding exceptions for specific executables. This is configured in the antivirus tool. Contact the tool provider for assistance.

Many users are running PolarFire successfully with no modification to their antivirus software. Microsemi is aware of issues for some antivirus tool settings that occur when using Symantec, McAfee, Avira, Sophos, and Avast tools. The combination of operating system, antivirus tool version, and security settings all contribute to the end result. Depending on the environment, the operation of Libero SoC PolarFire v2.2, ModelSim ME and/or Synplify Pro ME may or may not be affected.

All public releases of Libero software are tested with several antivirus tools before they are released to ensure that they are not infected. In addition, Microsemi's software development and testing environment is also protected by antivirus tools and other security measures.

4 System Requirements

The Programming and Debug PolarFire v2.2 release has the following system requirements:

- 64-bit OS
  - Windows 7, Windows 8.1, or Windows 10 OS
  - RHEL 5, RHEL 6, RHEL 7, CentOS 5, CentOS 6, or CentOS 7
    - Programming is not supported on RHEL 5, CentOS 5
- A minimum of 32 GB RAM

Note: Setup instructions for using Programming and Debug PolarFire v2.2 on Red Hat Enterprise Linux OS or CentOS are available here. As noted in that document, installation step 2 now includes running a shell script (bin/check_linux_req.sh) to confirm the presence of all required runtime packages.

Note: Programming and Debug PolarFire v2.2 does not support the OS versions listed below. For more information, refer to PCN17031.

- RedHat Enterprise Linux 5.x through 6.5
- CentOS 5.x through 6.5

5   Download Programming and Debug Tools PolarFire v2.2 Software

The following are available for download:

- [Programming and Debug Tools PolarFire v2.2 for Linux](#)
- [Programming and Debug Tools PolarFire v2.2 for Windows](#)

Note: Installation requires administrative privileges.